



# Single Event Upsets in ATLAS SCT

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Topical Workshop on Electronics for  
Particle Physics  
Perugia, 26<sup>th</sup> September 2013

# Single Event Upsets in ATLAS SCT

- Single Event Upsets (SEU) studied for ATLAS & CMS in test beams but this is first reported study of SEU in ASICs in LHC operation.
- Expectations for (SEU) from test beam data.
- SEU in SCT operation and comparisons with test beam
  - *p-i-n* diodes in TTC link.
  - DAC threshold registers in FE ASIC: ABCD.
- Mitigation for ATLAS operation.
- Mitigation strategy for SEUs at HL-LHC.

# SEUs in SCT, how and where?

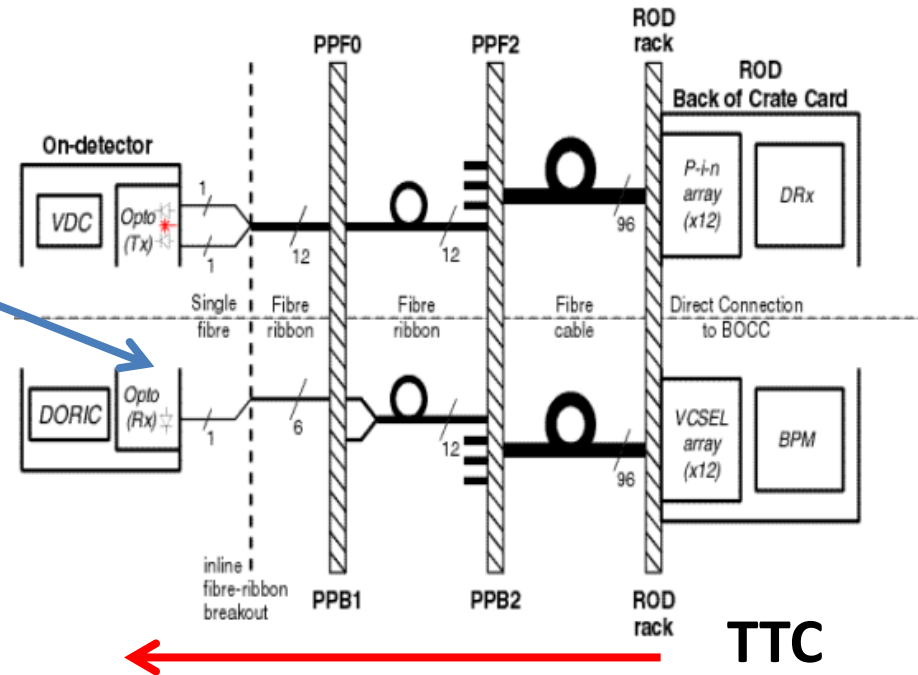
- **Particles deposit sufficient charge in small region of silicon → bit error (SEU)**
  - Typically needs nuclear interaction to deposit sufficient energy, i.e. MIPs are harmless.
- **In *p-i-n* diode that receives optical TTC signal**
  - Single bit error → loss of synchronisation of a FE module.
- **In static registers in ABCD**
  - Don't care about dynamic memory (pipeline) but static registers will stay wrong after an SEU until reset.
  - Look at effects in DAC threshold register.

# SEU Studies

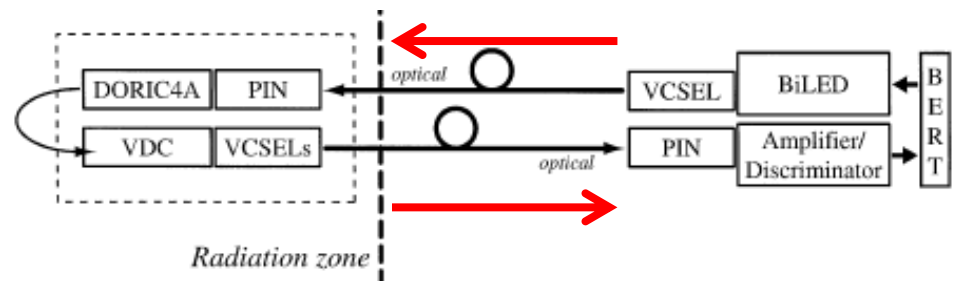
- **Measure SEU rates for prototype in test beams:**
  - Low energy  $\pi/p$  beams (mainly 200 – 500 MeV/c)
  - Extrapolate to LHC spectrum?
  - No synchronisation with beam bunches.
  - Angle of incidence.
- **Measure actual SEU rates in ATLAS operation and compare with test beam based predictions.**
  - Results shown for barrel SCT only.

# SEU In SCT Optical Links

- On-detector *p-i-n* diode is Sensitive to SEU
  - Small electrical signal before amplifier stage.

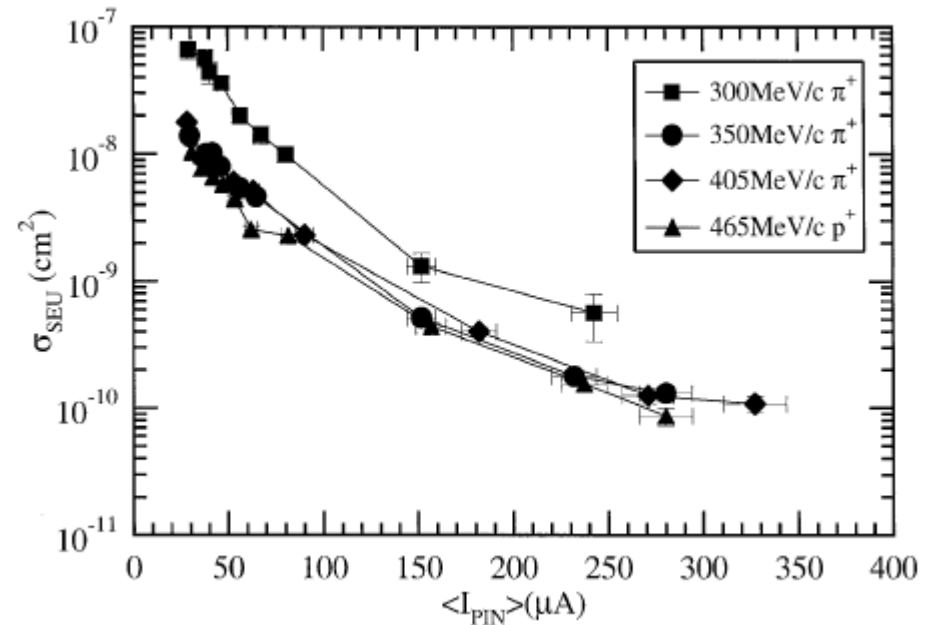


- Measure BER with loopback
  - With beam
  - Without beam
  - Difference → SEU



# SEU in *p-i-n* diode – Test Beam

- Measured SEU vs current in *p-i-n* diode  $I_{PIN}$  (simple loopback test) .
  - No errors with beam off.
  - No errors for MIPs.
  - Measured Bit Error Rate vs  $I_{PIN}$  with beam on.
  - ac coupled  $\rightarrow$  charge required to cause bit flip is proportional to  $I_{PIN}$  .
- $\sigma$  higher for 300 MeV/c  $\pi$  because of  $\Delta$  resonance  $\rightarrow$  large variation of  $\sigma$  with energy  $\rightarrow$  difficult to predict rates for LHC operation.



$$\sigma(\text{SEU}) = \# \text{ bit errors/fluence}$$

J.D. Dowell et al., Single event upset studies with the optical links of the ATLAS semiconductor tracker, Nucl. Instr. Meth. A 481 (2002) 575.

# SEU in ATLAS Operation (1)

- *p-i-n* diode receives optical TTC signal.
- Indirect measurement BER
- Signature for SEU in *p-i-n* diode is loss of synchronisation for L1A trigger:
  - TTC sends
    - full L1A number to ROD: L1A(full)
    - L1A signal to detector FE via optical links.
  - On-detector 4 bit counter counts L1A and returns 4 LSBs in data stream: L1A(4)
  - SEU causes 0→1 can cause loss of L1A on-detector.
  - Compare L1A(full) with L1A(4). Persistent discrepancy is SEU.
- No errors seen in “physics mode” running with no beam  
→ suspect that these errors during beam are due to SEU.

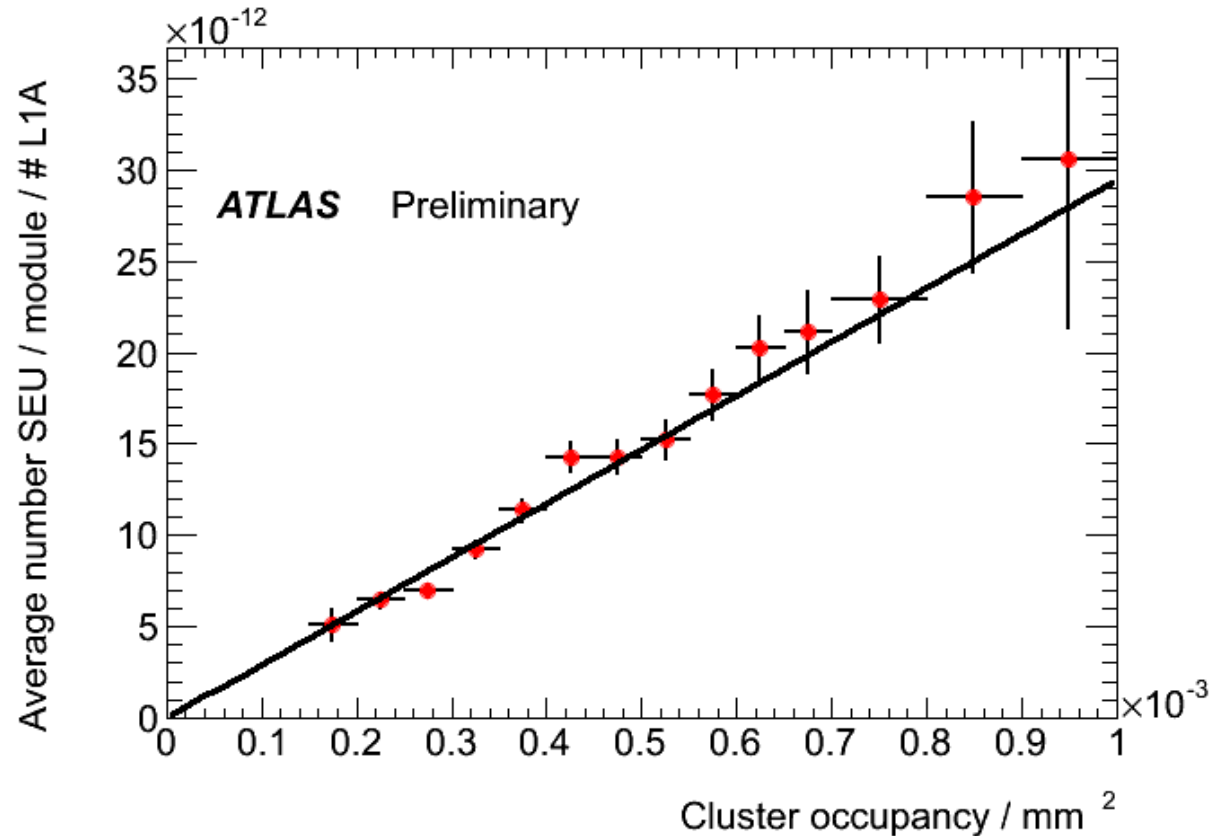
# SEU in ATLAS Operation (2)

- L1A signal is 110
- Short code vulnerable to single bit error (minimize latency).
- Assume  $0 \rightarrow 1$  transitions more probable than  $1 \rightarrow 0$  because of high value of  $I_{PIN}$ .
- Most probable error “110”  $\rightarrow$  “111”
- In ATLAS energy deposition synchronised to bunch crossing, unlike test beam
- Creates large uncertainties in extrapolating test beam cross section to ATLAS operation.



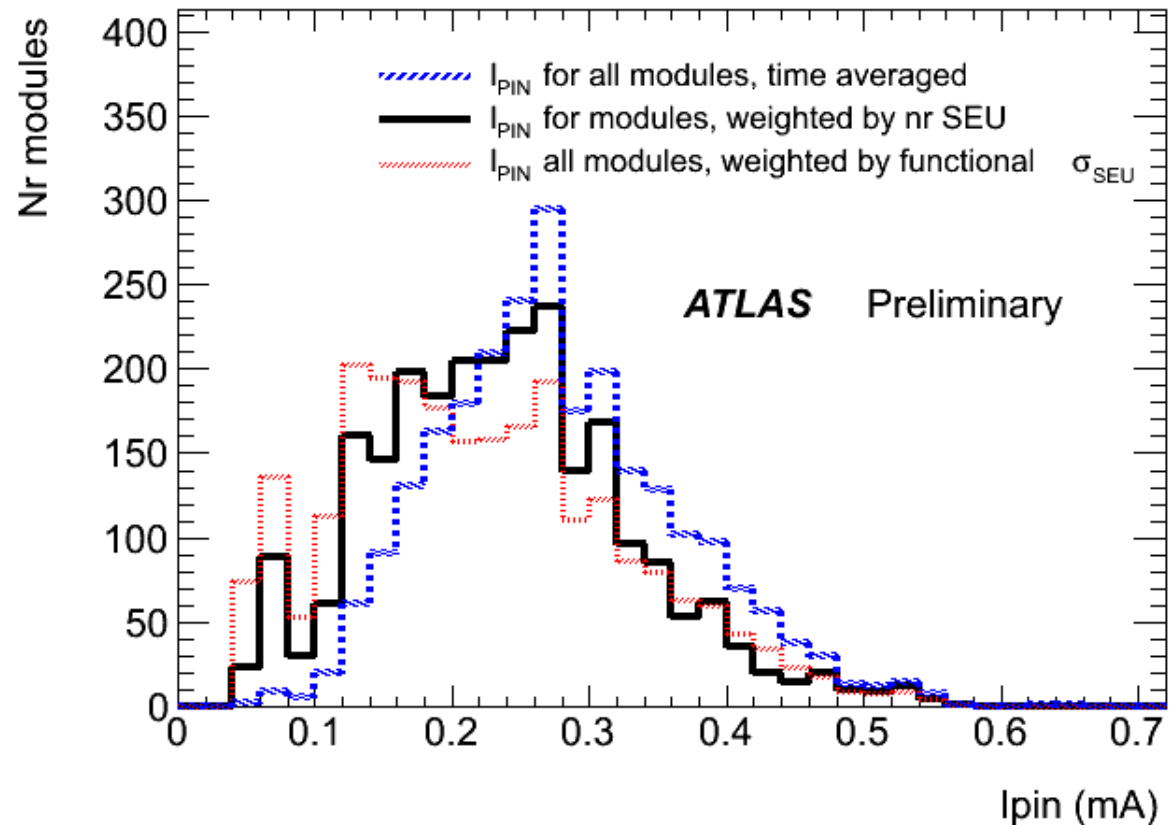
# Are errors really SEU (1) ?

- SEU rate should scale with module occupancy (proxy for particle flux).
- Occupancy changes from luminosity variations and decreases as radius of barrels increase
- Shows expected linear behaviour



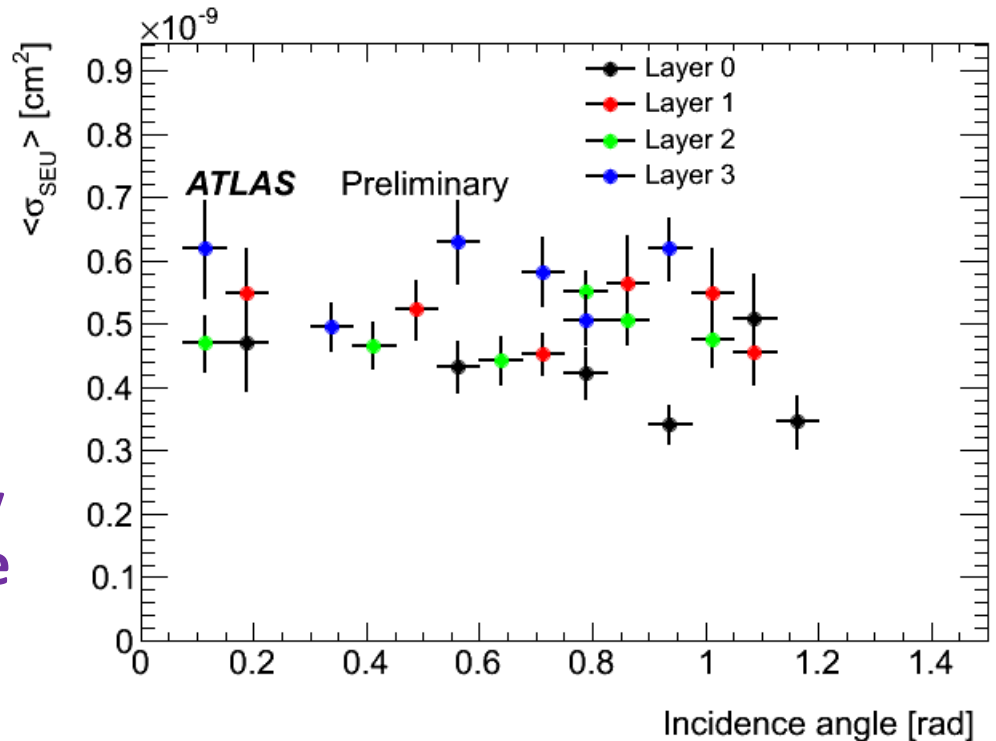
# Are errors really SEU (2) ?

- SEUs should be biased towards modules with low values of  $I_{PIN}$
- Compare:
  - All modules
  - Weighted by SEU
  - Model prediction based on exponential fit to test beam  $\sigma(SEU)$ .



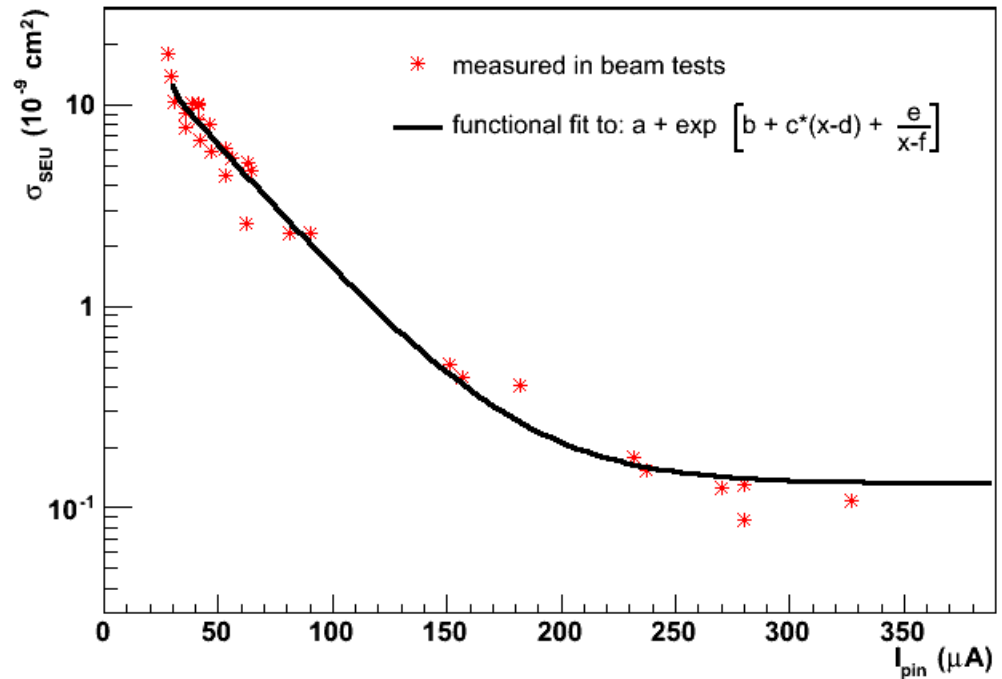
# Angular Dependence?

- Normalise SEU rate by cluster occupancy (flux).
- Look at normalised rates vs incident angle in 4 barrel layers.
- No significant effect.
- Possible explanation:
  - High  $I_{pin}$   $\rightarrow$  large energy threshold for SEU  $\rightarrow$  rate volume of active region ( $p-i-n$  diode is a micro-calorimeter).



# Absolute Rates (1)

- Many uncertainties
  - Fit to  $\sigma(\text{SEU})$  vs  $I_{\text{PIN}}$  (ignore data at 300 MeV/c)
  - Don't know how to make extrapolation to ATLAS particle spectra → large uncertainty
  - Different beam conditions
    - ATLAS r/o synchronised to bunch crossings
    - Test beam asynchronous



# Absolute Rates (2)

- Naïve prediction:
  - $N(\text{SEU}) = \sigma(\text{SEU}) * \text{Fluence}$
  - Ignore variation in  $\sigma(\text{SEU})$  with LHC spectrum.
  - Corrected for variation of  $\sigma(\text{SEU})$  with  $I_{\text{PIN}}$ .
  - Fluence: use <module occupancy>
  - Reject long SEU bursts (>60s) 13% uncertainty
  - Reject modules with multiple errors in one run: 5 to 6% bias.
- Number SEU in data set
  - Luminosity  $7.81 \text{ fb}^{-1}$
  - Measured: 2504
  - Predicted : 1949
  - Good agreement within large uncertainties.

# SEU in ABCD DAC registers

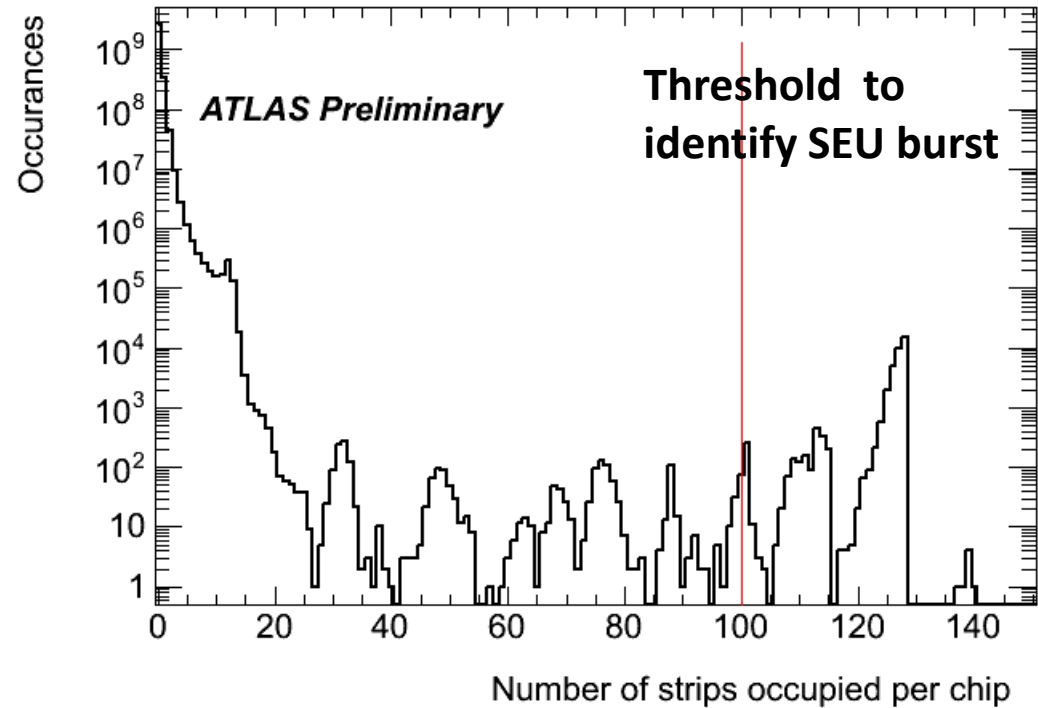
- **Test beam studies:**
  - PSI 200 MeV/c  $\pi^+$  angle of incidence 79°.
- **No simple read/write test for registers in ABCD.**
  - Indirect determination using mask register at o/p of pipeline.
  - Assume SEU rate in mask register same as DAC.
  - Measured 0  $\rightarrow$  1 errors but expect cross section for 1  $\rightarrow$  0 to be larger (according to ABCD chip designer).
- **Fluence/SEU =  $3.7 \cdot 10^{13} \pi/\text{cm}^2/\text{SEU}$** 
  - **Some batch to batch variations**
- L. Eklund et al., SEU rate estimates for the ATLAS/SCT front-end ASIC, Nucl. Instr. Meth. A 515 (2003) 415.

# SEU in ATLAS Operation

- Indirect measure SEU.
- SEU in DAC threshold register change discriminator threshold for that ABCD:
  - (1)  $1 \rightarrow 0$  bit flip  $\rightarrow$  increase in chip occupancy
  - (2)  $0 \rightarrow 1$  bit flip  $\rightarrow$  decrease in chip occupancy
  - In practice only sensitive to the 5<sup>th</sup> bit.
- Easier to look for effect (1) than (2).
- Effect should persist until module reset
  - Look for chips with persistently high occupancy.

# Chip Occupancy

- 128 strips/chip
- Average over 10 events
- Mean occupancy very low as expected.
- Spike at 128 → every strip fires every event
- Also see rarer spikes from when all strips fire in 9 or 8 events (start or end of burst)

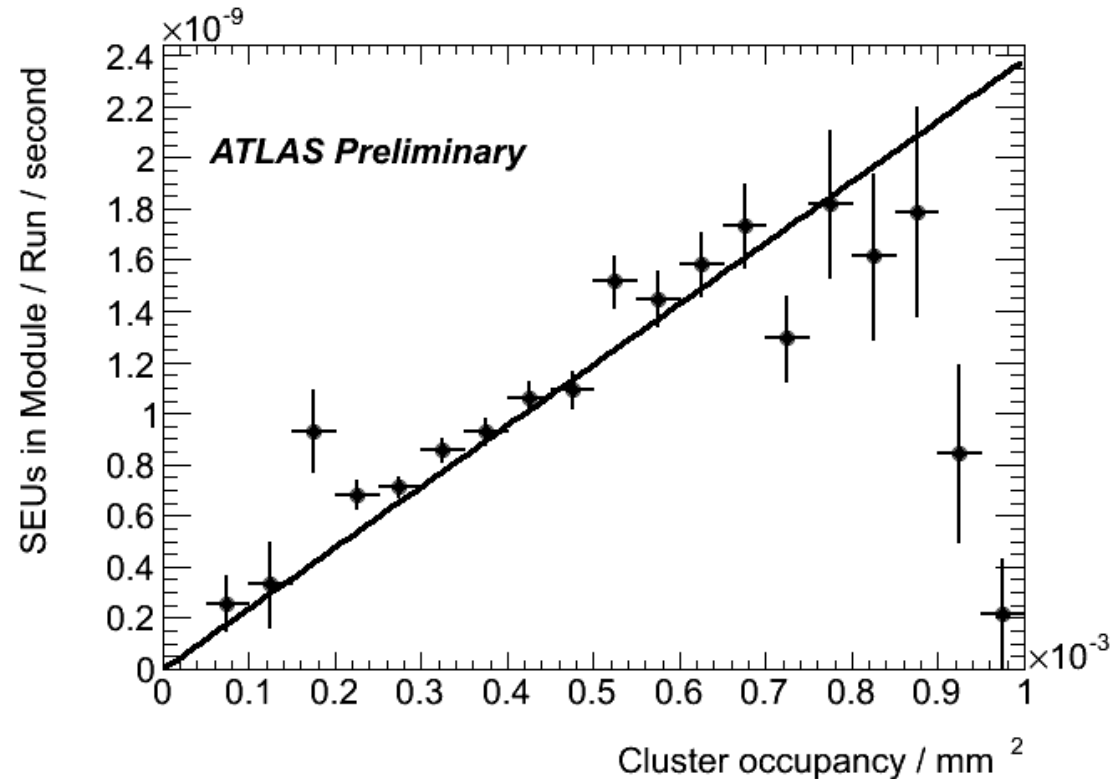


Note compressed log scale on y-axis  
Vary threshold to identify start of burst but lower fixed threshold at 50 for end of burst.



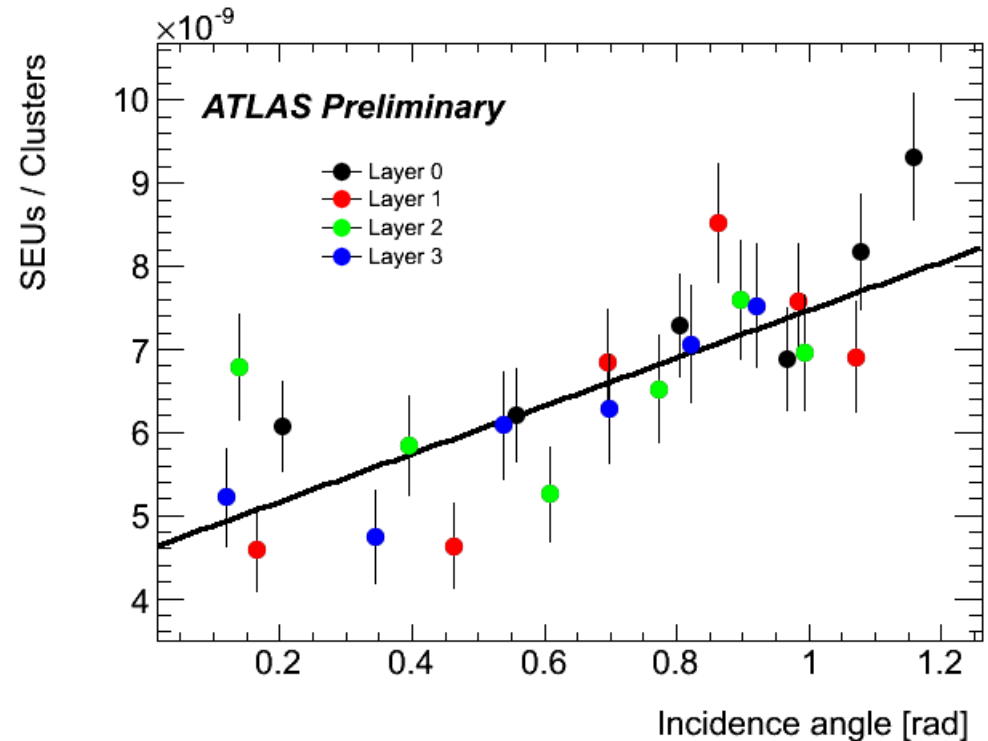
# Are Errors Real SEU?

- Plot SEU rate vs chip occupancy per event (proxy for particle flux)
- See expected linear slope.



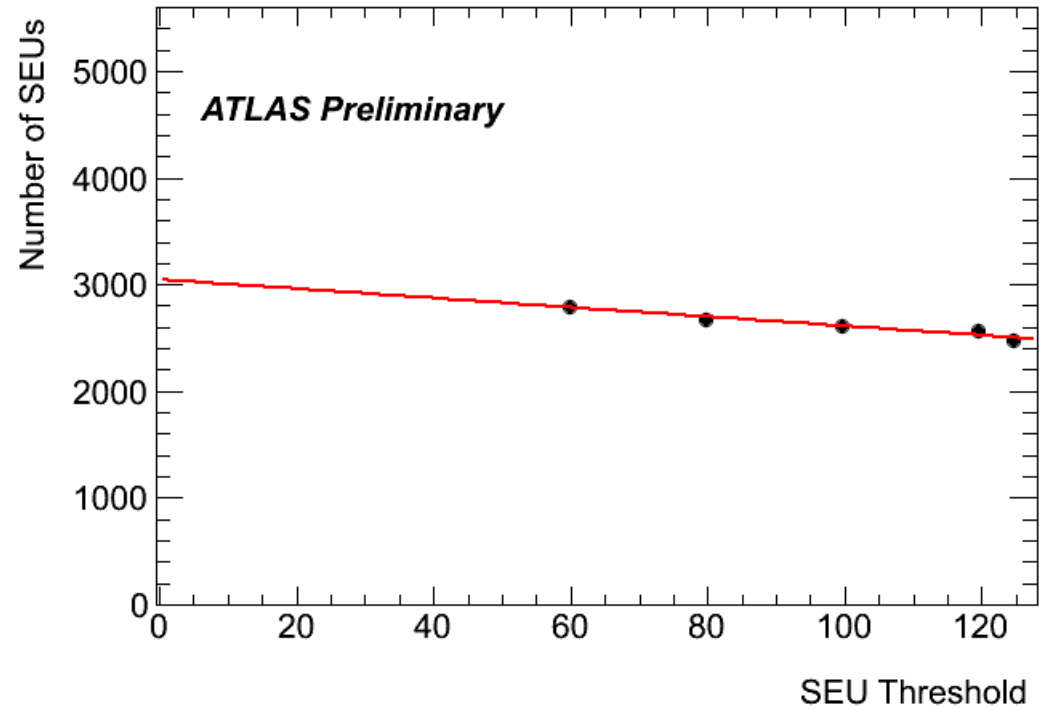
# Angular Dependence

- Measure SEU/cluster occupancy vs incidence angle for barrel layers.
- See increase in rate with angle.
- Linear fit to compare PSI data at  $79^\circ$  with ATLAS data.



# Absolute Predictions (1)

- Measure SEU rates as a function of threshold in number of hits/chip used to identify SEU bursts.
- Use fit to extrapolate to 0 threshold  
→ measured # SEU.
  - 3% uncertainty from extrapolation.

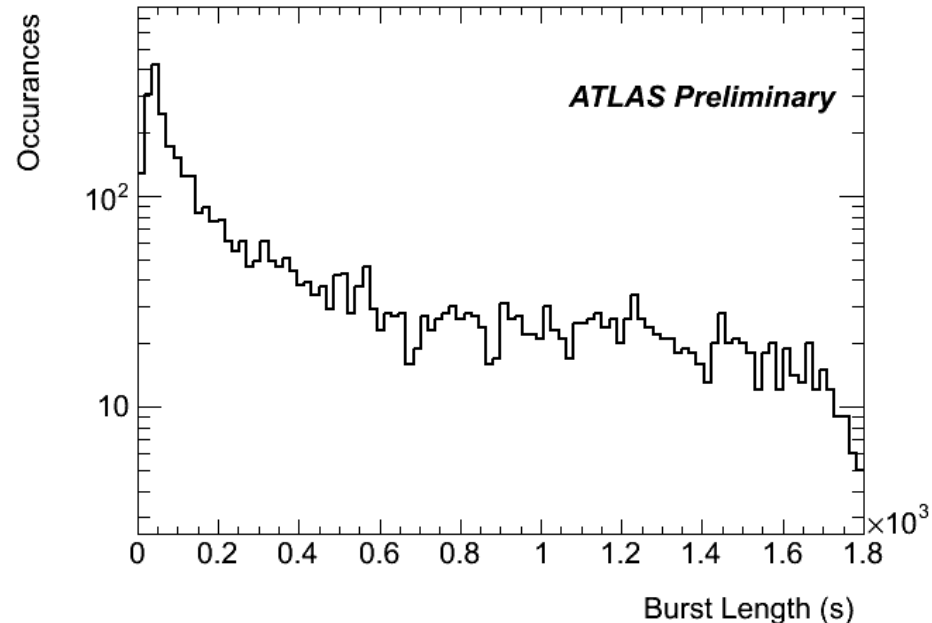
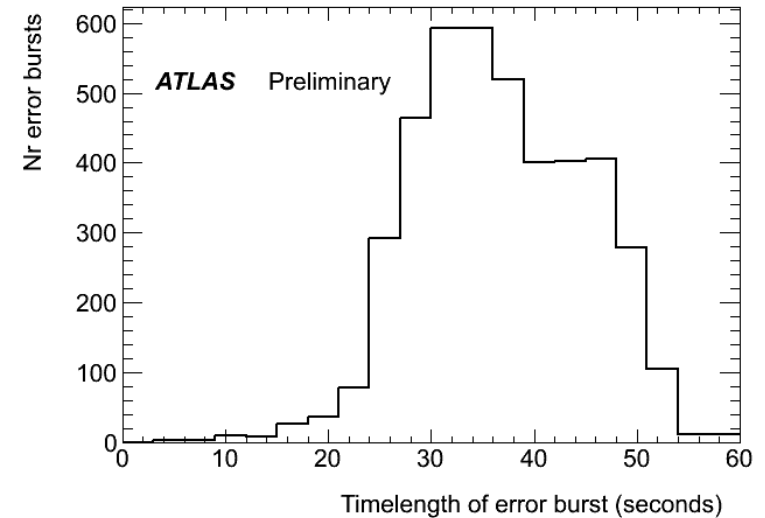


# Absolute Predictions (2)

- Don't know how to scale  $\sigma(\text{SEU})$  for  $\pi$  at 200 MeV/c to LHC spectrum  $\rightarrow$  large uncertainty
- Naïve model:
  - $N(\text{SEU}) = \sigma(\text{SEU}) * \text{Fluence}$
  - Fluence: FLUKA simulations scaled to luminosity
  - Results for inner barrel layer scaled to other layers using measured chip occupancies.
  - Corrected for angular dependence observed in data.
- # SEU in  $23.4 \text{ fb}^{-1}$ :
  - Measured: 3046
  - Predicted: 1090
- Understand rates to within a factor  $\sim 3$ .

# Mitigation Strategies for ATLAS Operation

- SEU in TTC links
  - Use large values of  $I_{PIN}$  ( $> 100 \mu\text{A}$ ) to reduce  $\sigma(\text{SEU})$
  - Reset pipeline in FE chips and all counters if this de-synchronisation detected by DAQ (20 to 50s).
- SEU in DAC register
  - Operator reset of module with high occupancy.
  - Full reset of all modules every 30 minutes.
- Mitigation strategies reduce effects of SEU to negligible level.



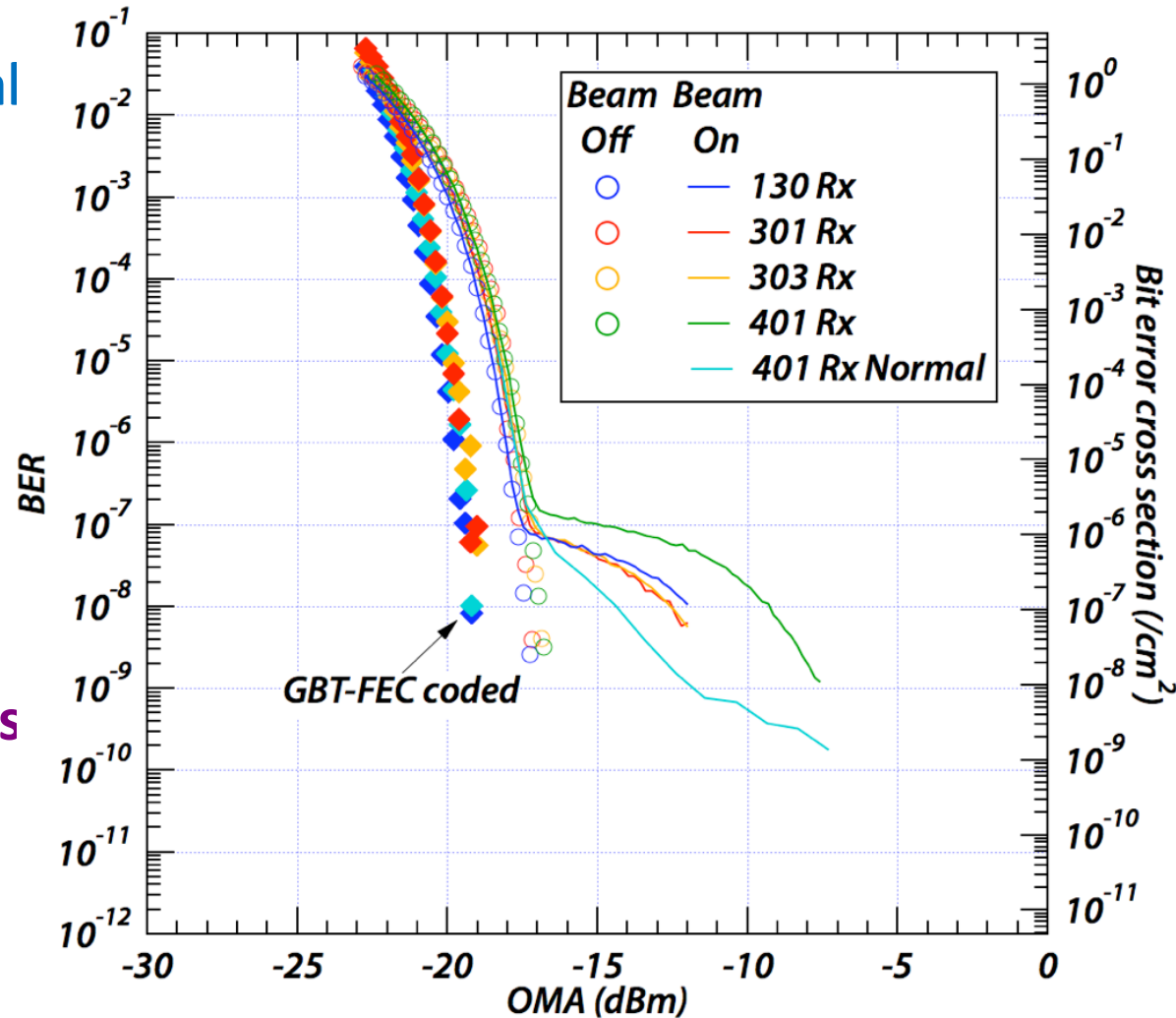
# SEUs @ HL-LHC

- **Expect SEUs to be more important @ HL-LHC because of higher Luminosity.**
- **What can we do to mitigate SEU?**
  - Triple event redundancy in gates
  - Error correction on TTC link. P
  - Propose to correct for sequence of error bursts up to 16 bits long → slide.

# Versatile Link TTC SEU

- Measured BER vs optical power, Optical Modulation Amplitude (OMA).
- SEU killed by error correction (FEC) → Error correction required for TTC links
- Tests to determine if it is also required for data

A. Jimenez Pacheco et al., Single-Event Upsets in Photoreceivers for Multi-Gb/s Data Transmission, IEEE Trans. Nucl. Sci., Vol. 56, Iss. 4, Pt. 2 (2009), pp. 1978 – 1986.



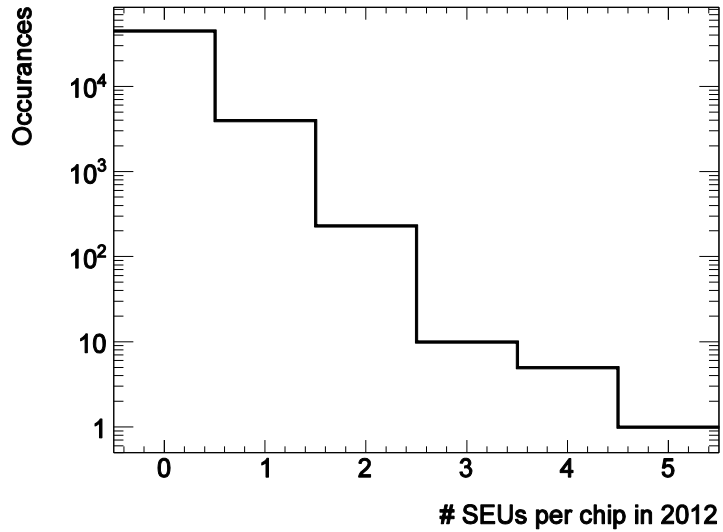
# SEU Summary

- **SEUs expected in SCT readout.**
- **Clear evidence of SEUs in ATLAS operation:**
  - Predicted rates in  $\sim$  agreement with measurements.
  - Mitigation strategies work well.
- **Mitigation strategies planned for HL-LHC should minimize impact of SEU.**



# Backup Slides

# Number SEUs/chip



# Burst Length SEU p-i-n

