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The eCDR, a Radiation-Hard 40/80/160/320 Mbit/s CDR with internal VCO frequency calibration and 195 ps programmable phase resolution in 130 nm CMOS

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A clock and data recovery IP, the eCDR, is presented which is intended to be implemented on the detector front-end ASICs that need to communicate with the GBTX by means of e-links. The programmable CDR accepts data at 40, 80, 160 or 320 Mbit/s and generates retimed data as well as 40, 80, 160 and 320 MHz clocks that are aligned to the retimed data. Moreover, all the outputs have a programmable phase with a resolution of 195 ps. The radiation-hard design, integrated in a 130 nm CMOS technology, operates at a supply voltage between 1.2 V and 1.5 V.

Summary

The GBT project, currently under development as part of the LHC upgrade program, aims at the realization of a radiation-hard chipset to be used as an on-detector transceiver to implement radiation-hard optical links between the counting room and the detector front-ends. In order to establish the communication between the front-ends and the GBT by means of the e-links, the presented CDR has been developed. This eCDR operates with 40, 80, 160 or 320 Mbit/s data to comply with the e-links specification. Apart from recovering the received data, the eCDR also generates in-phase clocks at 40, 80, 160 and 320 MHz, regardless of the data rate. These clocks can be used as a local reference for the front-ends. The eCDR is implemented in a 130 nm CMOS technology, it is able to operate at a supply voltage between 1.2 V and 1.5 V and is fully radiation-hardened.
In order for a CDR to lock, its VCO should oscillate at a frequency very close to the incoming data rate. The eCDR incorporates 2 measures to accomplish this, namely an external and an internal calibration system. The external calibration phase-locks the VCO to an external reference clock before initiating the CDR operation. On the contrary, the internal calibration system does not require an external reference and can bring the VCO close to the required oscillation frequency all by itself. The frequency generated by the internal calibration can be set with a 6-bit word. Excellent temperature stability of 96 ppm/°C has been shown in simulation.
When the eCDR is locked, the loop is controlled by means of a phase-detector (PD) measuring the phase difference between the divided VCO clock and the incoming data. The VCO control voltage is then steered to compensate for this difference. When switching between the calibration phase and CDR operation or in the case of an SEU, it can happen that the VCO frequency deviates significantly from the data frequency. Because the loop based on the PD has a limited locking range, a frequency detector (FD) loop has been incorporated as well in order to extend the locking range. The dynamics of the 2 loops can be set independently.
As mentioned before, the output clocks of the eCDR, which are always in-phase with the retimed data, can be used as a reference for the front-end. To make these clocks even more useful, their phase, as well as the phase of the retimed data, can be set with a very fine resolution of 195 ps. As such, the output clocks can be aligned to the bunch crossing or to another clock in the front-end. This has been realized by making use of the 16 phases of the 8-stage differential VCO running at 320 MHz.
The eCDR has been conceived as a radiation-hard circuit. Therefore, all digital blocks are triplicated while the analog cells have been designed to minimize the effect of SEUs. The used technology is inherently tolerant to total ionizing dose. The eCDR consumes less than 40 mW.

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