

GBT Project Status

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On behalf of the GBT team

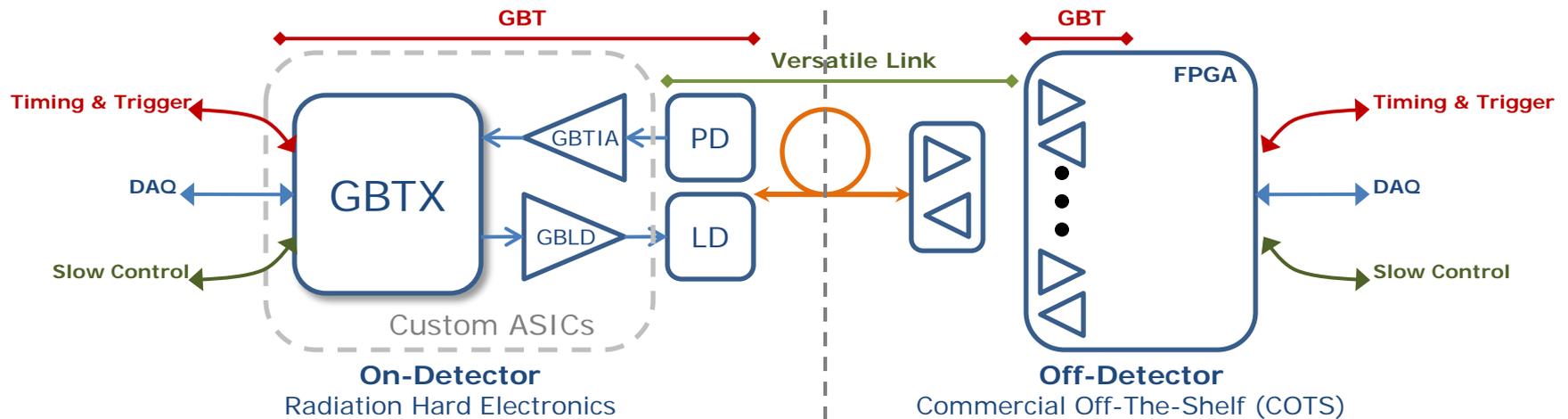
TWEPP, 26 September 2013

Perugia, Italy

Outline

- Radiation Hard Optical Link Architecture
- The GBT System
- GBLD Status
- GBTIA Status
- GBTX:
 - Data Bandwidth
 - Functionality
 - ASIC Status
 - Testing Status
 - GBTX Future
- GBT-SCA Status
- GBT Building Blocks Status
- GBT-FPGA Status

Radiation Hard Optical Link Architecture



GBLD Status

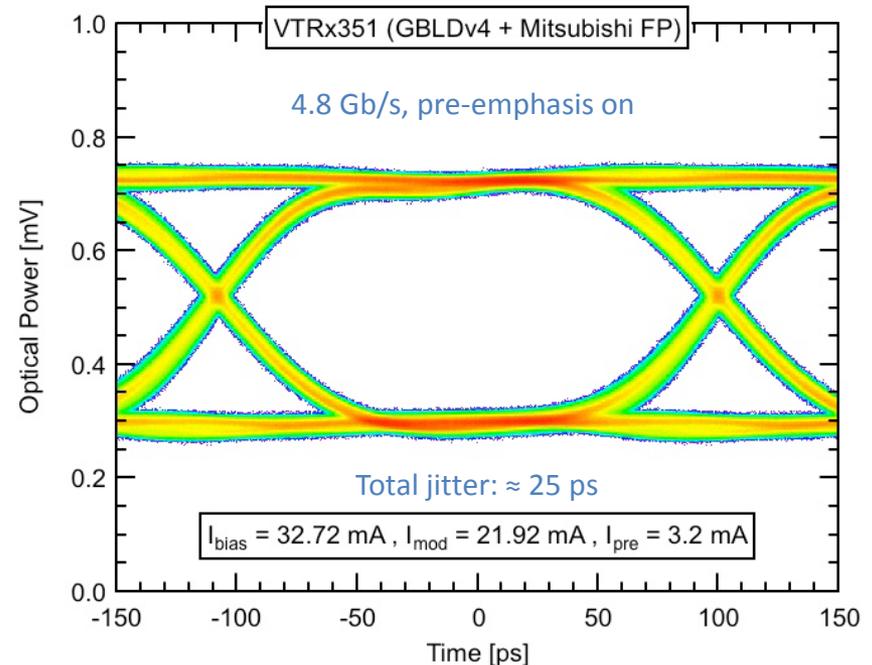
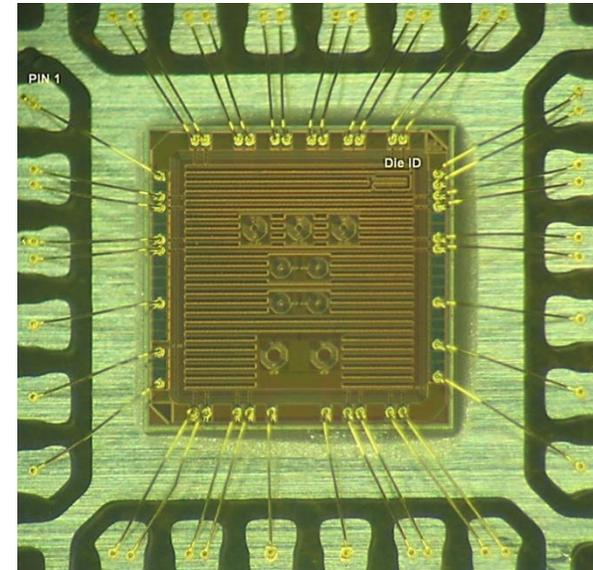
GBLD V4.1

• Main Specs

- Bit rate 5 Gb/s (min)
- Modulation:
 - Current sink
 - Single-ended/differential
- Laser modulation current: 2 to 24 mA
- Laser bias: 2 to 43 mA
- Equalization:
 - Pre-emphasis/de-emphasis
 - Independently programmable for rising/falling edges
- Supply voltage: 2.5 V
- Die size: 2 mm × 2 mm
- I2C programming interface

• Status

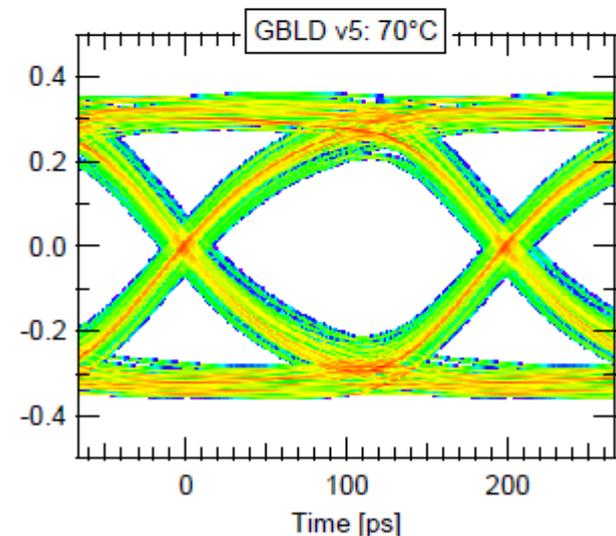
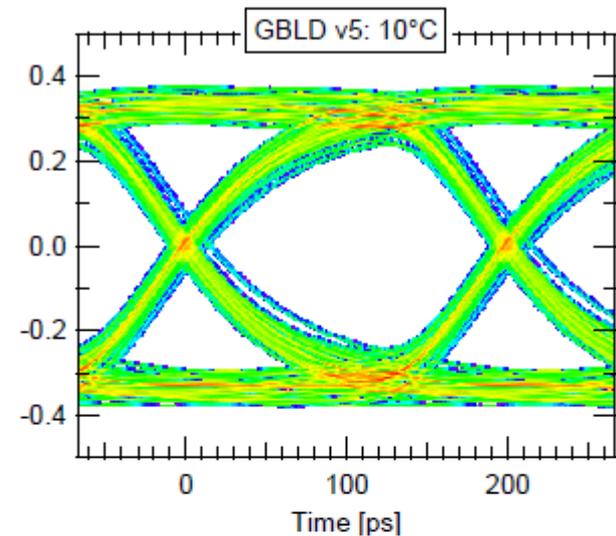
- Available in small quantities
 - Integrated in the VTRx and VTTx
- Fully functional
- Excellent performance
- Radiation hardness proved (total dose)
- Final SEU tests to be done October 2013
- Technology: 130 nm DM metal stack
- Device is production ready



LpGBLD Status

Low power GBLD (LpGBLD)

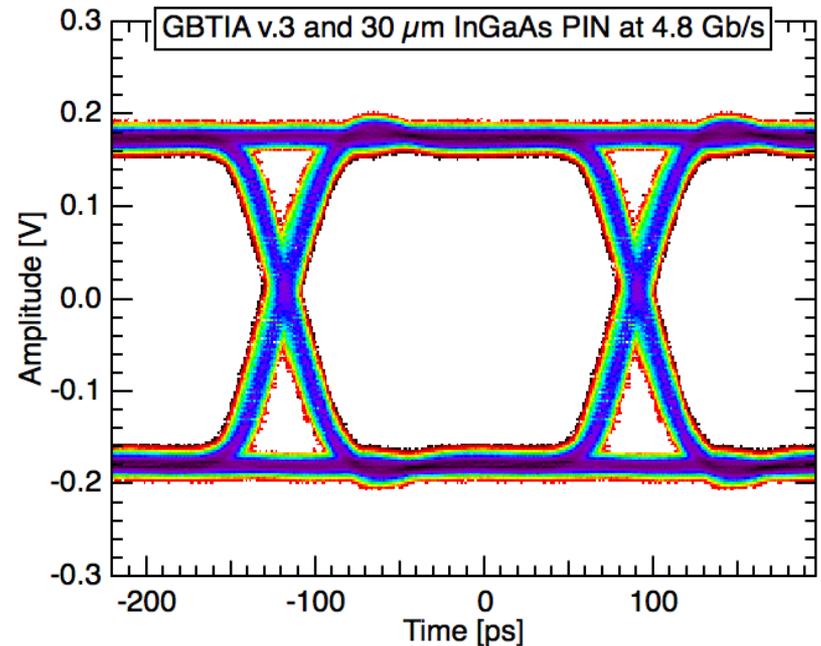
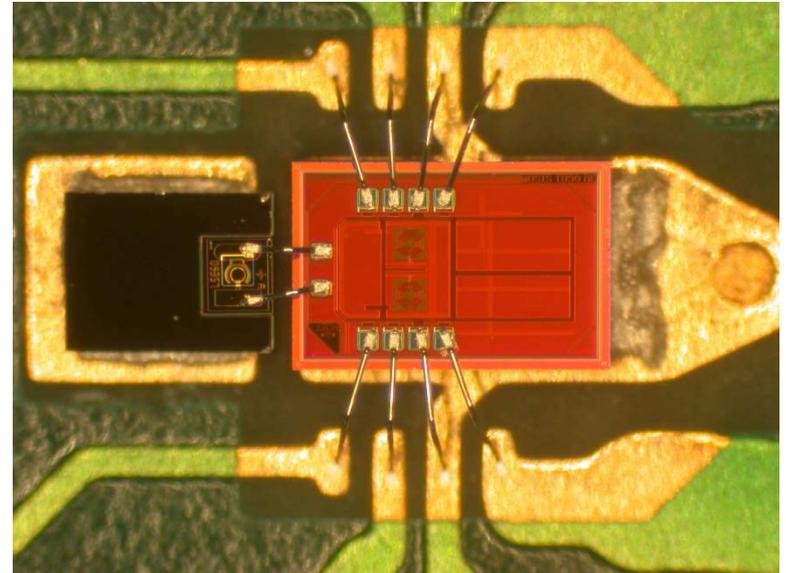
- **Main Specs, mostly as for GBLD V4 but:**
 - VCSEL driver only:
 - Lower modulation current:
 - 12 mA max
 - Power consumption reduced by 40%
 - VCSEL choice is determinant
 - Min: 138 mW
 - Max: 325 mW
 - Uses the LM stack:
 - It can be fabricated with GBTIA and GBTX
- **Status:**
 - Devices available in small quantities
 - Electrically characterization done
 - Performance is good at ambient temperature:
 - Slower than GBLD V4 as expected
 - At high temperatures (> 70) the electrical performance degrades slightly
 - When convolved with the laser response at high temperatures the performance falls behind specs:
 - Further studies require to evaluate performance with multiple VCSEL devices



GBTIA Status

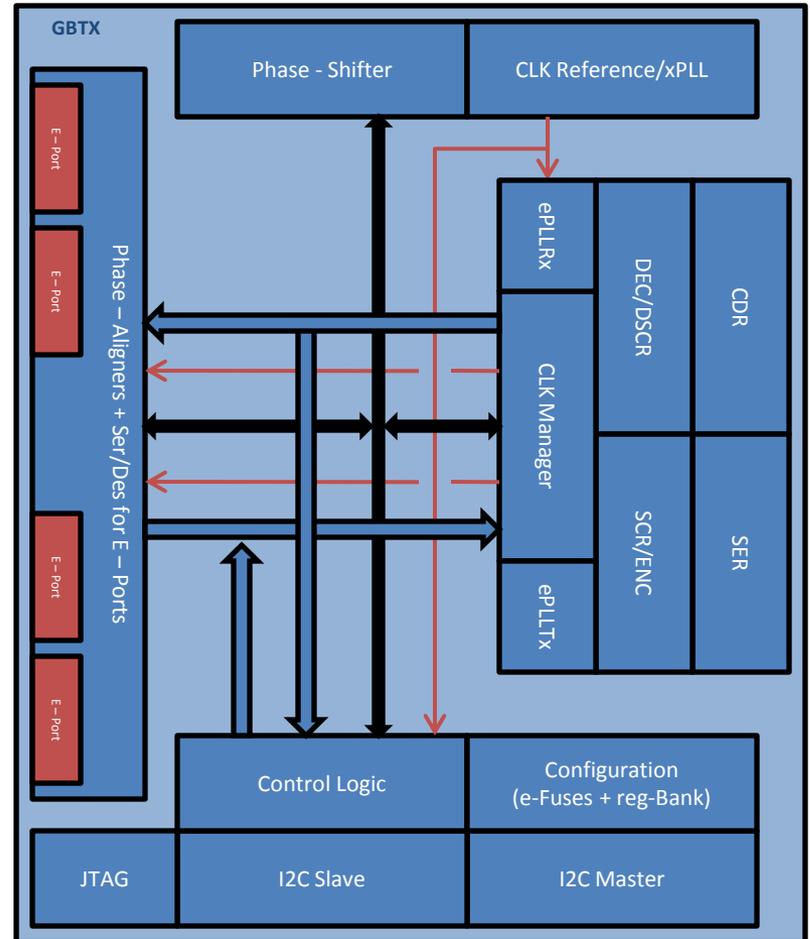
GBTIA V2.0 / V2.1

- **Main specs:**
 - Bit rate 5 Gb/s (min)
 - Sensitivity: 20 μ A P-P (10^{-12} BER)
 - Total jitter: < 40 ps P-P
 - Input overload: 1.6 mA (max)
 - Dark current: 0 to 1 mA
 - Supply voltage: 2.5 V
 - Power consumption: 250 mW
 - Die size: 0.75 mm \times 1.25 mm
- **Status:**
 - Fully functional
 - Excellent performance
 - Radiation hardness proved
 - Tested up to 200 Mrad (SiO_2)
 - Device is production ready
 - LM metal stack



GBTX Data Bandwidth

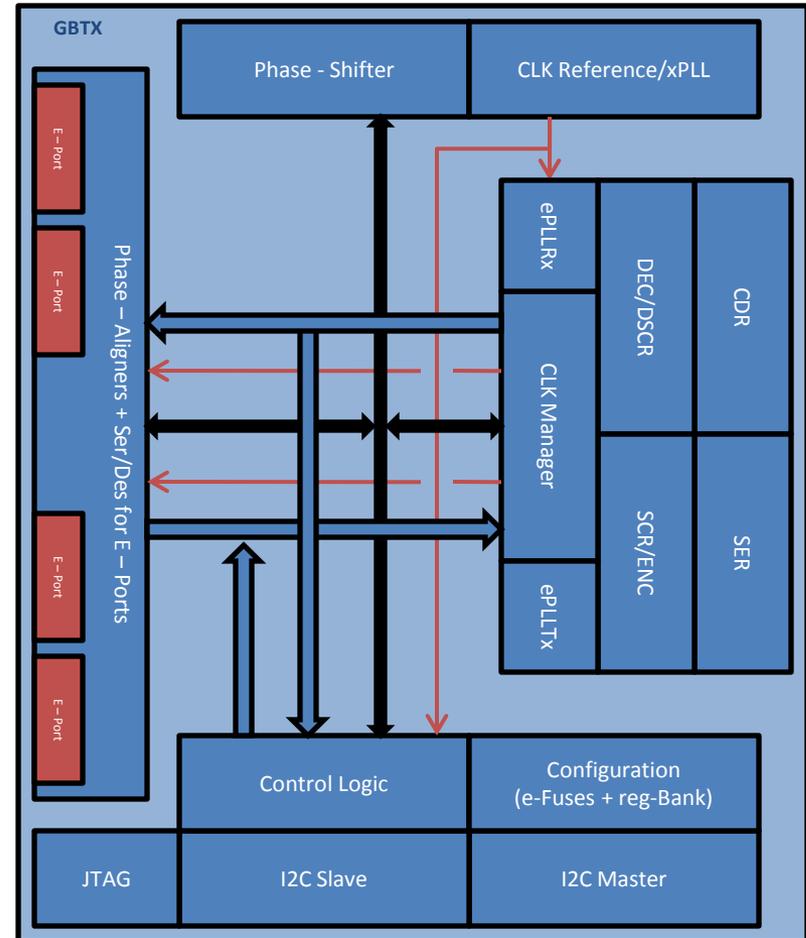
- The GBTX supports three frame types:
 - **“GBT” Frame**
 - **“Wide Bus” Frame**
 - **“8B/10B” Frame**
- **“GBT” Mode**
 - User bandwidth: 3.28 Gb/s
 - Up/down-links
- **“Wide Bus” and “8B/10B” frames are only supported for the uplink**
 - The downlink always uses the **“GBT” frame**.
- **“8B/10B” Mode**
 - Downlink data 8B/10B encoded
 - No FEC
 - User bandwidth: 3.52 Gb/s
- **“Wide Bus” Mode:**
 - Uplink data scrambled
 - No FEC
 - User bandwidth: 4.48 Gb/s



GBTX Functionality (1/4)

e-Links

- 40 bi-directional e-Links
 - Up to 40 @ 80 Mb/s
 - Up to 20 @ 160 Mb/s
 - Up to 10 @ 320 Mb/s
- e-Port data rate can be set independently for:
 - each group
 - Input / output ports
- 1 bi-directional e-Link:
 - 80 Mb/s
- 40 e-Link clocks (fixed phase) programmable in frequency:
 - 40/80/160/320 MHz (per group)
 - *(independently of the bit rate)*
- Automatic, semi-automatic or user controlled phase alignment of the incoming serial data embedded in the e-Ports
 - Automatic alignment
 - Tracks temperature and voltage variations
 - Transparent to the user
 - Works on any type of data:
 - DC balanced / un-balanced
 - A few “occasional” transition enough to ensure correct operation



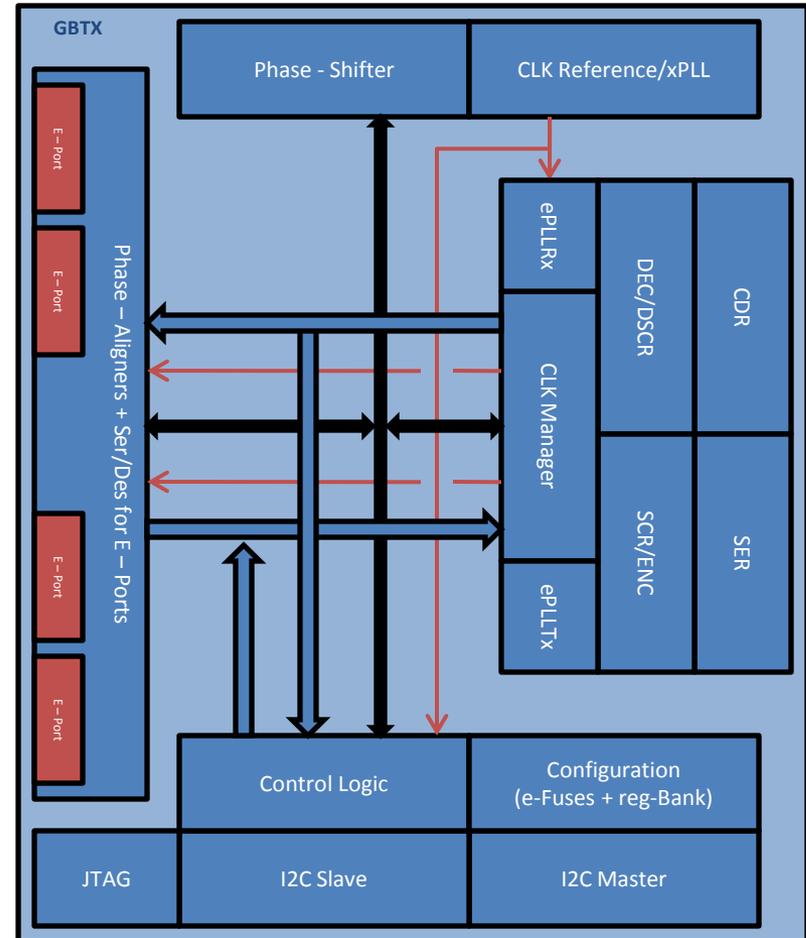
GBTX Functionality (2/4)

e-Links Special cases

- 8B/10B mode:
 - 44 input (max @ 80 Mb/s)
 - 36 output (max @ 80 Mb/s)
 - (Four outputs reused as inputs)
- Wide-Bus mode:
 - 56 input (max @ 80 Mb/s)
 - 24 output (max @ 80 Mb/s)
 - (16 outputs reused as inputs)

e-Links electrical characteristics

- Drivers:
 - SLVS signaling
- Receivers:
 - SLVS/LVDS signaling



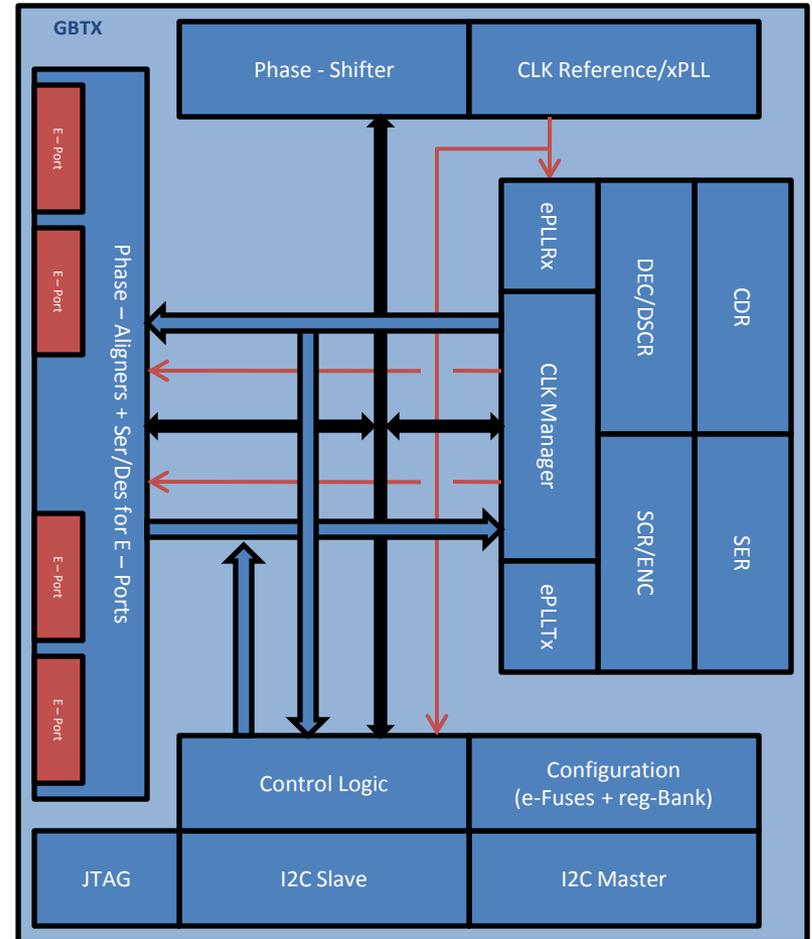
GBTX Functionality (3/4)

Phase-Shifter

- 8 independent clocks
- Programmable in frequency:
 - 40 / 80 / 160 / 320 MHz
- Programmable in phase:
 - 0 to 360°
 - Phase resolution: 50 ps
 - (for all frequencies)
- Clock driver electrical levels:
 - SLVS

Reference clock:

- On package crystal
- Built-in crystal oscillator
- Built-in VCXO based PLL (xPLL)
- External reference can be used as well



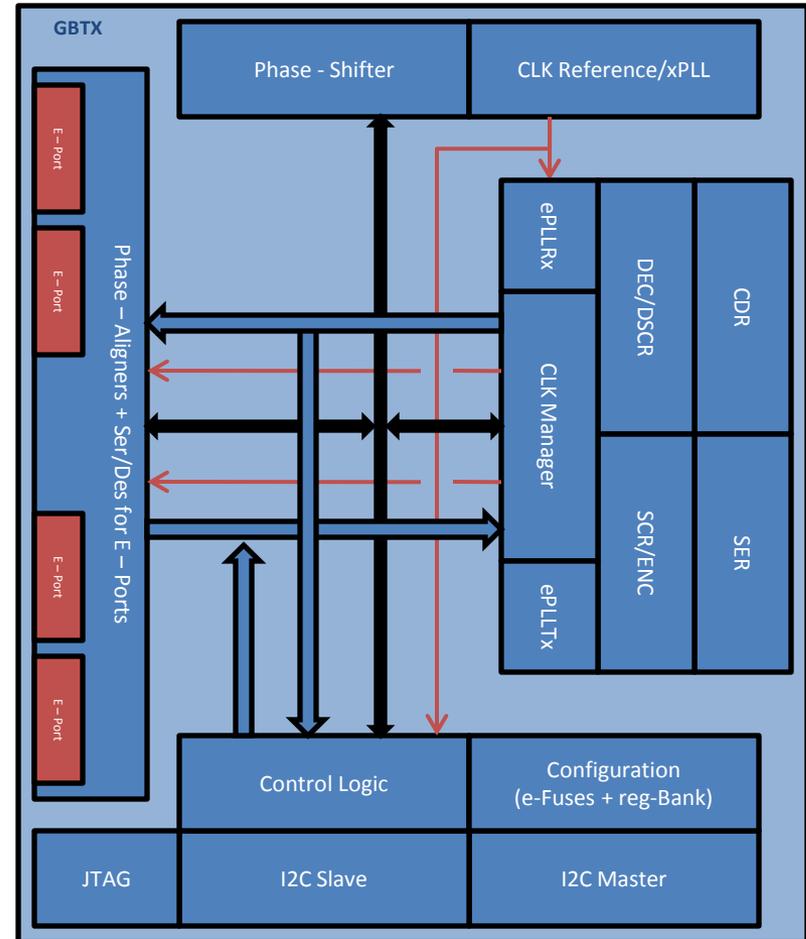
GBTX Functionality (4/4)

Chip Control

- e-Fuse register bank for burn in configuration
 - Standalone operation
 - Ready at power up
- Dynamic configuration and control
 - I2C Slave interface
 - IC control channel through the optical link
- Watchdog circuit for chip operation supervision.

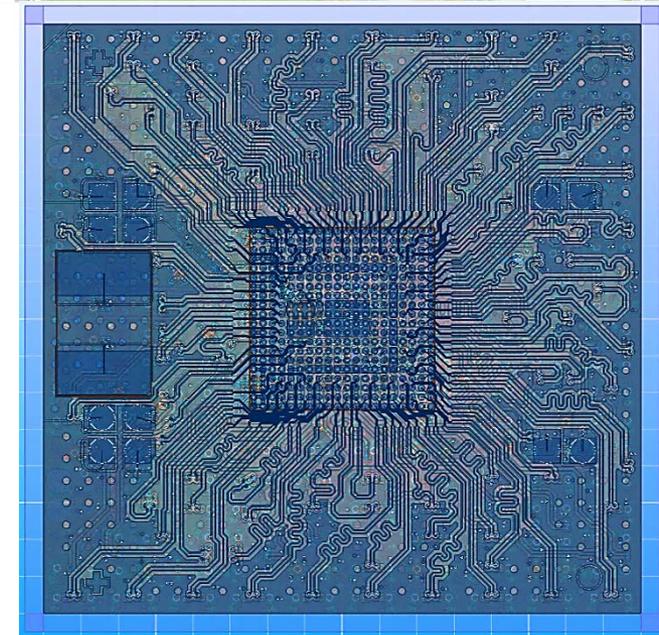
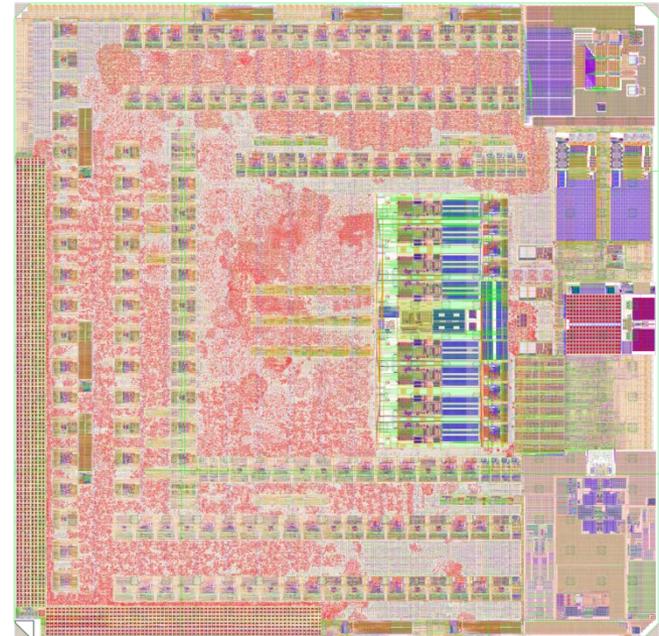
GBLD Control

- GBLD dedicated I2C master interface
 - Copies configuration burned in in the GBLD into the GBLD at start-up
 - Allows to program the GBLD either through the IC channel or through the I2C slave port



GBTX Status

- GBTX submitted for fabrication on the 6th of August 2012
- Prototypes:
 - 120 ASICs (bare die) available since December 2012
 - First packaged chips available May 2013
 - Long design/production cycle!
 - Due to a manufacturing error the package presented a short-circuit between the power and ground planes
 - This caused the loss of 60 die and testing delays
 - “Preliminary testing” could nonetheless be done by drilling the short-circuit in a few packages at the loss of a few connections!
 - Fully functional packaged chips were finally delivered September 2013



GBTX Testing Status

Function	Status	Comment
SER	Done	Tested up to 5.4 Gb/s
CDR	Done	Tested up to 5.4 Gb/s
e-Port Tx	Done	
e-Port Rx	Done	
e-Port Phase Aligner	Done	
Phase-Shifter	Done	
xPLL	Done	Functional but VCXO "gain" must be increased for reliable start when in the PLL mode
e-Fuses	Done	
I2C Master	Done	
I2C Slave	Done	
IC control channel	TBD	
JTAG	TBD	

GBTX Future

- Q4 – 2013
 - Two SEU test runs: October / November
 - Total dose irradiation tests: December
 - Chip characterization: October – December
 - Samples available for prototyping: December
 - Only small quantities available
 - (Remember that we have lost a substantial fraction due to the packaging problem)
- Q1 – 2014
 - Depending on the SEU test results small changes might be required to improve the robustness of the circuit
 - Although the circuit is fully functional a “a few small corners need to be rounded” to make it “plug-and-play” for the users
- Q2 – 2014
 - Split Engineering Run to produce in quantities:
 - GBTX
 - GBTIA
 - GBLD V4/V5
- Q3 – 2014
 - Chips available from the foundry
 - ASIC Packaging
- Q4 – 2014
 - ASIC production testing
 - First production ASICs distributed to the users

GBT-SCA Status

- Analog Circuitry
 - ADC block
 - Design development outsourced to an IP vendor. Design is based on the DCU ADC architecture.
 - Integration work of the IP block is on going.
- DAC
 - Building block borrowed from the MEDIPIX-3 project.
 - Integration work is on going.
- Digital Circuitry
 - RTL code extensively redesigned during last year. Level of completeness 95%
 - Development of a test bench based on System Verilog
 - Development of a hardware test benched based on an FPGA development board.
- ePort (with HDLC transmission protocol)
 - Level of completeness 100%
 - Functionality checks are O.K. and code is synthesizable
- Chip Assembly and prototype submission
 - Floor planning, Place & Route work is on going.
 - Target tape out date:
 - MOSIS MPW run in November 2013

GBT Building Blocks (IP) Status

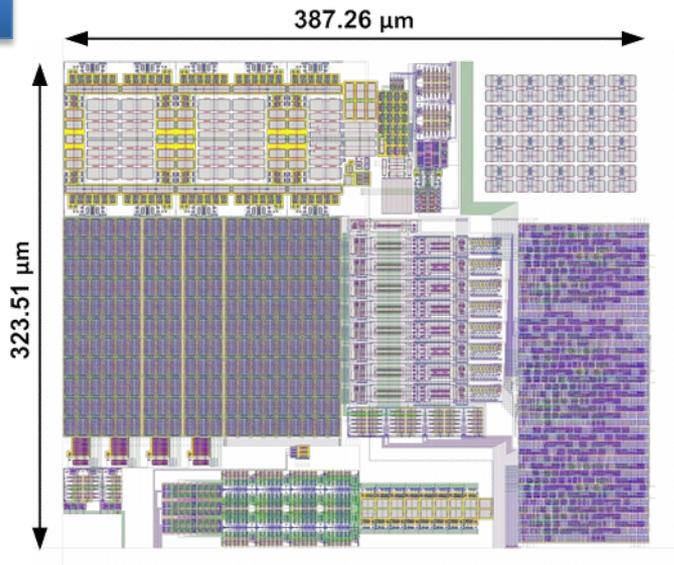
Available “IP” to facilitate the implementation of e-Link transceivers in the frontend ASICs:

- SLVS Receiver
 - Wire-bond, DM metal stack
 - C4, LM metal stack
- SLVS Driver
 - Wire-bond, DM metal stack
 - C4, LM metal stack
- SLVS Bi-directional
 - C4, LM metal stack
- HDLC transceiver
 - Synthesizable Verilog
- 7B/8B CODEC
 - Synthesizable Verilog

- ePLL-FM
 - Frequency Multiplier PLL
 - Radiation Hard
 - 130 nm CMOS technology with the DM metal stack (3-2-3).
 - Input frequencies: 40/80/160 MHz
 - Output frequencies: 160/320 MHz regardless the input frequency
 - Programmable phase of the output clocks with a resolution of 11.25° for the 160 MHz clock and 22.5° for the 320 MHz clock
 - Programmable charge pump current, loop filter resistance and capacitance to optimize the loop dynamics
 - Supply voltage: 1.2 V - 1.5 V
 - Nominal power consumption: 20 mW @ 1.2 V - 30 mW @ 1.5 V
 - Operating temperature range: -30°C to 100°C

- ePLL-CDR (currently under testing)
 - Data rate: 40/80/160/320 Mbit/s
 - Output clocks: data clock + 40/80/160/320 MHz with programmable phase
 - Internal or external calibration of the VCO frequency
 - Possibility to use it as a frequency multiplier PLL without applying input data
 - Programmable charge pump current, loop filter resistance and capacitance to optimize the loop dynamics
 - Supply voltage: 1.2 V - 1.5 V
 - Operating temperature range: -30°C to 100°C
 - Prototype fabrication: May 2013

ePLL- FM



GBT – FPGA Status

- **Aim:**
 - Implement the GBT serial link in all its flavours as an IP core for most of the current FPGAs used on Back-End boards for upgrades
 - Propose an emulation of the E-links for Front-End chip emulation on FPGA
- **On-going firmware updates**
 - Serial link encoding schemes
 - Reed-Solomon (used in GBT frame operation mode),
 - 8b/10b (using hardIP if possible to reduce resources)
 - Wide-bus
 - Fixed latency version
 - E-links modes
 - GBT modes x2, x4 and x8
 - Wide bus mode
 - 8b/10b mode
 - IC channel protocol (not yet started)
- **Available or targeted FPGA**
 - **Altera:**
 - Stratix II and IV (tested with the GBT-SerDes ASIC)
 - Cyclone V GT (tested with the real GBTx ASIC)
 - Stratix V (to be done)
 - **Xilinx:**
 - Virtex 5 and 6 (tested with the GBT-SerDes ASIC)
 - Kintex 7 (on-going)
 - Virtex 7 (on-going)
- **Available or targeted Reference designs**
 - **Xilinx:**
 - Virtex 5: ML523
 - Virtex 6: ML605 and GLIB
 - Kintex 7: KC705
 - Virtex 7: VC705
 - **Altera:**
 - Stratix II Gx:PCIe evaluation kit
 - Stratix IV: PCIe evaluation kit
 - Cyclone V GT: evaluation kit and GBTx Stand Alone Tester (SAT board)

GLIB board (Virtex 6)



KC705 (Kintex 7)



- **Project Resources**
 - 50% of one Fellow since this summer
 - More than 70 users registered
 - A sharepoint site: <https://espace.cern.ch/GBT-Project/GBT-FPGA/default.aspx>
- **A SVN repository:**
 - https://svnweb.cern.ch/cern/wsvn/phese/be/gbt_fpga
- **Contact us:**
 - Sophie.baron@cern.ch
 - manoel.barros.marin@cern.ch