Powering Large FPGAs
a designer nightmare

Altera case

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Outline

- Problem scope
- How to estimate power consumption
- Important factors
- Examples and limits
Power supplies in large FPGAs

Example of Stratix V GX

- SGXEA7 : 600 kLE, 48 x 10Gbps serial links, 1932 pins
- Multilevel powering:
  - 3V, 2.5V, 1.5V, 1.0V, 0.85V
- Up to 15 types
- Up to 52 differentiated power sources
- Some of them can be merged however
  - Under specific conditions
    - (loss of some functionalities: Ex: low speed, no AEQ, no EyeQ)
- Requires low noise powering
  - ~ <1 % of line regulation

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Additional constraints

Preventing large inrush current

- Requires sequencing of power rails supply
How to estimate power consumption?

**Ideal case (that never happens):**
- Your HDL code is completely known and you just start designing your board
  - Altera provides *PowerPlay Power Analyzer* (post fitting estimation)

**Normal case:**
- You start designing your board …
- But have only an estimation of what the size of the final firmware will be
  - Altera provides *Powerplay Early Power Estimator*
Estimation tool
Important factors

**FPGA:**
- Kind of I/Os used
- Percentage of core logic used
- Operating frequency
- Toggle rate

► You cannot maximize all of them!
- Static power: logic cells current leaks

**Layout**
- Powering takes room (a lot!)

**Cooling**
- The FPGA must not overpass a maximum temperature
  ➔ Usually 85°C on die
An example

**LHCb readout configuration:**
- 40 serial links (28 at 4.8 Gbits/s, 12 at 10 Gbits/s)
- 128 bits DDR3 interface at 800 MHz
- 100 % of logic used

![Pie chart showing resource usage](image-url)
Frequency and toggle rate limits

Power consumption vs frequency for several toggle rates
Conditions: 100% of logic cells – Ta = 35°C – Air flow: 3m/s
Heatsink cooling: 0.86°C/W – I Core: 30A
Locic cells limits

Power consumption vs locic cell occupancy for several frequencies

Conditions:
- Toggle rate: 30%  
- Ta = 35°C  
- Air flow: 3m/s  
- Heatsink cooling: 0.86°C/W
Power tree example

(*x,xV)
STRATIX V - ES

SEQ#x : Power supply Sequenceur 1 to 5

Pour les besoins du routage

3.3V
(*)3.6V
FLASH
Conclusion

Powerful tools for estimating Power consumption provided by Altera

But … very difficult exercise: powering a large FPGA is quite tricky

Maximizing all resources, speed, occupancy and toggle rate may lead to unfeasible solution

The more things you know about final VHDL code the better

Lot of noise in DCDC converters, lot of losses in LDOs: find the best compromise

The more Amps you inject, the more difficult decoupling will be … yet another story