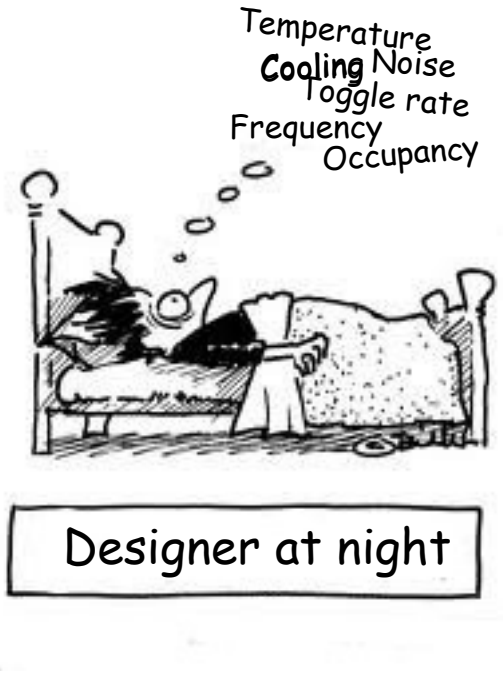
Powering Large FPGAs
a designer nightmare

Altera case



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Outline

- Problem scope
- How to estimate power consumption
- Important factors
- Examples and limits

Power supplies in large FPGAs

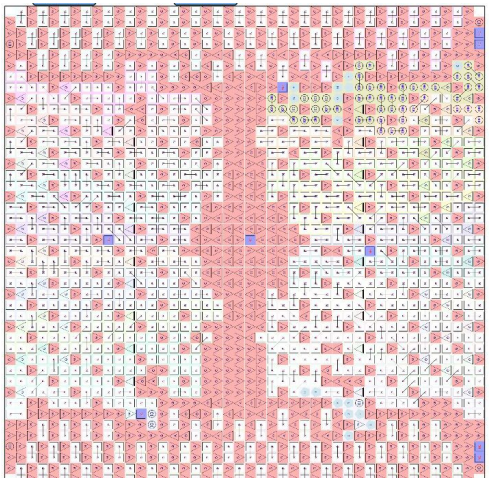
Example of Stratix V GX

- SGXEA7 : 600 kLE,
  48 x 10Gbps serial links
  1932 pins

- Multilevel powering :
  - 3V, 2.5V, 1.5V, 1.0V, 0.85V
- Up to 15 types
- Up to 52 differenciated power sources
- Some of them can be merged however
  - Under specific conditions

    (loss of some functionalities :
    Ex : low speed, no AEQ, no EyeQ)
- Requires low noise powering

  ~ <1 % of line regulation

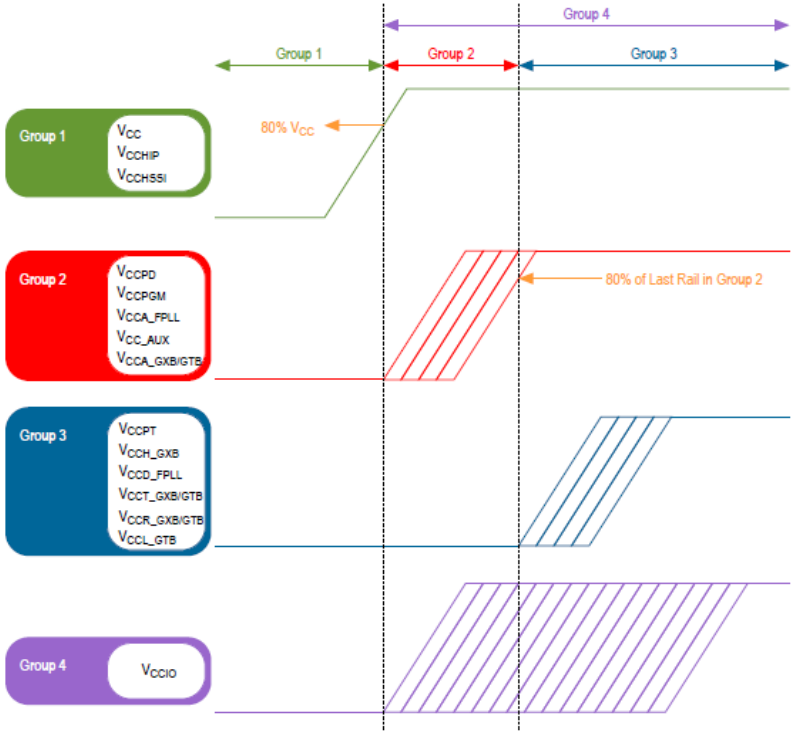


Power	Use
VCC	Core logic
VCCHIP	PCIe Hardware IPs
VCCHSSI	Physical Coding Sublayer
VCCR_GXB	GX receivers
VCCT_GXB	GX transmitters
VCCIO	I/Os
VCCPD	I/Os predrivers
VCCPGM	Configuration pins
VCC_AUX	Auxiliary supply for programmable power technology
VCCA_GXB	GX drivers and CDR
VCCA_FPLL	PLL analog power
VCCPT	Programmable power technology
VCCH_GXB	Block level TX buffers
VCCD_FPLL	PLL digital power
VCCBAT	battery backup

Additional constraints

Preventing large inrush current

- Requires sequencing of power rails supply



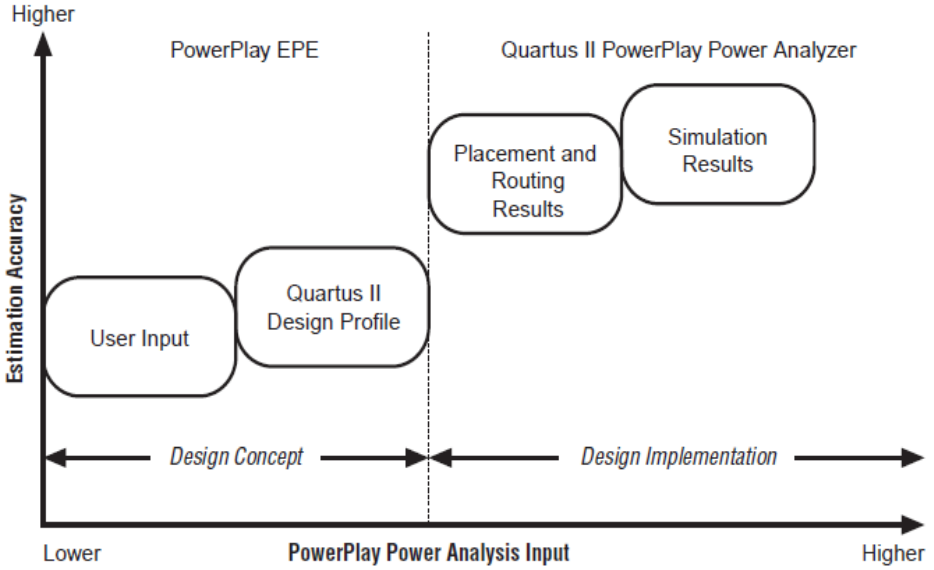
How to estimate power consumption ?

Ideal case (that never happens):

- Your HDL code is completely known and you just start designing your board
  - Altera provides ***PowerPlay*** **Power Analyzer** (post fitting estimation)

Normal case:

- You start designing your board …
- But have only an estimation of what the size of the final firmware will be
  - Altera provides ***Powerplay*** **Early Power Estimator**



Estimation tool

Module	# Combinational ALUTs	# FFs	Clock Freq (MHz)	Toggle %	Average Fanout	Routing	Block	Total
0	4500	0	120	50,0%	3	0,034	0,039	0,072
1	9607	0	120	50,0%	4	0,099	0,082	0,182
2	100000	0	120	50,0%	2	0,396	0,857	1,253
3	384	0	120	50,0%	4	0,004	0,003	0,007
4	245	0	120	50,0%	2	0,001	0,002	0,003
5	2	0	120	50,0%	1	0,000	0,000	0,000
						0,000	0,000	0,000
						0,026	0,030	0,056
						0,000	0,000	0,000
						0,010	0,064	0,074
						0,024	0,051	0,075
						0,639	0,729	1,367
						0,000	0,000	0,000
						0,000	0,000	0,000
						10,791	3,144	13,935
						0,000	0,000	0,000
						0,000	0,000	0,000
						0,000	0,000	0,000
						0,020	0,010	0,030
						0,004	0,001	0,005
						0,030	0,009	0,039
						0,016	0,003	0,020

ALTERA

Visit the Online Power Management Resource Center

Stratix® III, Stratix® IV, Stratix® V, HardCopy® III, HardCopy® IV

V11.1 B37 MS 93-2007

Comments: Release Notes

Input Parameters

Family	Stratix V
Device	5SGXEA7N
Package	F45
Temperature Grade	Commercial
Power Characteristics	Typical
V_{CCL} Voltage (V)	N/A

User Entered Tj / Auto Computed Tj

Ambient Temp, T_A (°C)	35

Custom Theta JA / Estimated Theta JA

Heat Sink	N/A
Airflow	N/A
Custom θ_{JA}(°C/W)	0,86
Board Thermal Model	N/A

Thermal Power (W)

Logic	17,785
RAM	1,821
DSP	0,000
I/O	5,923
HSDI	0,008
PLL	0,408
Clock	1,139
XCVR	4,902
PCS and HIP	1,672
P_{static}	2,966
TOTAL	36,624
HardCopy	N/A

Thermal Analysis

Junction Temp, T_J (°C)	72,5
θ_{JA} Junction-Ambient	0,86
Maximum Allowed T_A(°C)	46,4

Details

Power Supply Current (A)

I_{CCL} (N/A)	N/A
I_{CC} (0.85V)	26,730
I_{CCD_FPLL} (1.50V)	0,145
I_{CCPT} (1.50V)	0,239
I_{CCA_FPLL} (2.50V)	0,109
ICCPD	1,385
ICCIO	2,400
ICCXCVR	4,822
I_{CCH8I} (0.85V)	2,045
I_{CCHIP} (0.85V)	0,178

Click buttons for details.

Main | Logic | RAM | DSP | IO | PLL | Clock | HSDI | XCVR | IP | Report | Version

Important factors

FPGA :

- Kind of I/Os used
- Percentage of core logic used
- Operating frequency
- Toggle rate

- *You cannot maximize all of them !*
  - Static power : logic cells current leaks

Layout

- Powering takes room (a lot !)

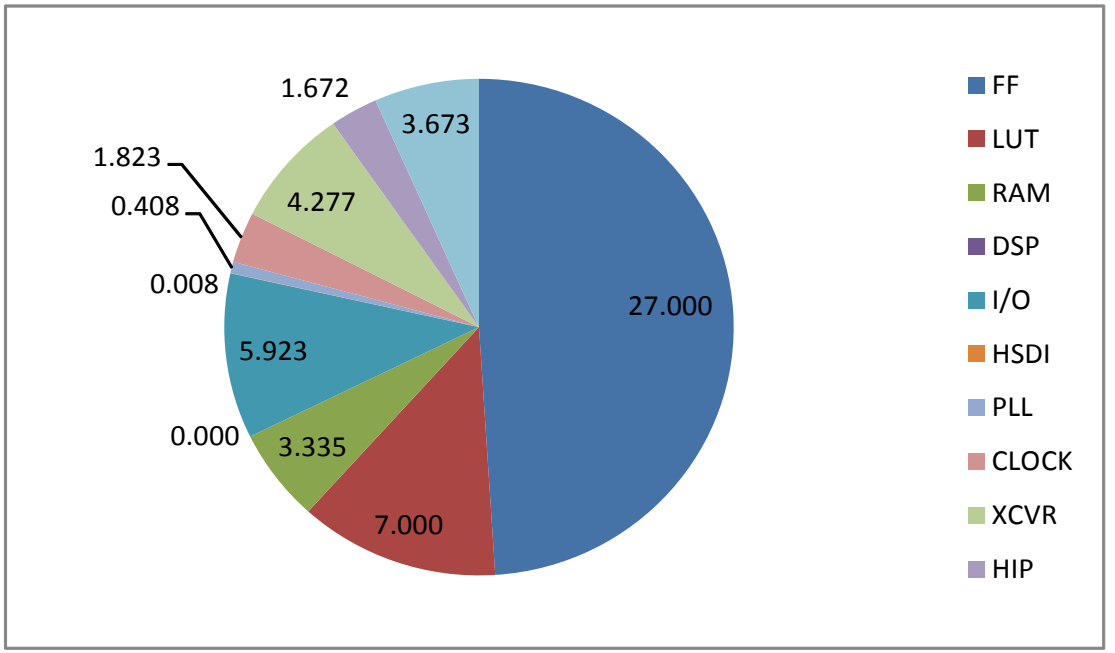
Cooling

- The FPGA must not overpass a maximum temperature
  - Usually 85°C on die

An example

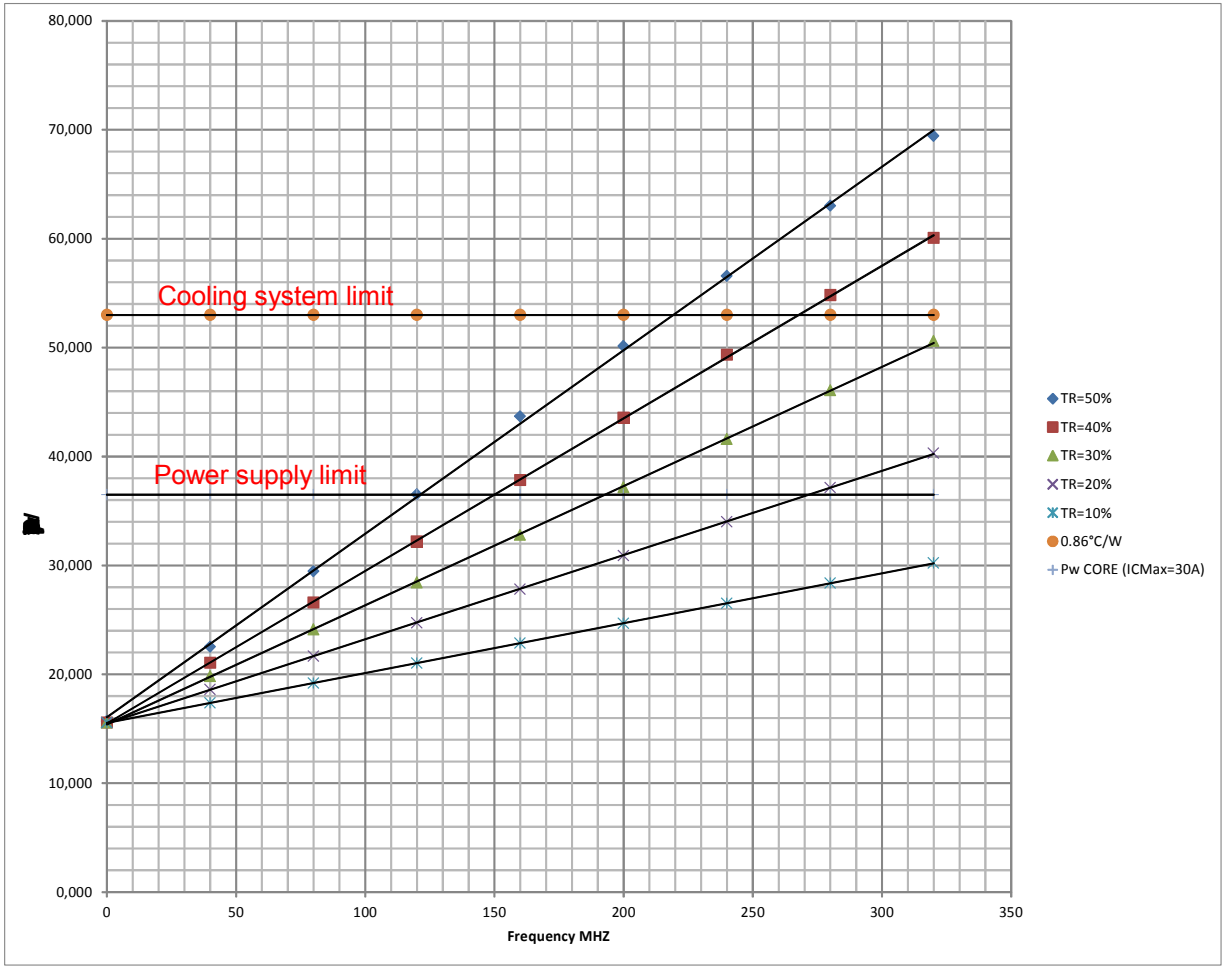
LHCb readout configuration:

- 40 serial links (28 at 4.8 Gbits/s, 12 at 10 Gbits/s)
- 128 bits DDR3 interface at 800 MHz
- 100 % of logic used



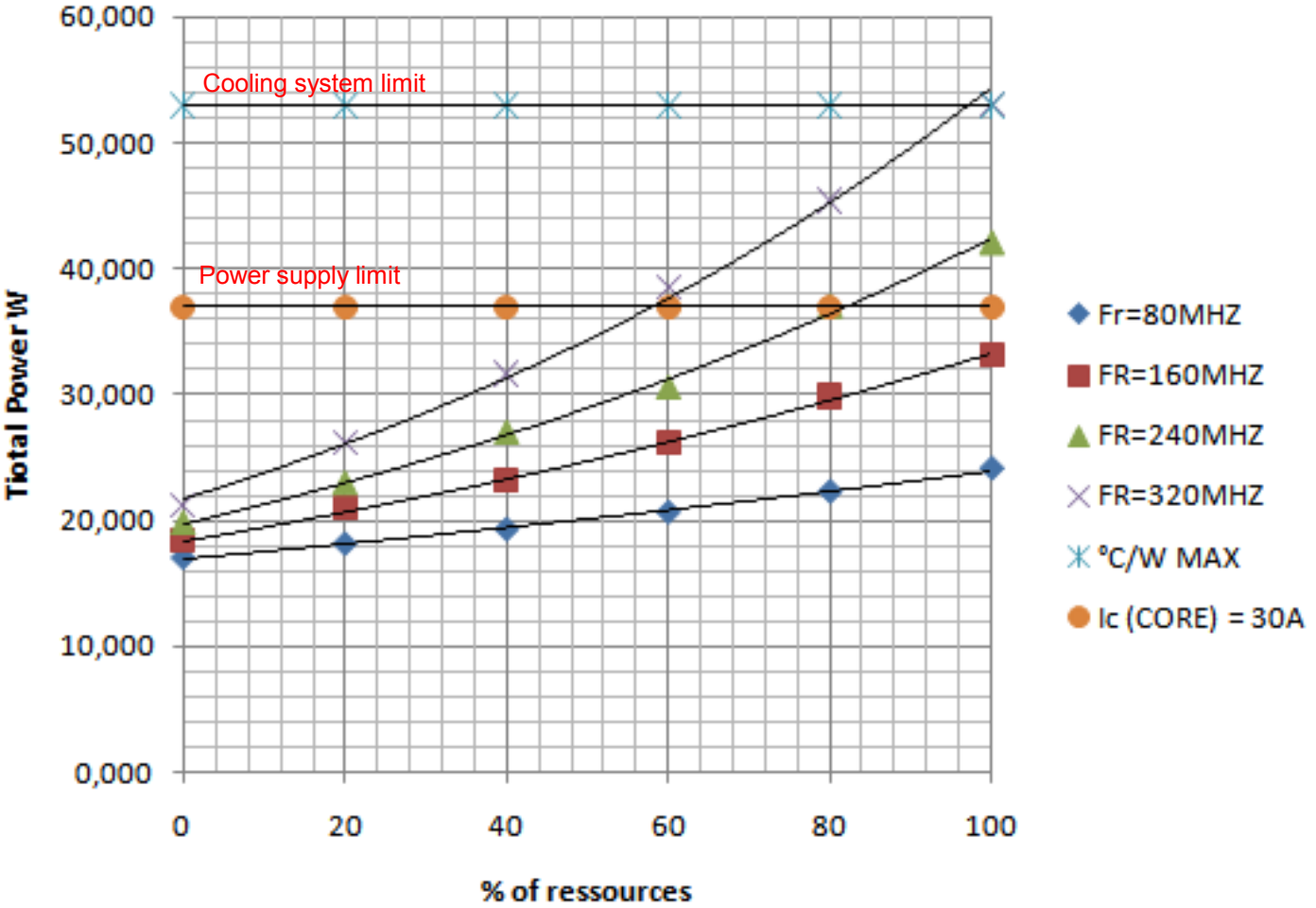
Toggle 50% - Fr=240MHZ
100% of ressources – T°=25

Frequency and toggle rate limits



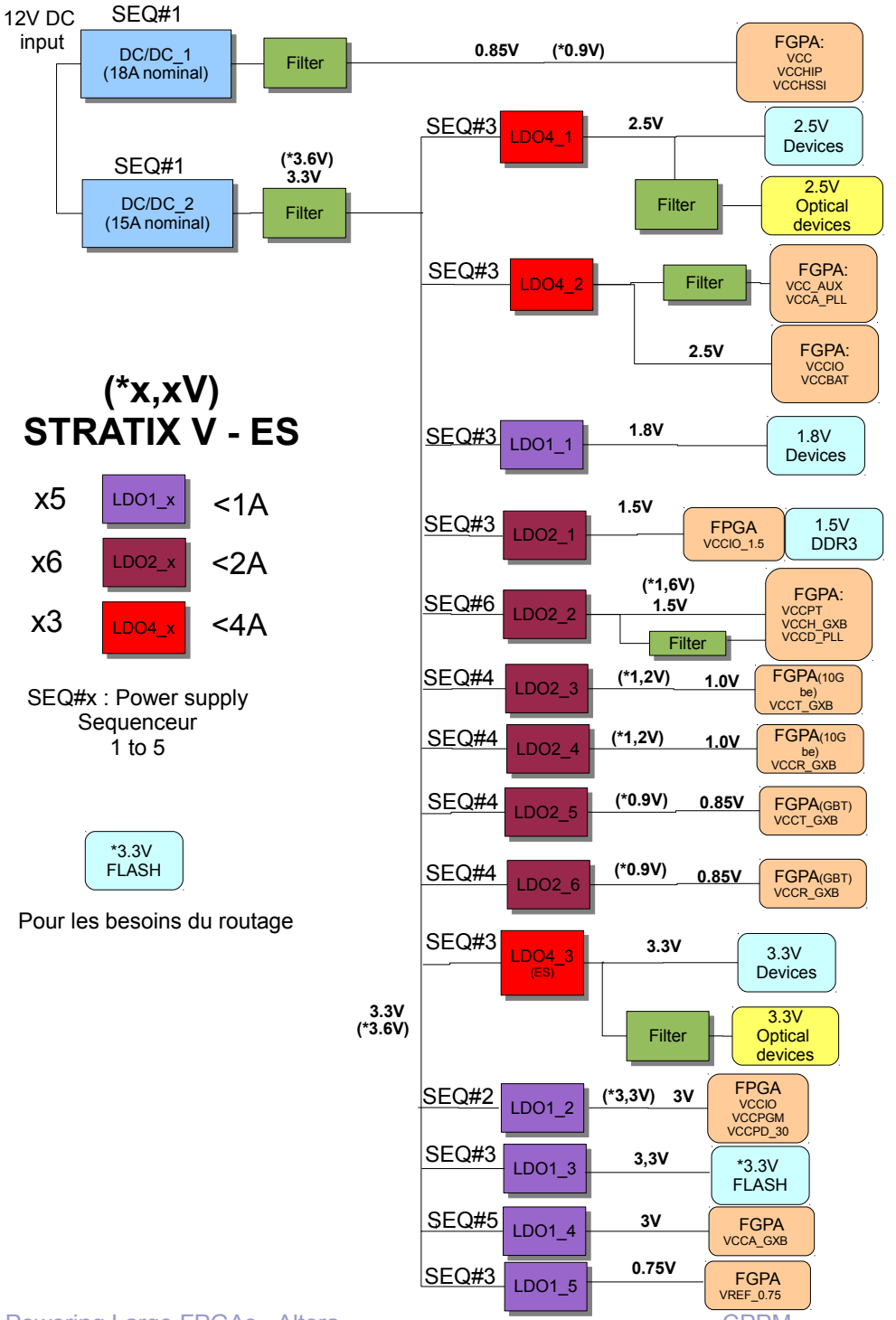
Power consumption vs frequency for several toggle rates
Conditions : 100 % ol logic cells – Ta = 35°C – Air flow : 3m/s
Heatsink cooling : 0.86°C/W – I Core : 30A

Locic cells limits



Power consumption vs locic cell occupancy for several frequencies
Conditions : Toggle rate : 30 % – Ta = 35°C – Air flow : 3m/s
Heatsink cooling : 0.86°C/W

Power tree example



Conclusion

Powerful tools for estimating Power consumption provided by Altera

But … very difficult exercize: powering a large FPGA is quite tricky

Maximizing all ressources, speed, occupancy and toggle rate may lead to unfeasible solution

The more things you know about final VHDL code the better

Lot of noise in DCDC converters, lot of losses in LDOs : find the best compromize

The more Amps you inject, the more difficult decoupling will be
… yet another story