Contribution ID: **108** Type: **Poster**

Prototype pixel detector in the SOI technology

Wednesday, 25 September 2013 16:41 (1 minute)

We present the prototype pixel detector built in the Silicon on Insulator (SOI) technology. The sensor matrix contains 1024 integrating type cells, read continuously out as a serial analog signal. The pixels are protected from the back-gate effect by the Buried P-Well implantations. Measured ENC value was found to be 130 electrons at 100us integration time. An on-chip prototype SAR ADC and a precise voltage reference and temperature sensors have been also included in the design

Summary

Based on a well established commercial process, the SOI pixel detectors offer a freedom in tight integration of the particle sensors and readout electronics. The weakly doped areas under the Buried Oxide layer (BOX), called Buried P (N) Well layers (BPW, BPN), have proved to successfully suppress the Back-gate effect, originating from the detector bias. Although almost sub-micron, the radiation hardness of the technology is not yet satisfactory; an improvement is expected by means of the BPW, BPN combinations and newly developed Double SiO2 process extension, where the BOX contains thin layer of a weak conductor, which is supposed to reduce an electric field from the trapped charges.

The new pixel detector with the matrix of 1024 sensors was built in the Double SiO2 technology, with the single BPW type protection. Two kind of pixels, with the same circuit but different layouts have been used in the matrix. The chip was made as an integration type detector, with capability of a continuous readout in the "rolling shutter"mode, where the signals from consecutive pixel rows are transferred out without interrupting the charge acquisition. The chip is driven by the simple set of the reset and clock signals. The upper limit of the clock frequency is 25MHz, what origins in the slew rate of the analog buffers used. For simplicity the same clock was used both for the sensor control and for the readout; the clock frequency determines the integration time. In addition to the pixel sensor system, two standalone blocks of electronics have been put. The first one, the Successive Approximation type (SAR) 10-bit ADC is foreseen to be applied in the pixel readout in next chip iterations. The second one was a precise, thermally stable voltage bandgap reference.

Preliminary measurements with the Am241 source resulted in ENC value around 130 electrons at 100us integration time. Large difference between gain and noise of the pixels with different layouts have been observed. The bandgap source was operational, both as a voltage and temperature reference. The SAR ADC tests so far have not gave satisfactory results, mainly due to the test board parasitic coupling effects; the new test platform is currently under development.

Primary authors: AHMED, Imran (AGH University of Science and Technology (PL)); IDZIK, Marek (AGH University of Science and Technology (PL)); TURALA, Michal (Polish Academy of Sciences (PL)); KAPUSTA, Piotr (Institute of Nuclear Physics PAN, Krakow (PL)); SGLAB, SEBASTIAN (AGH University of Science and Technology (PL))

Presenter: KAPUSTA, Piotr (Institute of Nuclear Physics PAN, Krakow (PL))

Session Classification: Poster