Technology Trends for Customized Analogue and Digital Circuit Manufacturing including Radiation Hardness Requirements

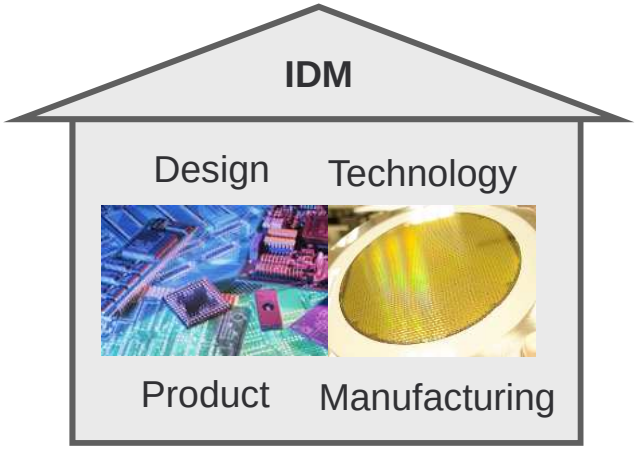
LFoundry

Outline

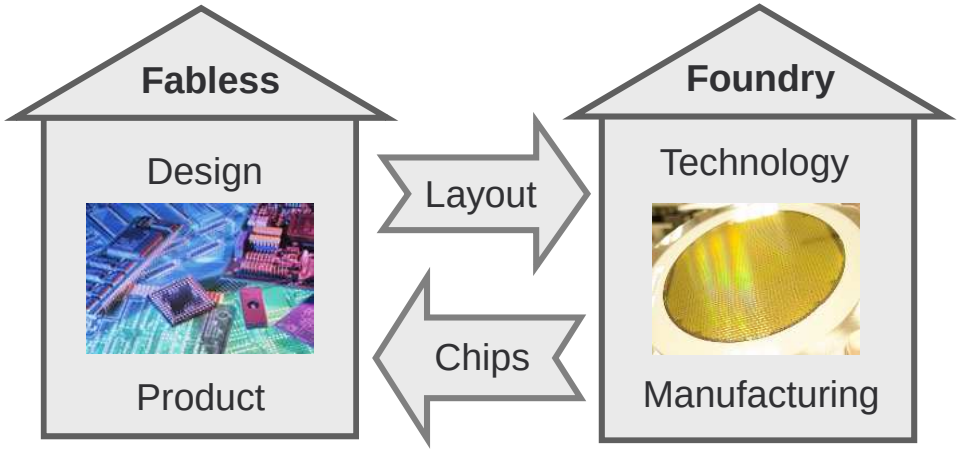
- Foundry Business Model
- Technology trends for More-than-Moore applications
- Semiconductor Devices - Radiation Hardness Requirements & Applications

Foundry / IDM / Fabless Business Model

- Traditional IDM Business

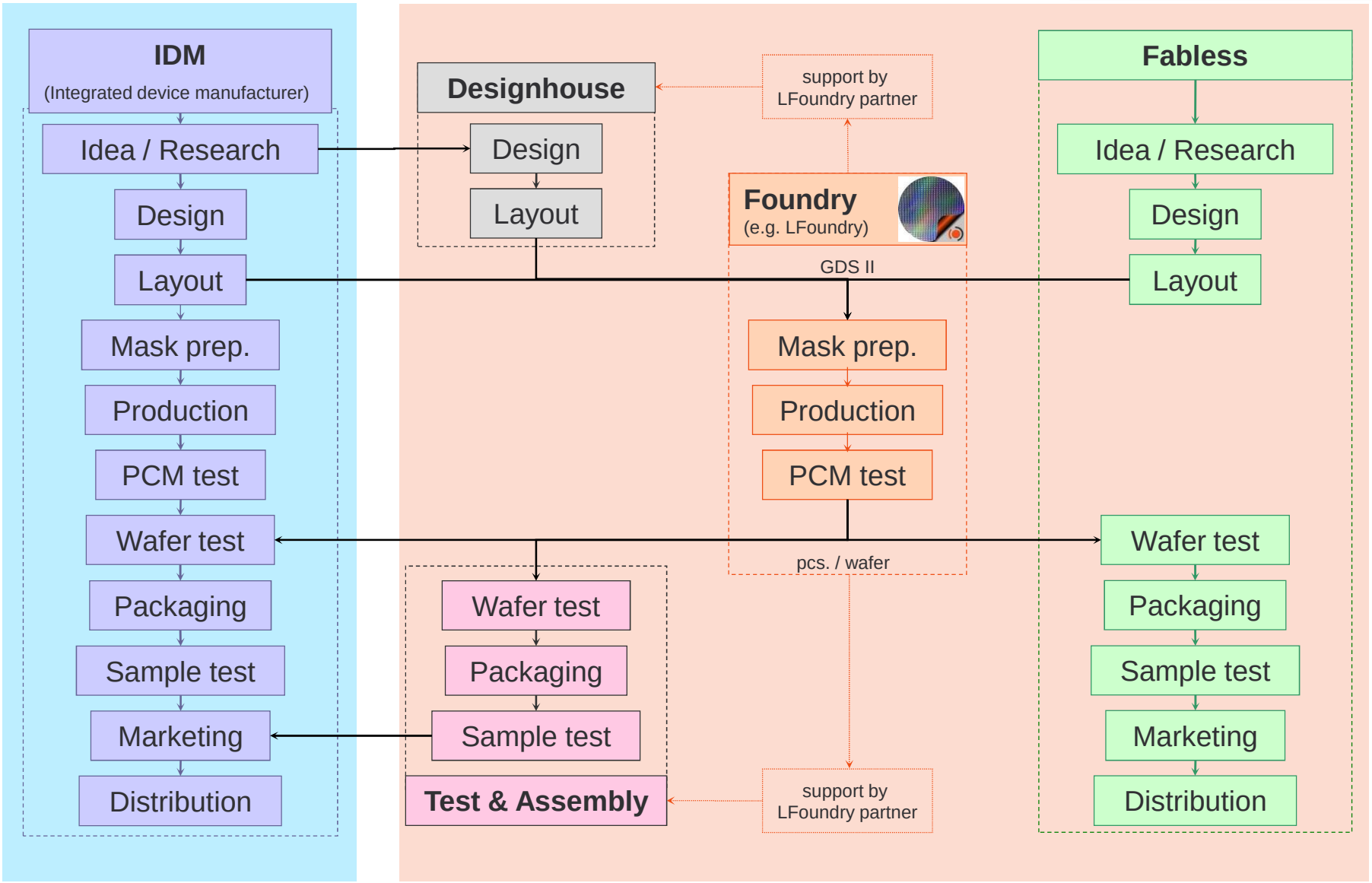


- Traditional Foundry Business



- LIFE (LFoundry integrated Foundry Ecosystem)
  - philosophy: increase the interaction with our customers and make them to our partner

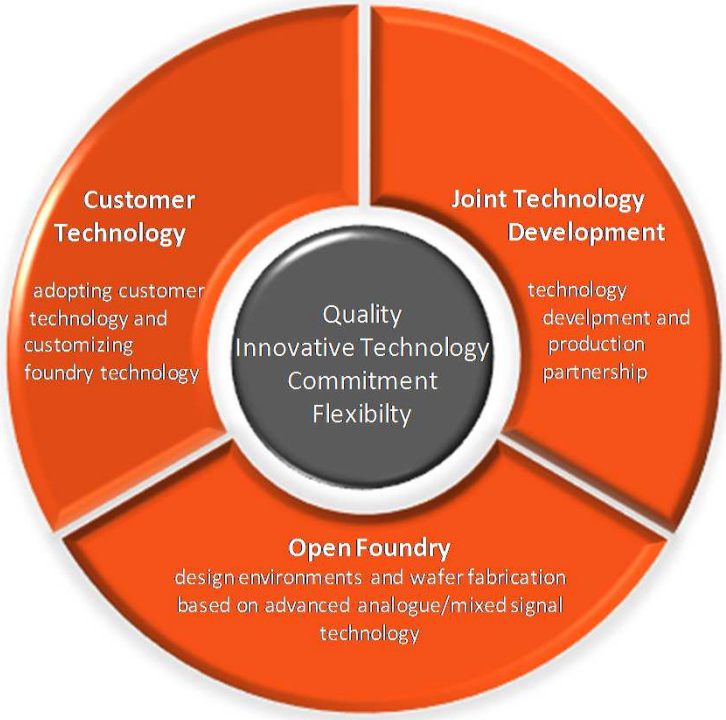
Foundry / IDM / Fabless Business Model



LFoundry Business Model

LFoundry has invented from the beginning an expanded foundry model to support trends in semiconductor device business

- Offering special process platforms & engineering knowhow, enabling partners to setup their integrated technologies:
  CMOS image sensor,
  CMOS-MEMS processes,
  Backside processing,
  Special metallization,
  …



- Supporting product companies in their next developments from the beginning
- Support growth plans of partners
- Utilizing the excellent network to leading institutes

- Support open foundry access through
  - Flexible PDK platform (i-PDK)
  - Continuous mainstream technology enrichment with modules like High Voltage, Opto-technology modules, RF devices , High density flash…
  - Specific qualifications like automotive and security for technologies and manufacturing sites

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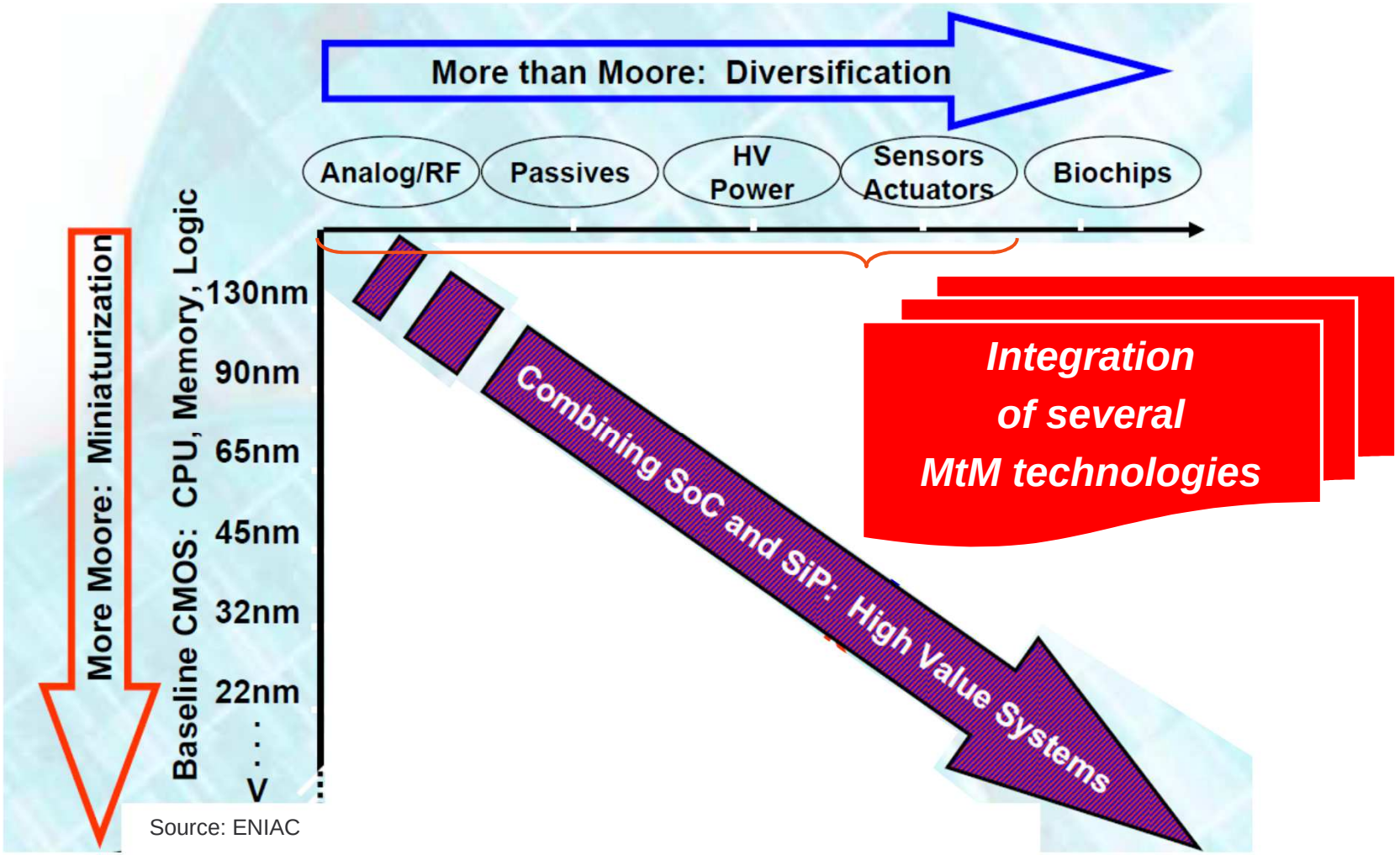
Technology Trends
More-than-Moore → Integration



Source: ENIAC

Integration in the Analog-Mixed-Signal Area

- Standard System on Chip SoC Integration
- Key requisite therefore is a proven, modular iPDK (interoperable Process Design Kit) and a qualified or accessable IP design block portfolio

PDK
Design rules, verified library models,
physical verification,
Reliability qualification, ESD, PCMs

Cell Library
low leak standard library
high speed standard library
elements such as Buffer,
Latches, Flip-Flop, Physical
Delay, Tristate, ...

Memory IP
SRAM (Mobile Semi)
EEPROM (LFoundry)
Flash (SST)
OTP (NSCore)
MTP (NSCore)

Cores
8051 until high end
8b to 32b also as RISC
low leak to high performance

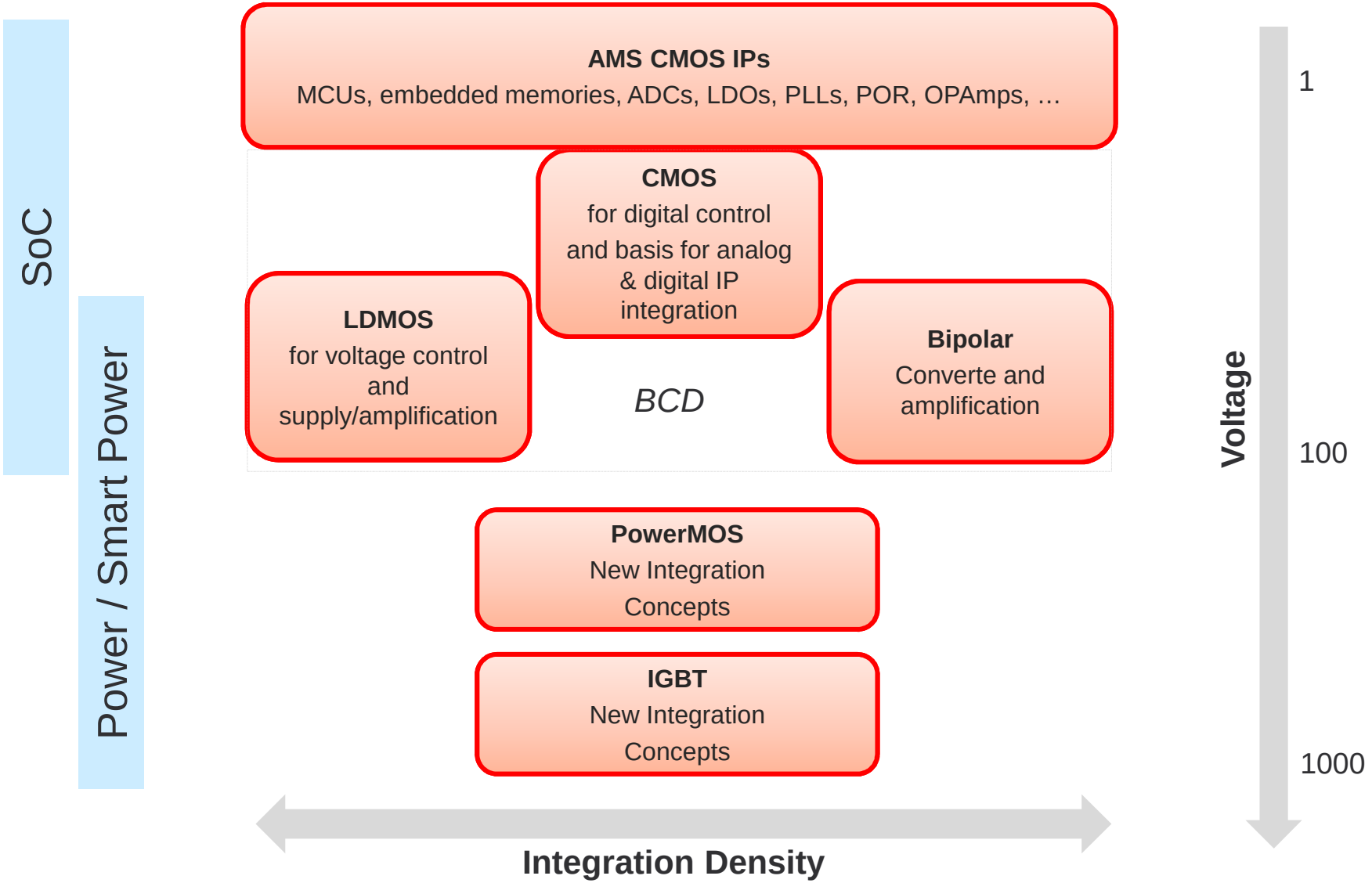
Mixed-signal IPs
ADC, DAC, LDO, PLL, Bandgap,
Bias Generator, Charge Pump,
Oscillator, OP Amps, OTA, POR, ...

Interfaces
GPIO library, Serial,
SPI Interface bus, I2C,
USB, ...

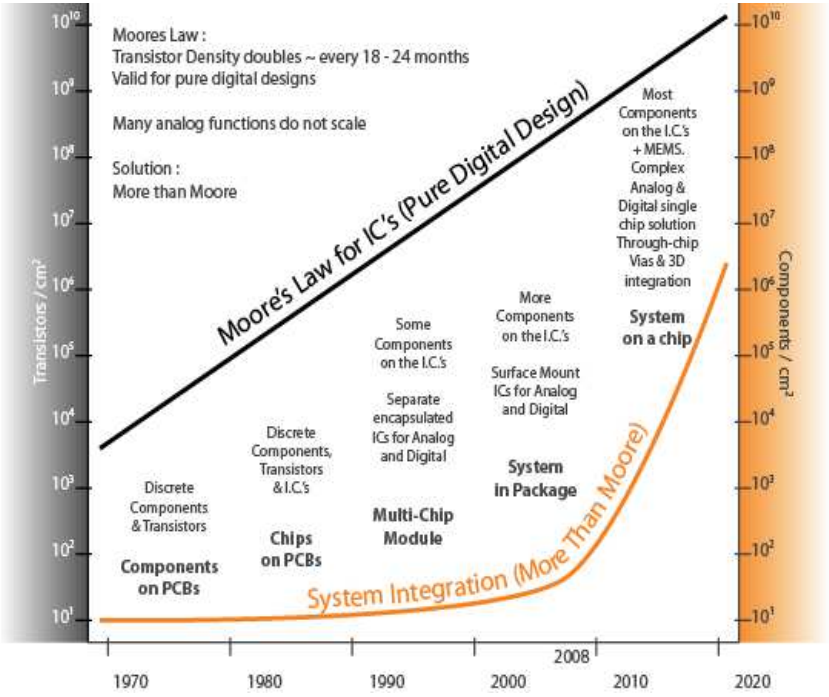
Detectors / Security
temperature sensor, AES/DES, ...

... whatever you need for your SOC, we have it

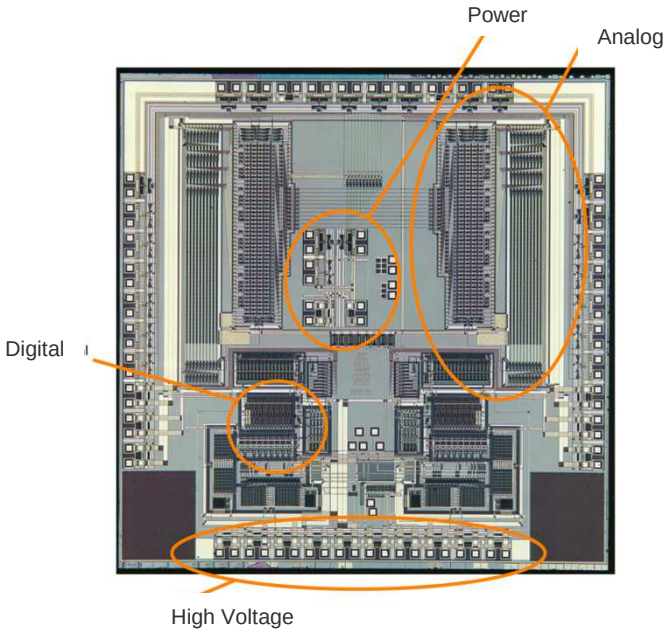
Integration from SOC to Smartpower Area



Integration of New Technology Applications



SoC with different 'IP' blocks, i.e. embedded memories, µController, analog-digital-converter



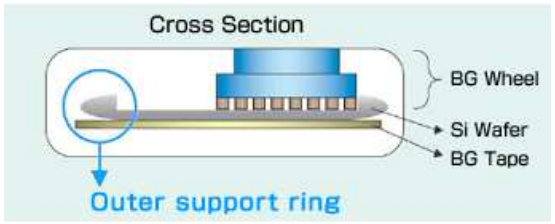
Beyond SoC:
Image Sensor Adv. Techn.
MEMS on CMOS
Backside processing
Thin wafer handling
3D Integration
Through Si Via TSV
Wafer Level Packaging

Wafer Thinning as enabler for various Technology Applications

- i.e. for Advanced Image Sensors, Power Devices, 3D Integration
- Some options to decide
  - Thin wafer w/o carrier
    → handling concepts
    → low cost but barrier ~100µm

LFoundry

  - Taiko process
    → easier handling
    → application limited



www.disco.co.jp

  - Thin wafer with carrier
    → various bonding methods (permanent vs temporary)
    → smallest wafer thickness but highest complexity

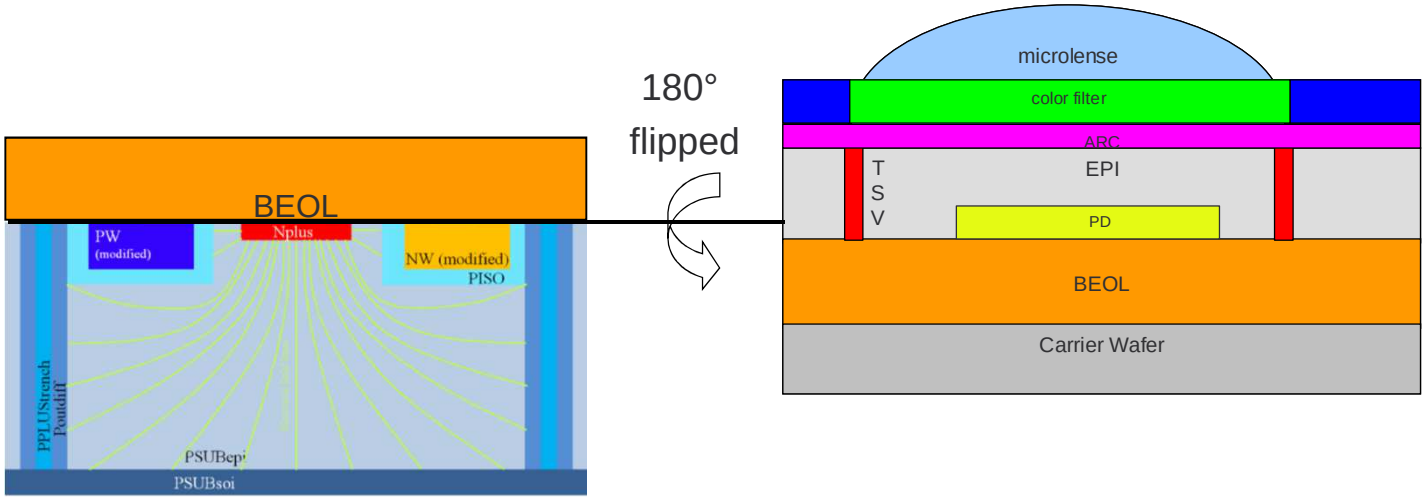
Integration in Advanced Image Sensor Technologies towards 3D

- Next performance level on CMOS imaging: BSI – Backside Illumination:

Parameter	BSI	FSI	Change	Units
Sensitivity (@FD, 3000°K)	1.83	0.74	2.5x increase	V/lux-sec
QE (3000°K)	81	30	2.7x increase	%
Full-well (linear)	16.5	13.0	26% increase	Ke
Dark Current (@ 60°C)	126	116	8% increase	e /pixel
Read noise	12.7	13.1	3% reduction	e
PRNU (@ 50% full-well)	1.85	1.83	unchanged	%
Dynamic Range	62.3	59.9	2.4 dB improvement	dB
Max.SNR	42.2	41.1	1.1 dB improvement	dB

Posted by Tom JOY on December 3, 2008

- Need to implement the following advance integration schemes: Backside processing, Wafer thinning, Through Silicon Via TSV

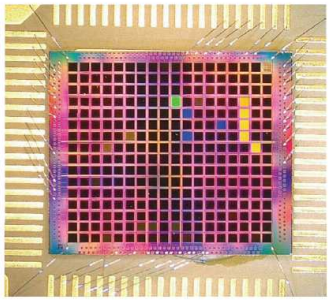


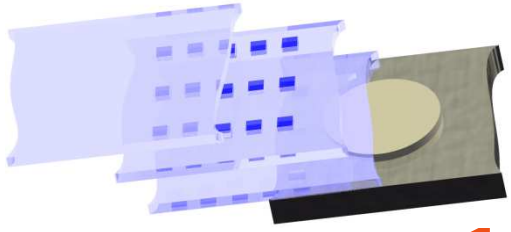
Smart Integration in Advanced Image Sensor Technologies

- Standard Filter for Image Sensors
  - Colour Filter Arrays CFA of type Bayer, RGB, …
- New approaches: smart optical components
  - integrated into CMOS BEOL
  - used for colour and also polarisation filter

Optical Filter integrated into std. CMOS

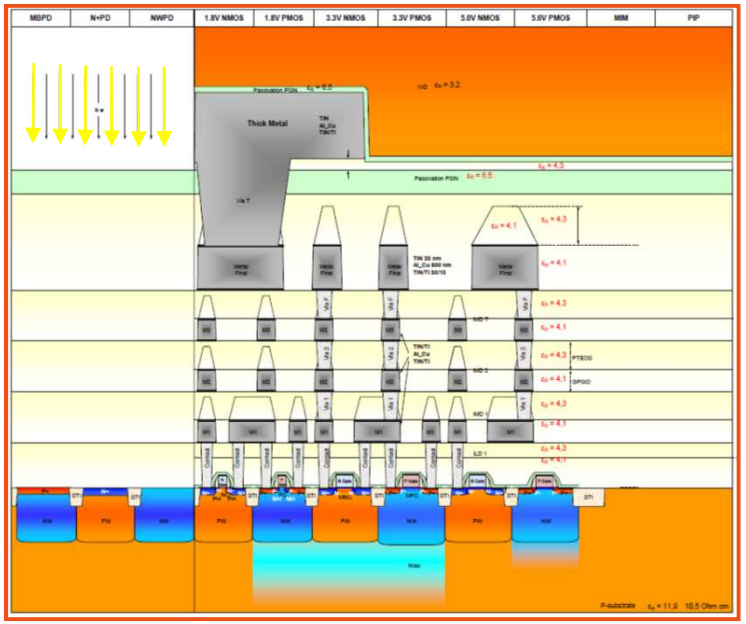
Result *Concept*





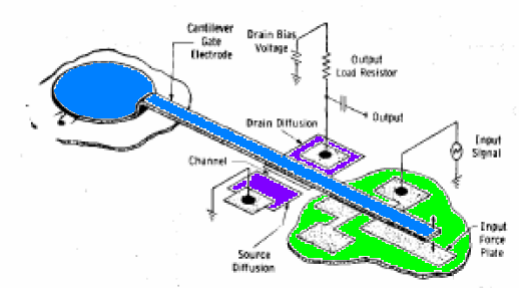
Photodiode building area

Illumination *CMOS*



Smart Integration MEMS into CMOS

- MEMS is not *new*:



In case you were wondering, microsystems have physically been around since the late 1960's. It is generally agreed that the first MEMS device was a gold resonating MOS gate structure. [H.C. Nathanson, et al., The Resonant Gate Transistor, IEEE Trans. Electron Devices, March 1967, vol. 14, no. 3, pp 117-133.]

http://www.ansys.com/industries/mems/mems-what-is.asp

- So, what is all the hype about MEMS for More-than-Moore ?

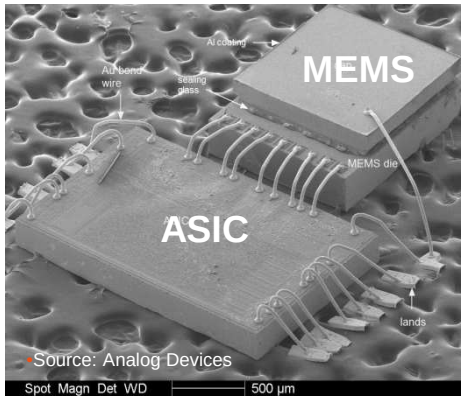
  → it is the miniaturizations and therefore possibility of integration with highend CMOS technologies

Source: Bosch

Smart Integration MEMS into CMOS

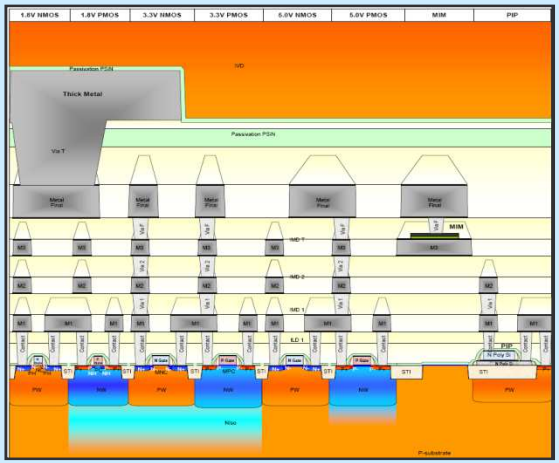
- Goal is integration of CMOS (ASIC) and Sensor (MEMS) into on chip
- Key for SMART is, to utilize advanced CMOS processes (i.e. 150nm) to enable complex circuit designs and then integrate MEMS on top
  - → smaller dimensions
  - → better signal performance & energy efficiency
  - → saving of packaging costs by factor >2

Current Standard

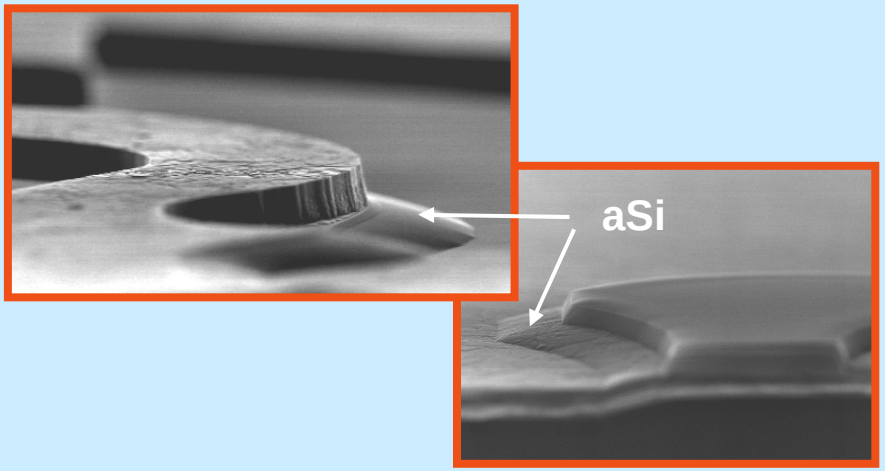


Smart Integration

CMOS



MEMS processes



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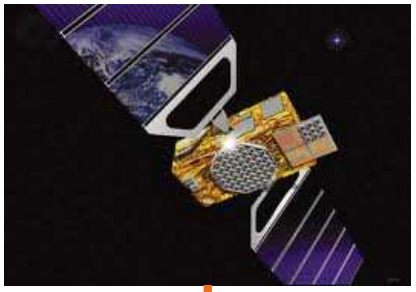
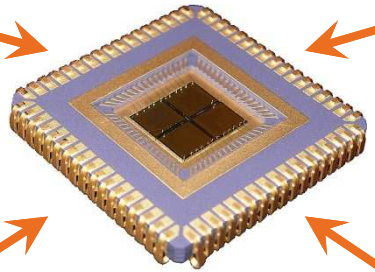
Markets who need Radiation Hardness Silicon

Space



Aeronautic

Medical / Health



Academic

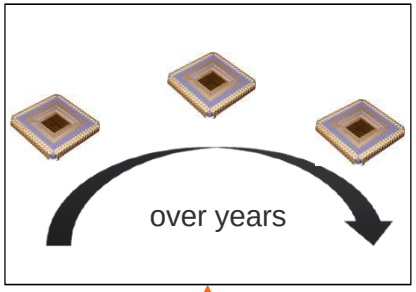
e.g. Cern accelerators / collider

Defence

Industrial / Energy

Demand of Radiation Hardness Silicon

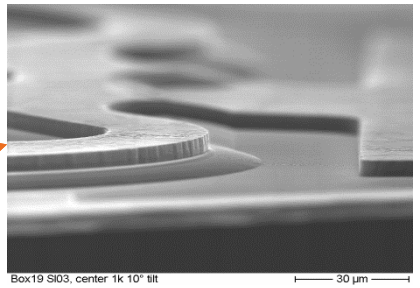
Reproducibility

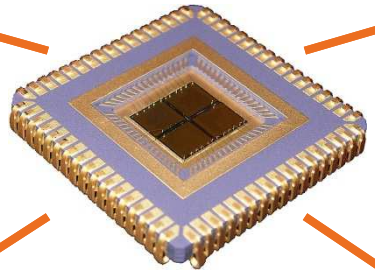


Availability

in Europe

Hardened Process

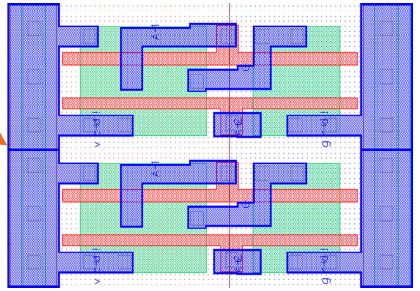




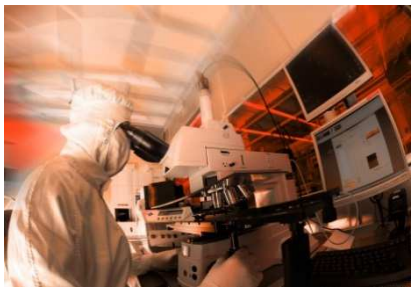
Long-life Technology

no EOL Technology

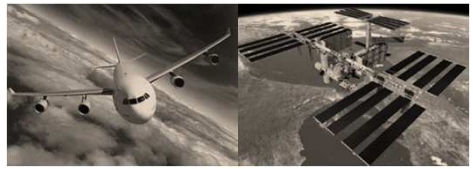
Hardened Design



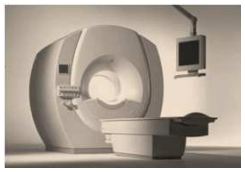
Quality awareness



LFoundry History with RadHard Silicon Devices



Aerospace

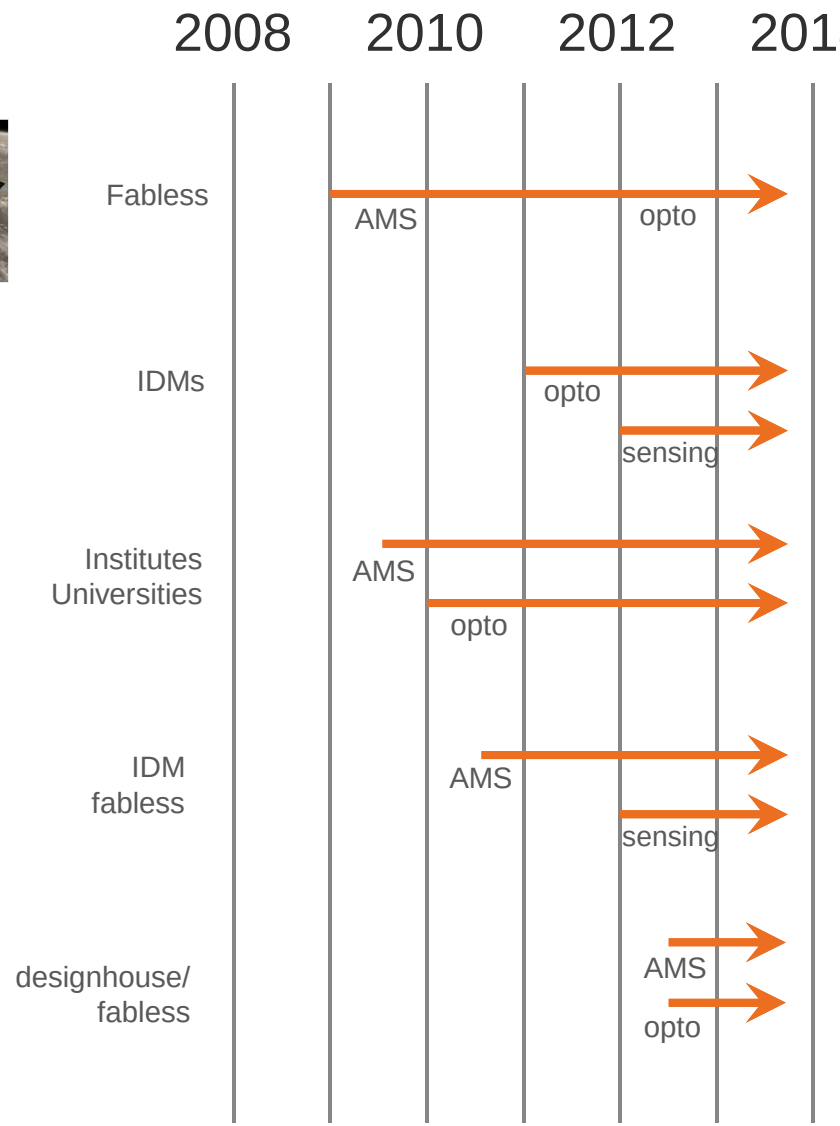


Medical / Health

Academic

Industrial / Energy

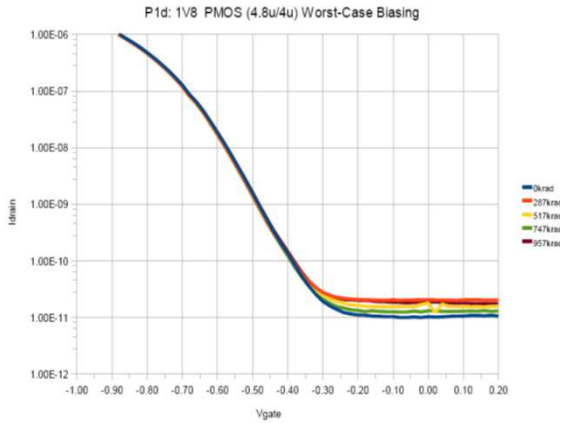
Defence



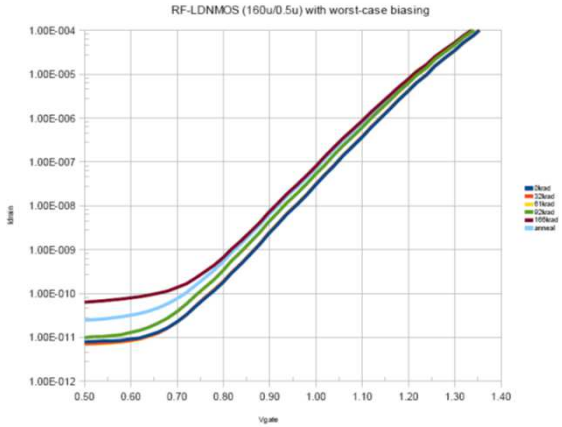
RadHard Evaluation on LFoundry 150nm foundry technology

- With partner TESAT Spacecom, LFoundry 150nm standard process single main devices were checked against TID (total ionizing dose)
  - The selected devices were fabricated with standard layout, including minimum geometries, and irradiated up to 1Mrad with different dose rates

1.8V PMOS



20V PLDMOS



irradiation sources
Gammacell 220

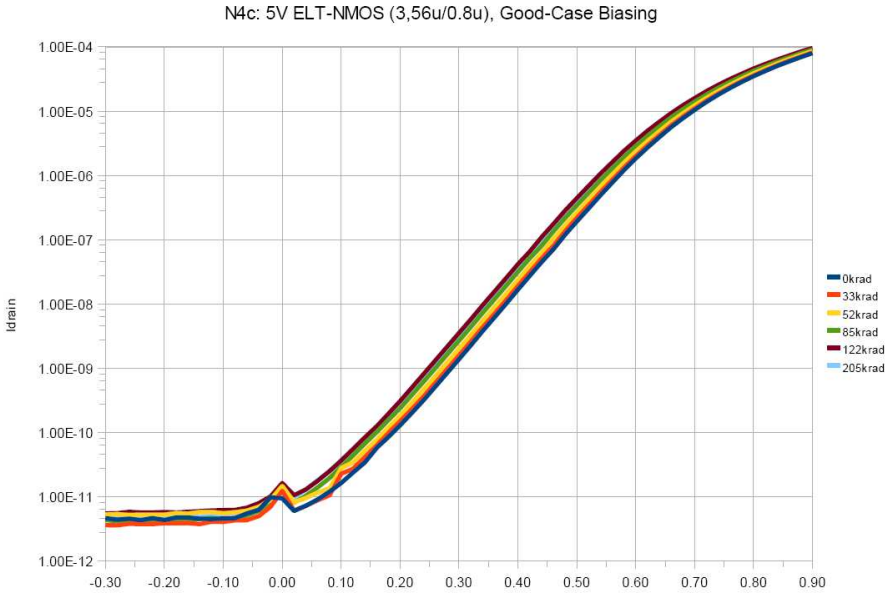
  - All PMOS devices show none or minimum degradation
  - 20V LDMOS are robust up to 160krad, with only ~50mV shift of threshold voltage
  - 1.8V NMOS are robust up to 300krad.
    At higher doses up to 1Mrad the off-state currents increase only to a few nA
  - 3.3V NMOS show good robustness with minor limitations

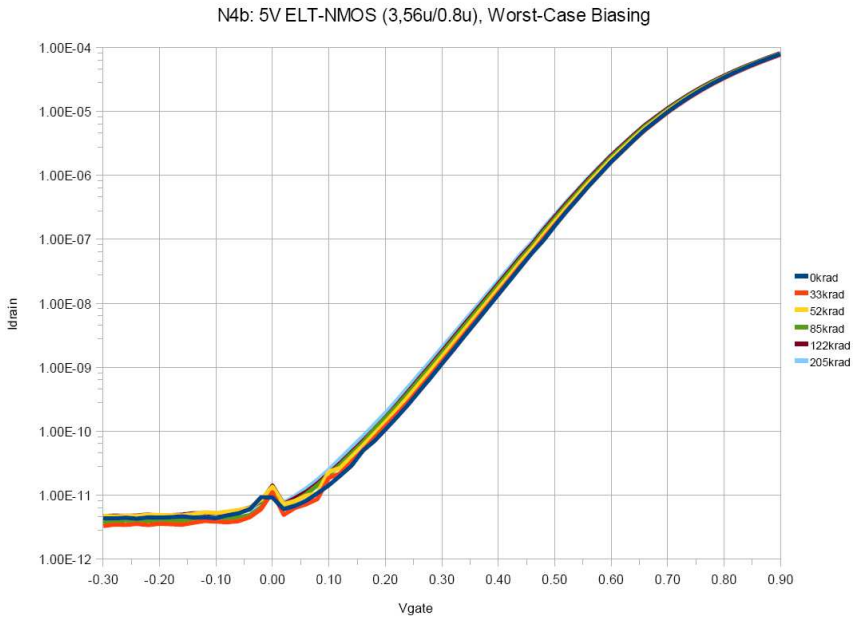
RadHard Evaluation on LFoundry 150nm foundry technology

- Devices of interest: NMOS/PMOS 5.0V MOSFET with ring shaped Poly-Gate.
  - Point of interest: Vth, Ioff
  - Method: use different Gate-Biasing during radiation; use different dose rate and total dose (100krad / 1Mrad)
- Result
  - LFoundry 150nm 5.0V with special layout of Poly-Gate is very robust and show no degradation of Vth due to radiation up to more than 200krad.

Total dose test upto 200krad: Preliminary results for 5V NMOS with „enclosed layout“

Measurement conditions: Input characteristic of drain current with Vds=5V. Vbs=0.
During radiation: Vgs=3V/Vds=0 (worst-case biasing) or Vgs=0V/Vds=3V (good-case biasing)

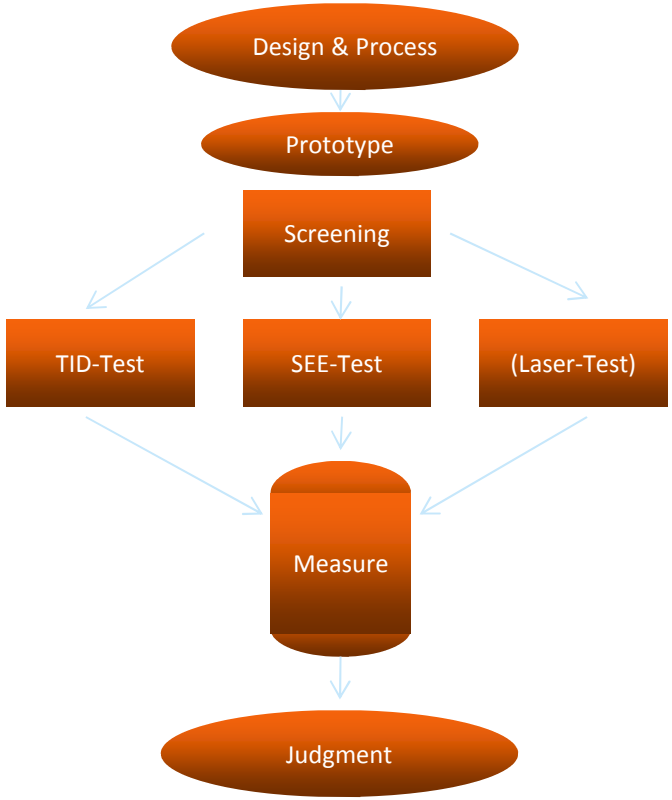




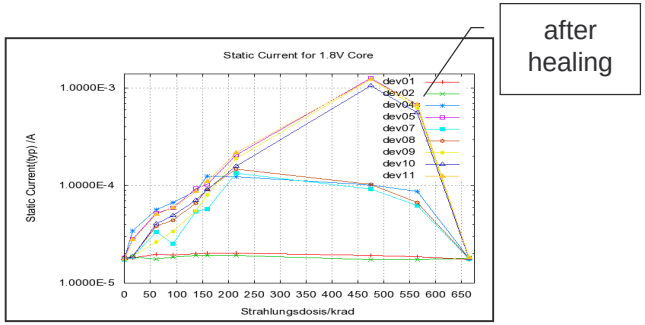
Dedicated Testchip for RadHard Evaluation of LFoundry 150nm technology

- Testchip by Tesat Spacecom / Processing at LFoundry within July 2010 MPW Shuttle
- Purpose: easy test structures first SEE-Test (single event effect) TID-Test

Function	TID	SEE (inkl. SEL)
Ring oscillator (4)	X	
Inverter Cains (3)		X
FF-Cains (3)		X
Digital Library Element's (4)		X
Input Buffer 3V	X	X
Output Buffer 3V	X	X
Output Buffer 5V	X	X
Output Buffer 7V	X	X
Output Buffer 12V	(X)	(X)
Temperature Sensor	X	X
Bandgap reference (3)	X	X
Voltage Regulator (3)	X	X
Current Control Amplifier		X

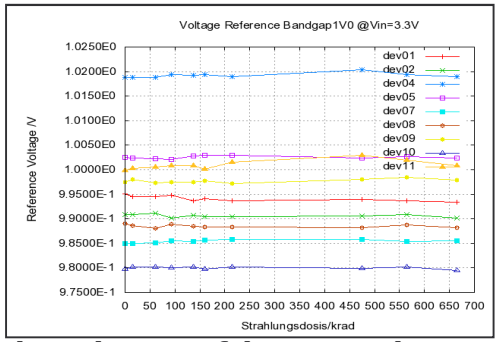


TID Results of Dedicated Testchip Evaluation of LFoundry 150nm technology

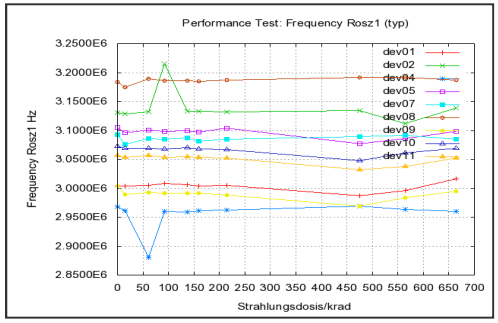


after healing

1.8V digital Core (static current)



bandgap ref (1V nom.)



freq. ring oscillator

Function	TID
Ring oscillator (4)	OK
Inverter Cains (3)	remain fully functional
Flip-Flop-Cains (3)	remain fully functional
Digital Library Element's (4)	remain fully functional
Input Buffer 3V	OK
Output Buffer 3V	OK
Output Buffer 5V	OK
Output Buffer 7V	OK
Temperature Sensor	OK until 60krad
Bandgap (3)	OK
Voltage Regulators (3)	OK

SEE Results of Dedicated Testchip Evaluation of LFoundry 150nm technology

Function	Test	Result	Comment
Digital Core	SEL	No SEL	OK
3.3 V digital IO	SEL	SELs from 33 MeVcm²/mg	further investigate
5V digital Outputs	SEL	No SEL	OK
7V digital Outputs	SEL	SELs at 85°C, 85 MeVcm²/mg	OK
Analog Circuits	SEL	No SEL	OK
Simple FFs	SEU	SEUs from 5 MeVcm²/mg	use double redundancy
Hardened FFs	SEU	Letth ~ 33 MeVcm²/mg	OK
Buffer structures	SET	Letth between 5 … 50 MeVcm²/mg	depend on the drive strength
Analog Circuits	SET	SETs from 5 MeVcm²/mg	rad hard by design

Summary

- The Foundry model enables technology access for semiconductor device designers in a neutral, non-competitive setup. This access is given
  - From small to large device design entities
  - For plug-and-play design-to-silicon but also for joint design-technology development
- More-than-Moore is not only diversification – *smart integration* of several MtM technologies into one solution is the key for new business opportunities: CMOS - OPTO - SMART POWER - MEMS
- New key techniques like wafer thinning & handling, through silicon via, … need to be more *smart integrated* into CMOS SoC setups in order to gain leverage for a wide application portfolio
- Well selected technologies in the 150nm range can be used for applications where radiation hardness is required

Thank You