The CUOF interface for the acquisition system upgrade of the CMS muon DT
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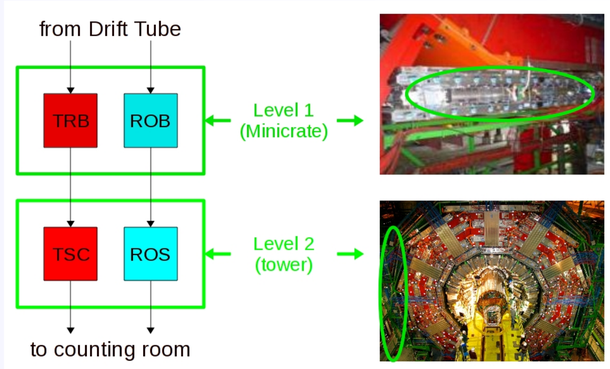
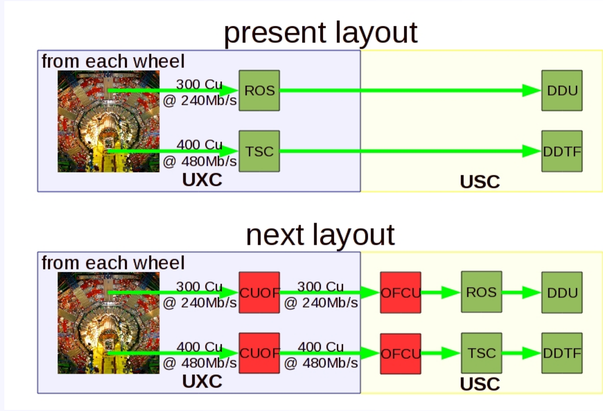
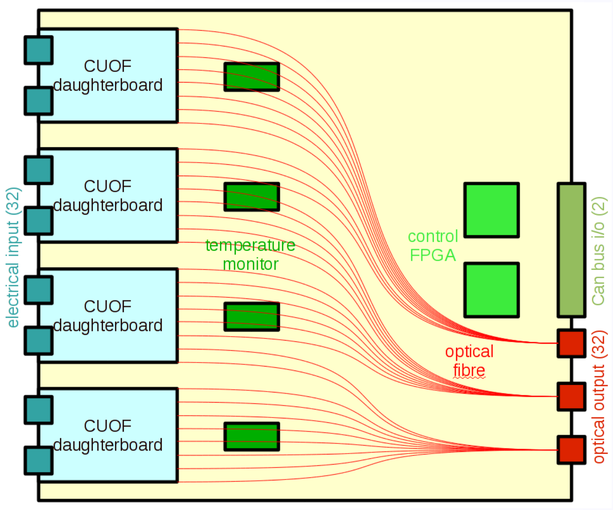
The muons generated inside the CMS experiment are detected by the Drift Tube (DT) system, that is a very large detector composed of 250 chambers arranged in 5 wheels each one split in 12 sectors, for an overall number of 172 k channels. The DT provide the muon identification and a precise momentum measurement, with input information for the trigger generation. The trigger and readout for DT is organized in layers: at the front-end, in the Minicrates, there are the on detector electronics such as the TRigger Board (TRB) and the ReadOut Board (ROB); at the back-end, in the Towers, there are the sector electronics such as the Trigger Sector Collector (TSC) and the ReadOut Server (ROS).

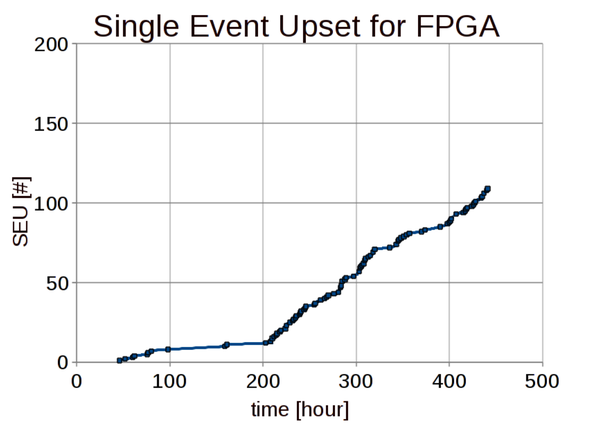


To keep the current high efficiency the complex ROS and TSC boards will be moved from the cavern to a more accessible place, where a possible fault can be handled at any time. So the new architecture foresees the relocation of these crucial cards, from the pit area (UXC) to the counting room (USC). Since the data will be transferred by optical signals, a Copper to Optical Fibre (CUOF) board is required in the cavern to manage the large number of 3500 links from the 5 wheels, while on the other side of the serial communication channel a complementary Optical Fibre to Copper (OFCU) board is planned. A maximum data rate of around 480 Mb/s is expected, for the signals relative to the trigger path.





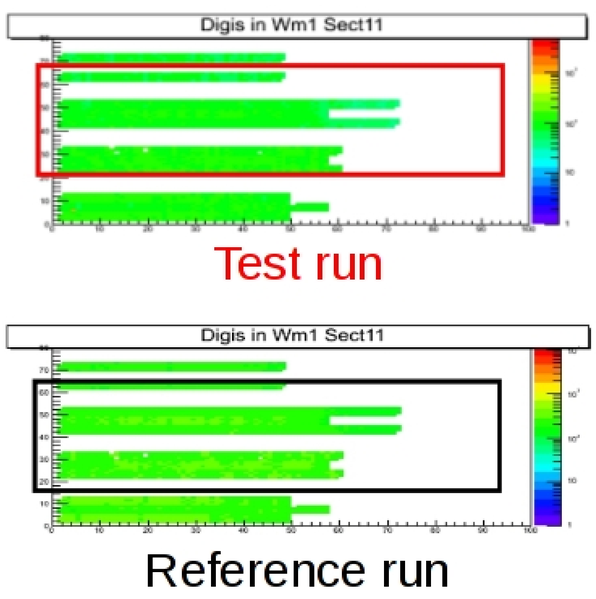
The proposed system is composed by a 9 U VME Motherboard, hosting 4 Mezzanines. Each mezzanine accommodates 8 high speed channels, where the optical outputs are available on some LC connectors. A set of fibre fanouts are foreseen to adapt the optical interface to MTP connectors, where each one is able to manage 12 optical signals. Parameters, such as the environmental temperature and supply voltage, are recorded by ADC with Inter Integrated Circuit (I^2C) ports. The slow control is managed by two redundant FPGA, to minimize problems of Single Event Upset (SEU), interfaced on two independent Can buses controlled from the counting room.



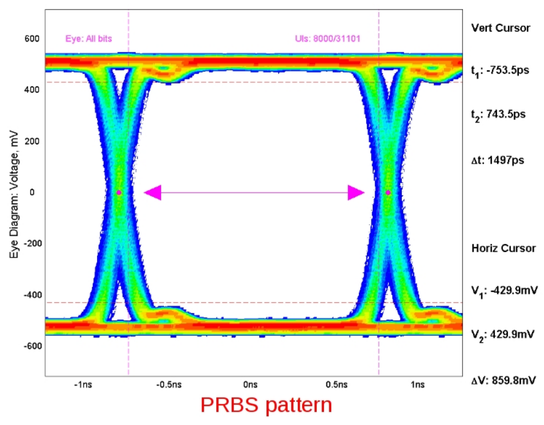
For the radiation tolerance of the system, several prototype tests were performed at the CERN facility aiming to evaluate the behaviour for a 10 years period in the High Luminosity LHC environment. With the last run an evaluation of the SEU number has been accomplished for the selected a3p600l FPGA, from Microsemi. An 8 b word has been written in a register and continuously monitored, searching for a bit flipping under irradiation. When such an event appears it is registered, and the word is restored. The SEU trend matches quite precisely with the beam integrated luminosity, and a 10 SEU/day rate for the full system has been calculated.

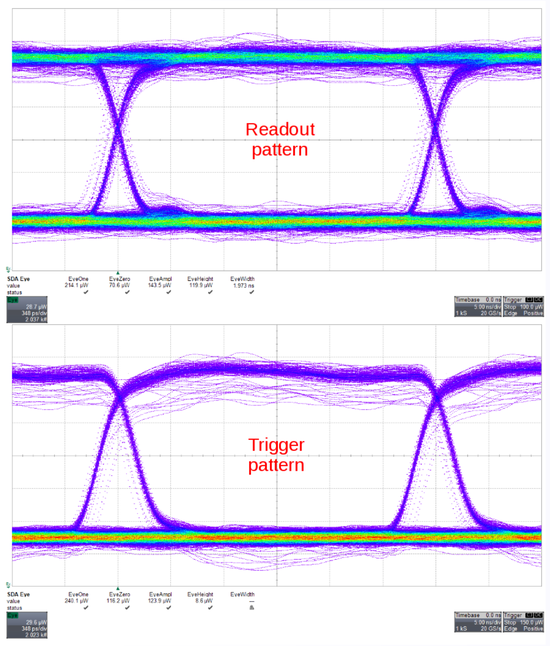
The CUOF and OFCU* prototypes were tested in the Towers to check the operation in the final environment, with the magnetic field at nominal value. The new cards were transferring data and trigger signals for several chambers, from 5 different sectors. The optical links were set according the bench tests and inserted in the current acquisition system, to compare the performances with respect to the copper links. The acquired data, analysed by the standard software tools, resulted quite good and it is not possible to distinguish them in terms of parameters as occupancy, efficiency or residuals.

* developed by INFN Bologna and by Ciemat Madrid

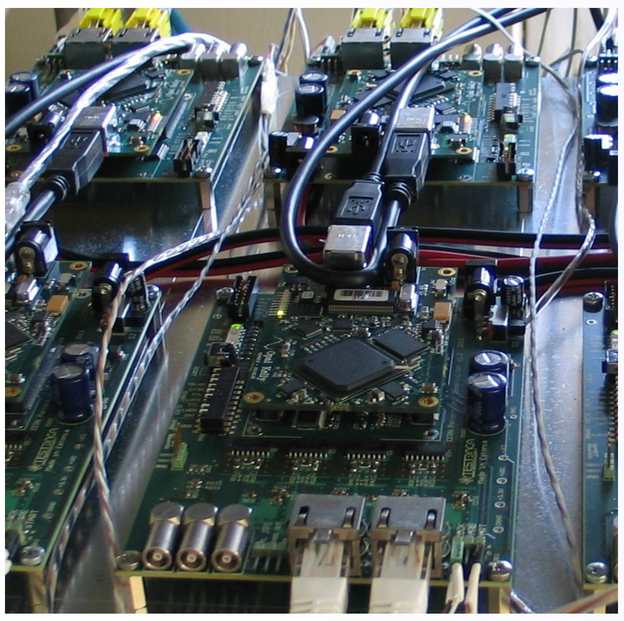


A measurement was performed for the jitter, with the Mezzanine prototype and a 50 m long optical fibre. The eye diagram shows a good image with a total jitter of 0.18 UI or 290 ps for a 622 Mb/s data rate, well beyond the required 480 Mb/s. The result was obtained by means of a Pseudo Random Bit Sequence (PRBS) with a pattern of 2^{23}-1 bit, and the circuit was verified both in open loop and in automatic power control mode. An aging test was carried out keeping the card in the climatic chamber at 70 °C and 70 % RH for 1000 hours without any significant change.





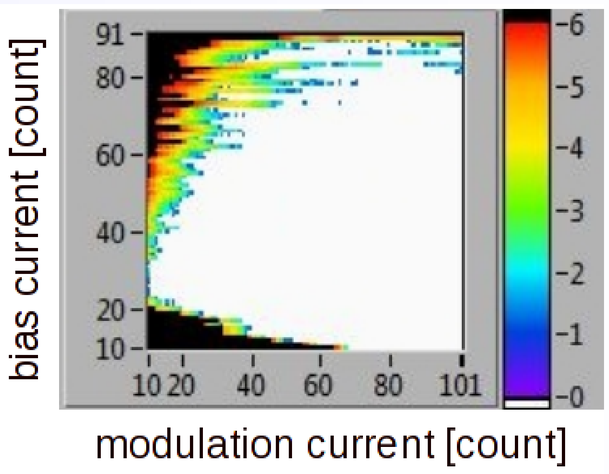
Unfortunately the actual data cannot be considered like a PRBS pattern, because the number of 0 and 1 are not balanced. This behaviour is an intrinsic factor of the current front end that doesn't allow any other data encoding, for that reason the eye diagrams are changing with respect to the pattern, with an increase of the total jitter for the trigger pattern where the unbalancing is maximum. In any case it is possible to find out a suitable working point tuning the laser diode parameters, as bias and modulation current.



To test the CUOF a new set of boards, called Pattern Unit*, has been designed to generate and acquire serial streams. The transmitter and receiver cards are controlled via USB ports, and triggered by an FPGA. All the hardware components are managed by a Labview program that, after the evaluation of the link latency, sends the input and reads the output data. Each set has its own controller PC and, if needed, they could be increased well above the current number of 4 slots.

* developed by Testonica Tallin

To qualify a CUOF Mezzanine for the experiment it must pass two test, that require several hours. The first, called scan test, is an overall error evaluation of each channel for every combination of the main laser parameters such as bias and modulation current. The second, called Bit Error Ratio (Ber) test, is a precise measurement of the link error rate in some working points that have to be less than 10^{-12} with a Confidence Level (CL) of 95%.



The first batch of CUOF Motherboard and Mezzanine is already received, and is currently under validation. With this initial production one wheel out of 5 can be equipped, and the installation is planned within October. At present, a preliminary Mezzanine yield of around 95% has been achieved. The whole production of the system is in progress, and all the cards are expected to be installed by April 2014.