

Design of the analog front-end for the Timepix3 and Smallpix hybrid pixel detectors in 130nm CMOS technology



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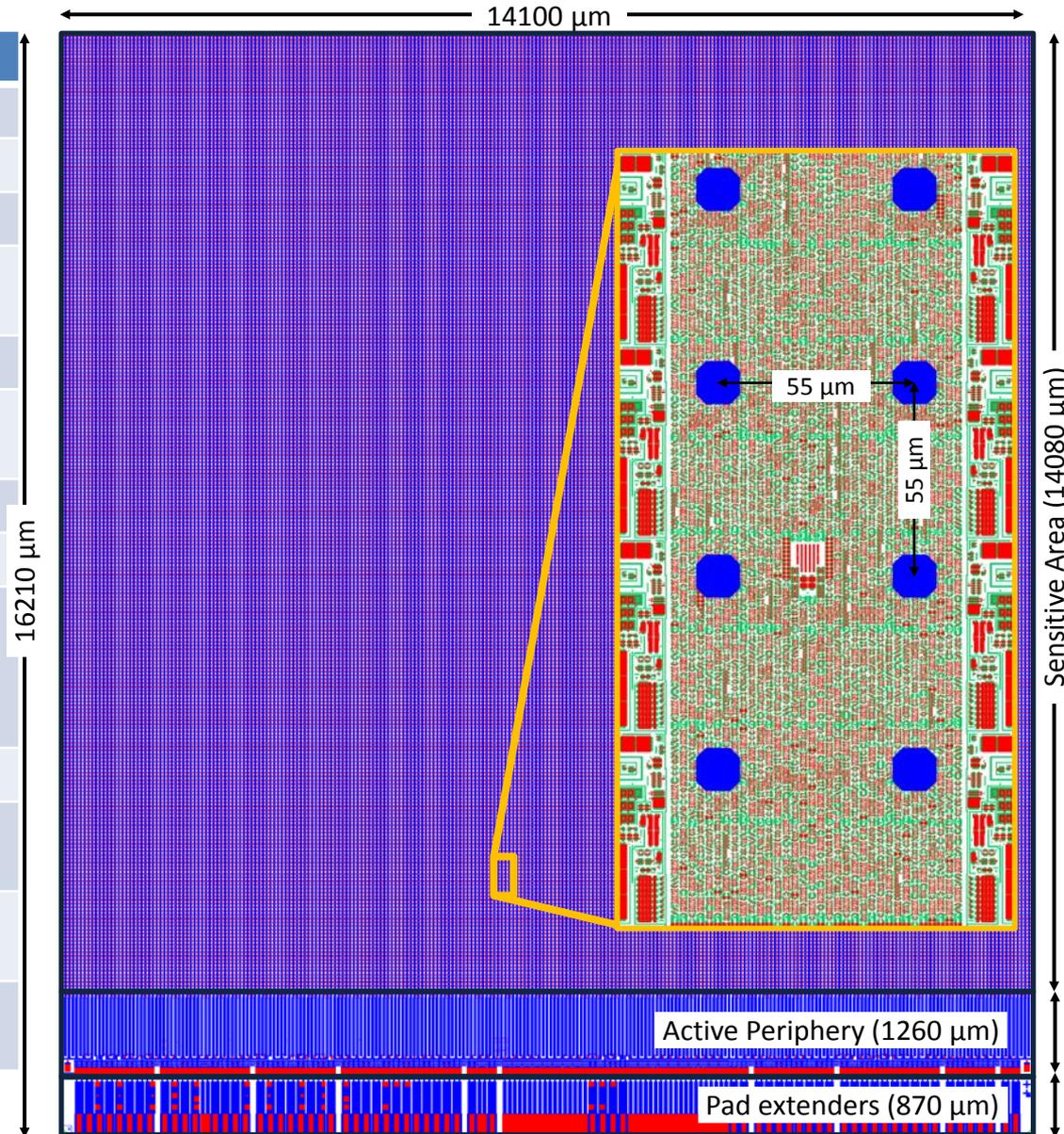
Presented at TWEPP 2013, Perugia, Sept 24th

Outline

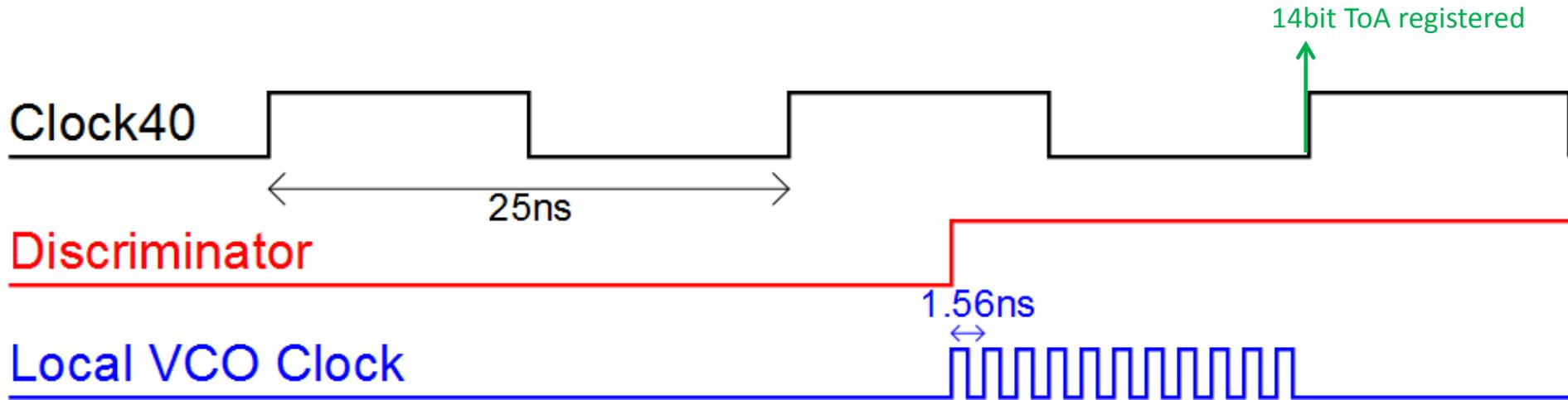
- Introduction to Timepix3
- Front-end architecture
- Timepix3: first tests
- Smallpix
- Summary

Timepix3

General features	
Pixel #	256x256
Pixel size	55 μ m x 55 μ m
Design	CERN, NIKHEF, Bonn University
Main Applications	Fast readout of solid-state pixelated sensors
	Readout of gaseous detectors (TPC)
	Vertex Locator for LHCb (further development into VELOpix)
	Power pulsing tests for the Linear Collider
What's new wrt Timepix1	Dosimetry
	2 main measurement modes: <ul style="list-style-type: none"> - simultaneous 10bit TOT and 18bit ToA - 10bit event counting and 14bit integral TOT
	TOT monotonic for large positive charges
	Fast ToA for time stamping with a precision of 1.56ns
	Data-driven readout: dead-time free, for a maximum hit rate of 40Mhits/s/cm ²
Shutdown/wake-up features for power pulsing tests on a full system	



Timepix3: fast ToA measurement



40MHz clock always running (14bit ToA)

One 640MHz VCO per superpixel (2x4 pixels) active only when a discriminator fires
(4bit fast ToA)

More information in these posters:

- “Digital Column Readout Architectures for Hybrid Pixel Detector Readout Chips” by Tuomas Sakari Poikela
- “The Charge Pump PLL Clock Generator Designed for the 1.56 ns Bin Size Time-to-Digital Converter Pixel Array of Timepix3 Readout Chip” by Yunan Fu

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- **Front-end architecture**
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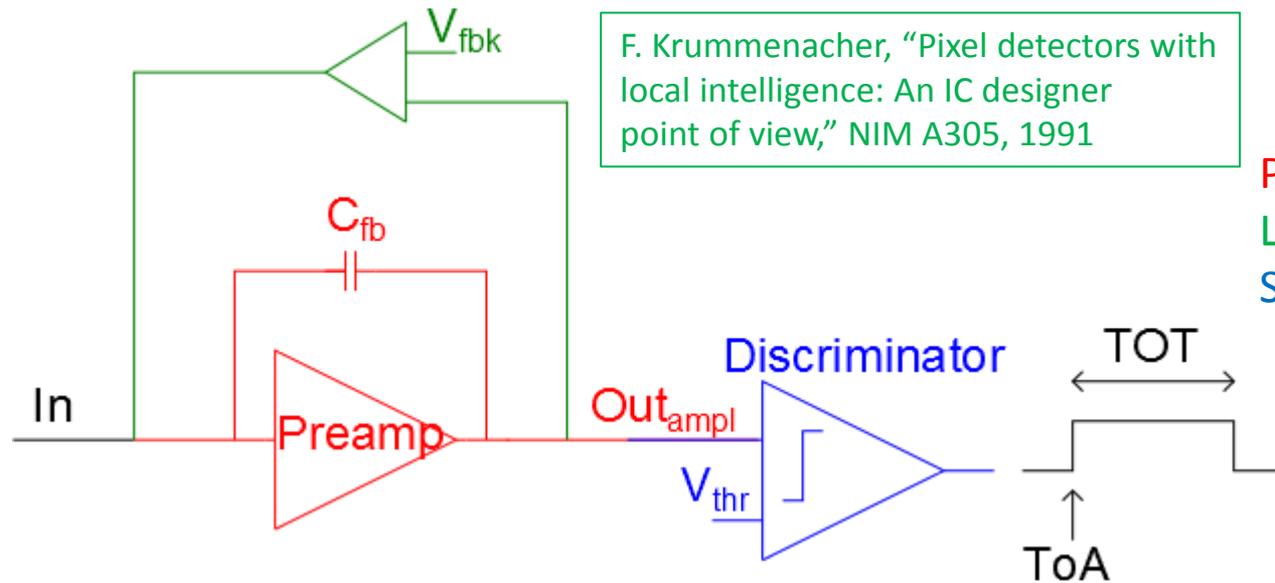
Front-end architecture in use

F. Krummenacher, "Pixel detectors with local intelligence: An IC designer point of view," NIM A305, 1991

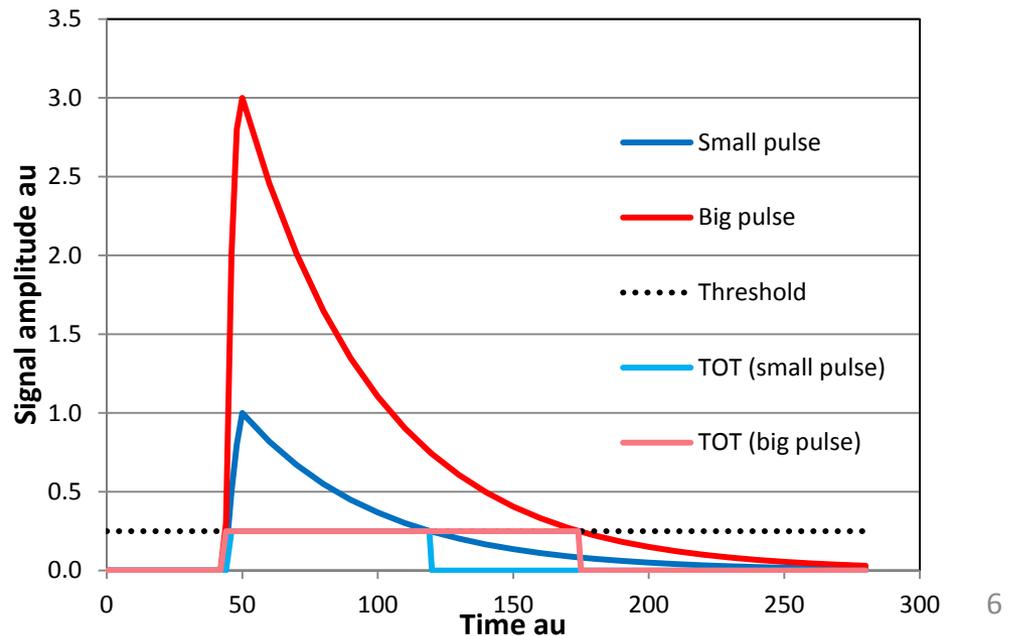
Preamplifier

Leakage current compensation

Single-threshold discriminator



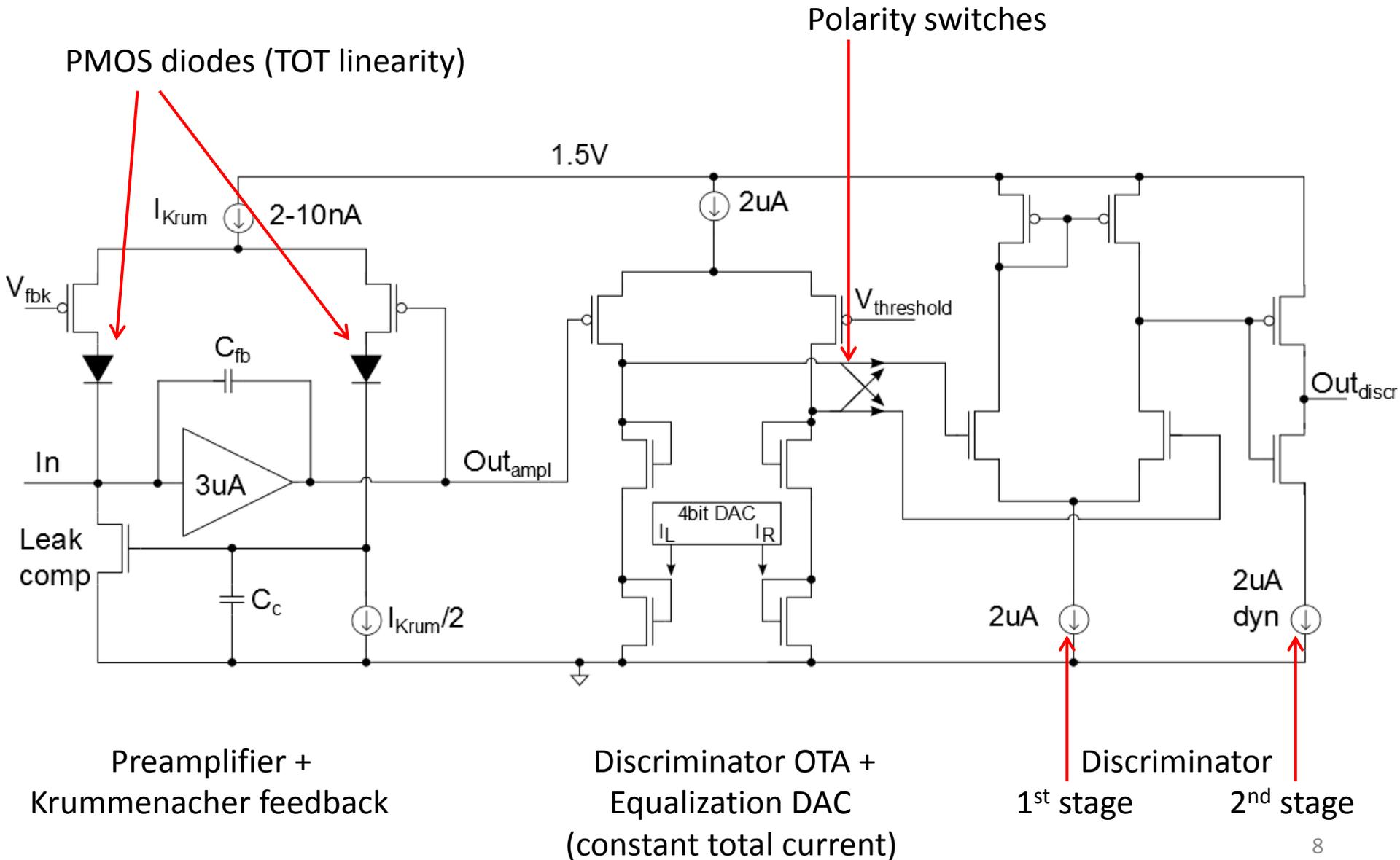
The output of the discriminator is used to measure Time-Over-Threshold (proportional to the energy deposited in the pixel) and/or Time of Arrival (time stamping of the hit).



Timepix3: front-end specifications

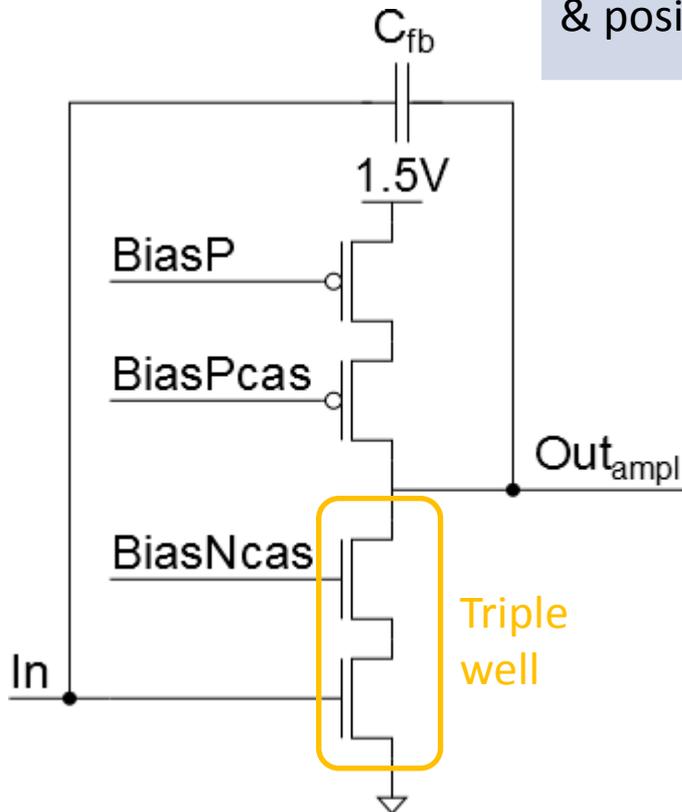
Parameter	Value	Notes
Area	55 μ m \times 13.5 μ m	
Signal polarity	Positive and negative	
Detector capacitance	~50fF	25fF to 100fF
Leakage current	-5nA to +20nA	
Amplitude linearity	Not required	Time measurement
TOT monotonicity	Yes, up to 300kh ⁺	
ToA jitter and mismatch	Compatible with 1.56ns resolution	Gas detector applications
Time-to-peak	Target 25ns	In view of VELOpix
Noise + threshold mismatch	~90e ⁻	for a minimum threshold ~500e ⁻
Equalization DACs	4bit	Compensate pixel-to-pixel threshold mismatch
Power consumption	12 μ W/pixel	

Timepix3: front-end architecture



Timepix3: preamplifier

	Timepix	Timepix3	Notes
Preamplifier	Differential	Single-ended	More efficient power usage
C_{fb}	8fF	3fF	Larger gain
Input pad size & positioning	20x20 μm , over analog domain	12x12 μm , over digital domain	Minimize parasitics, shielding to analog ground

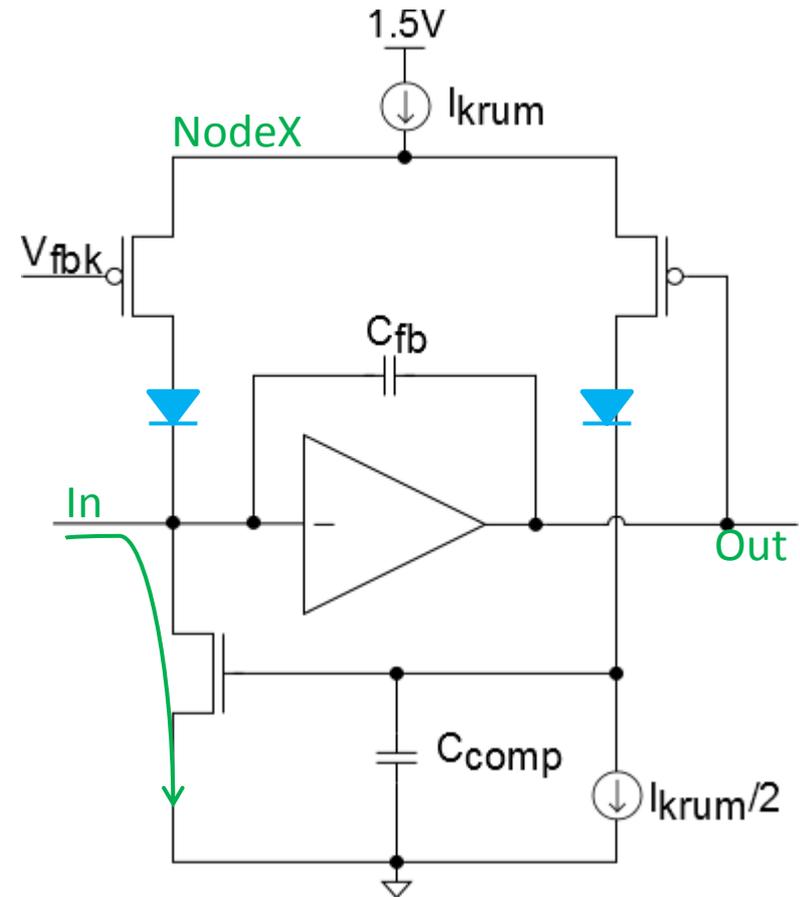
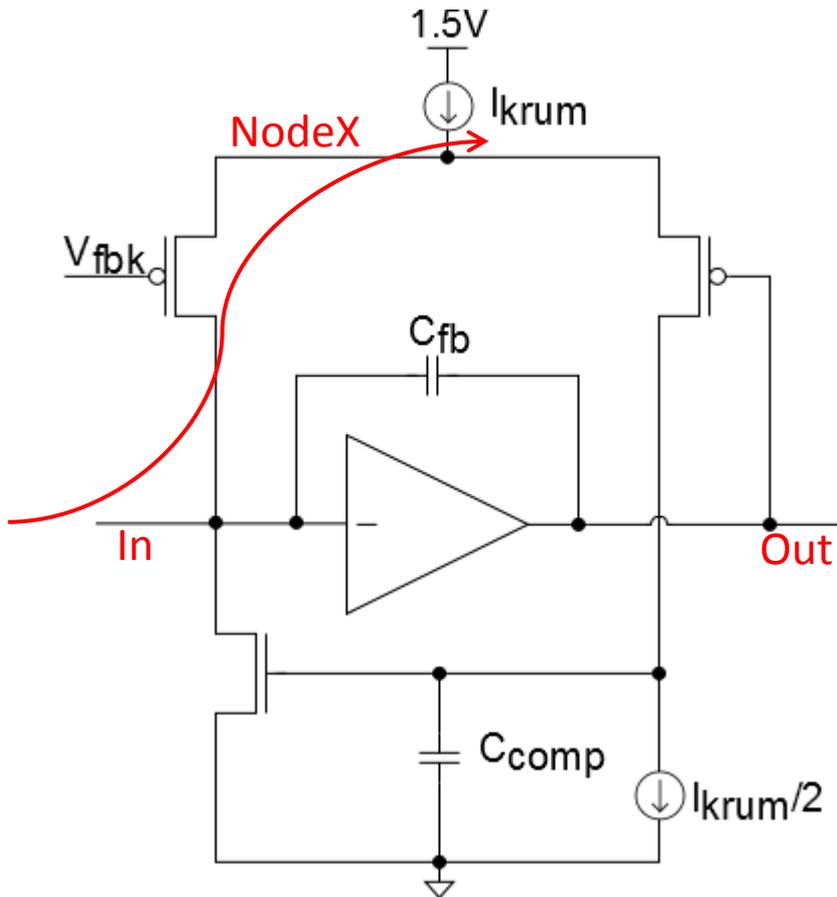


TOT monotonicity

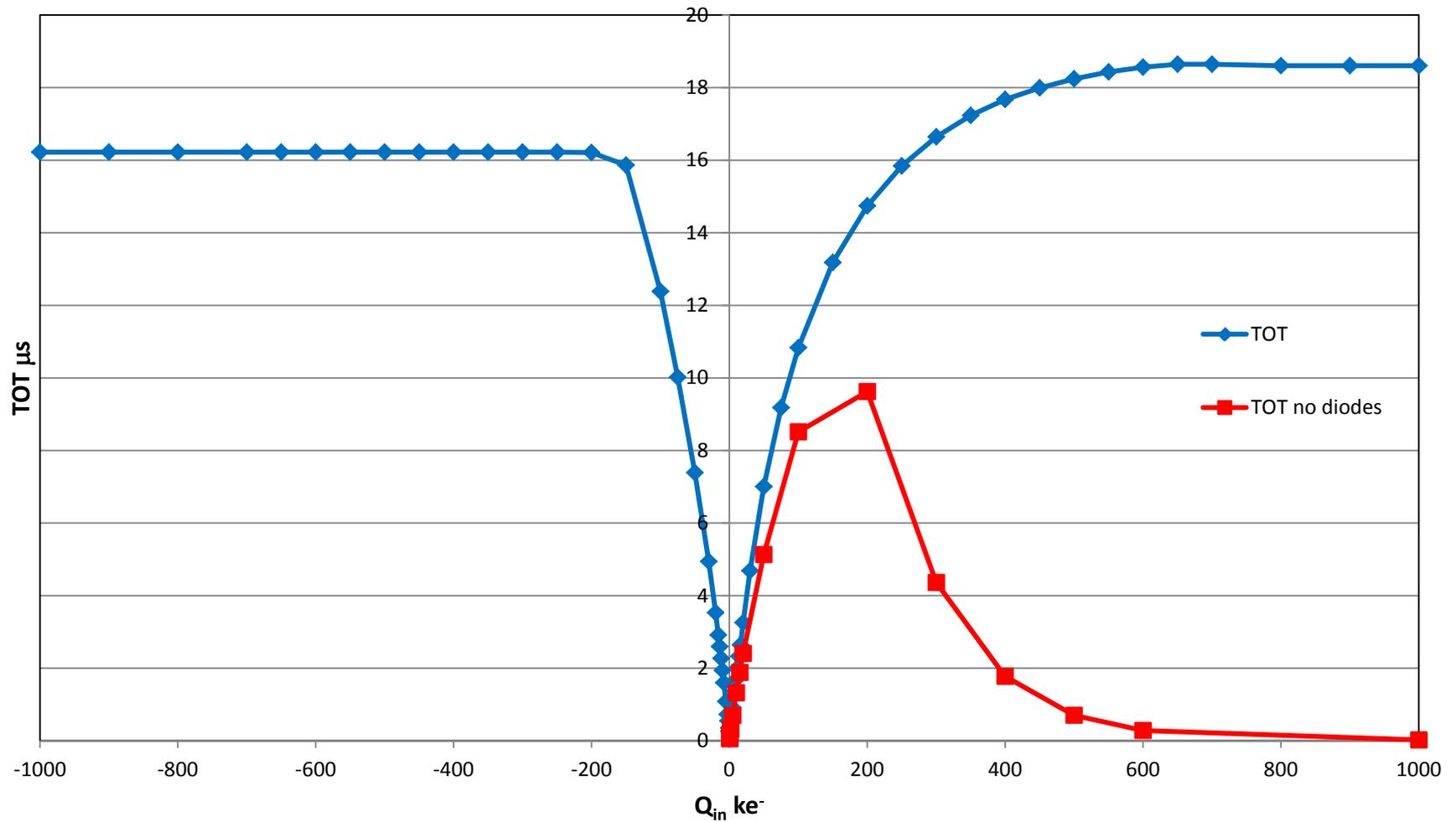
TOT monotonicity issue for large positive input charges:

$Q_{in} > 100kh^+ \rightarrow V(In) > V(NodeX) \rightarrow$ current through the **wrong path**

Added diode-connected PMOS transistors \rightarrow **good current path**



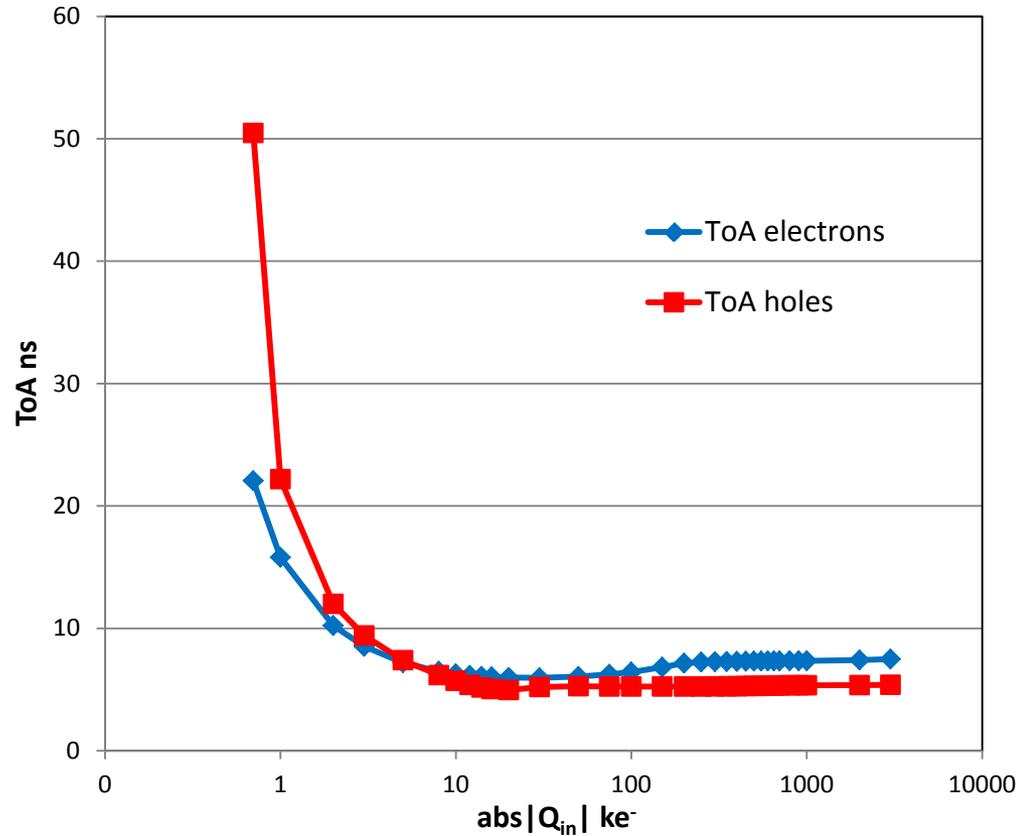
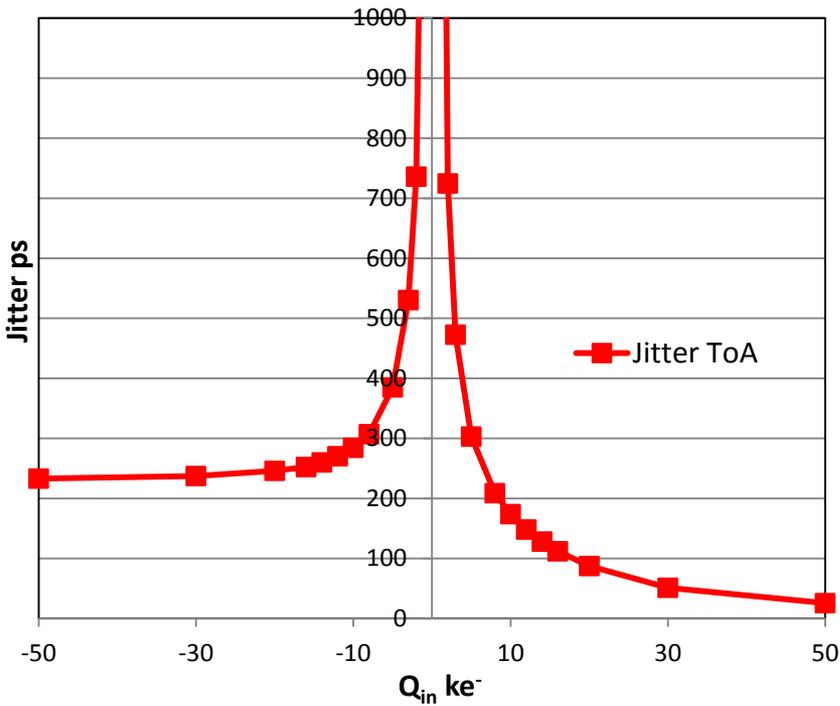
TOT monotonicity



Comparison between TOT with and without monotonicity PMOS diodes.

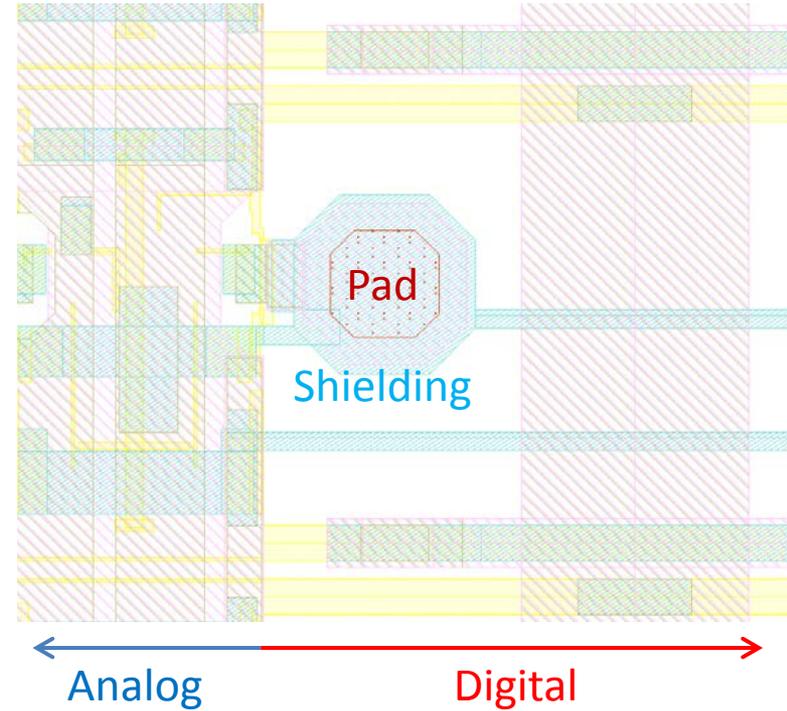
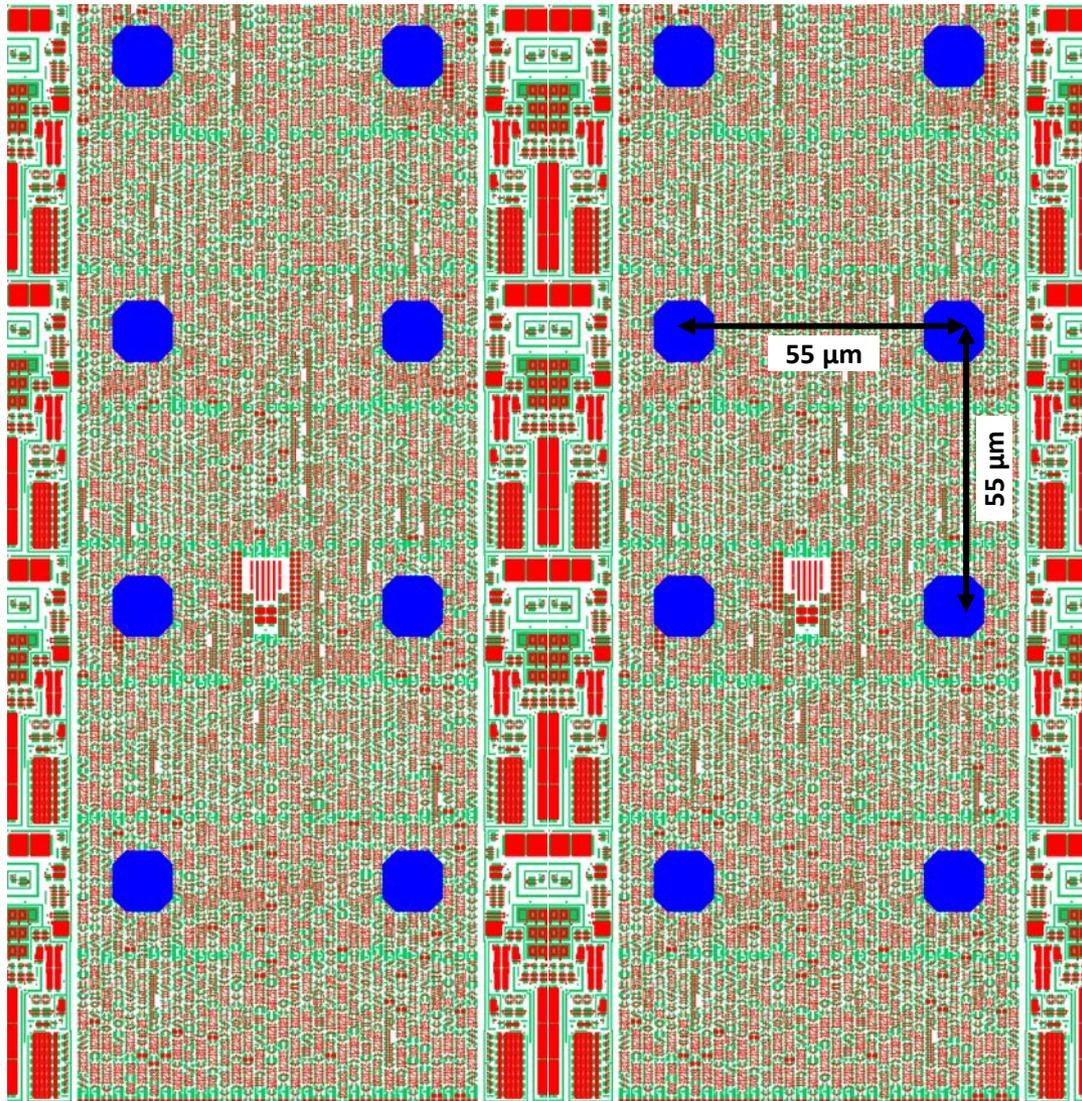
Fast ToA resolution

Time resolution of 1.56ns \rightarrow low ToA jitter and mismatch

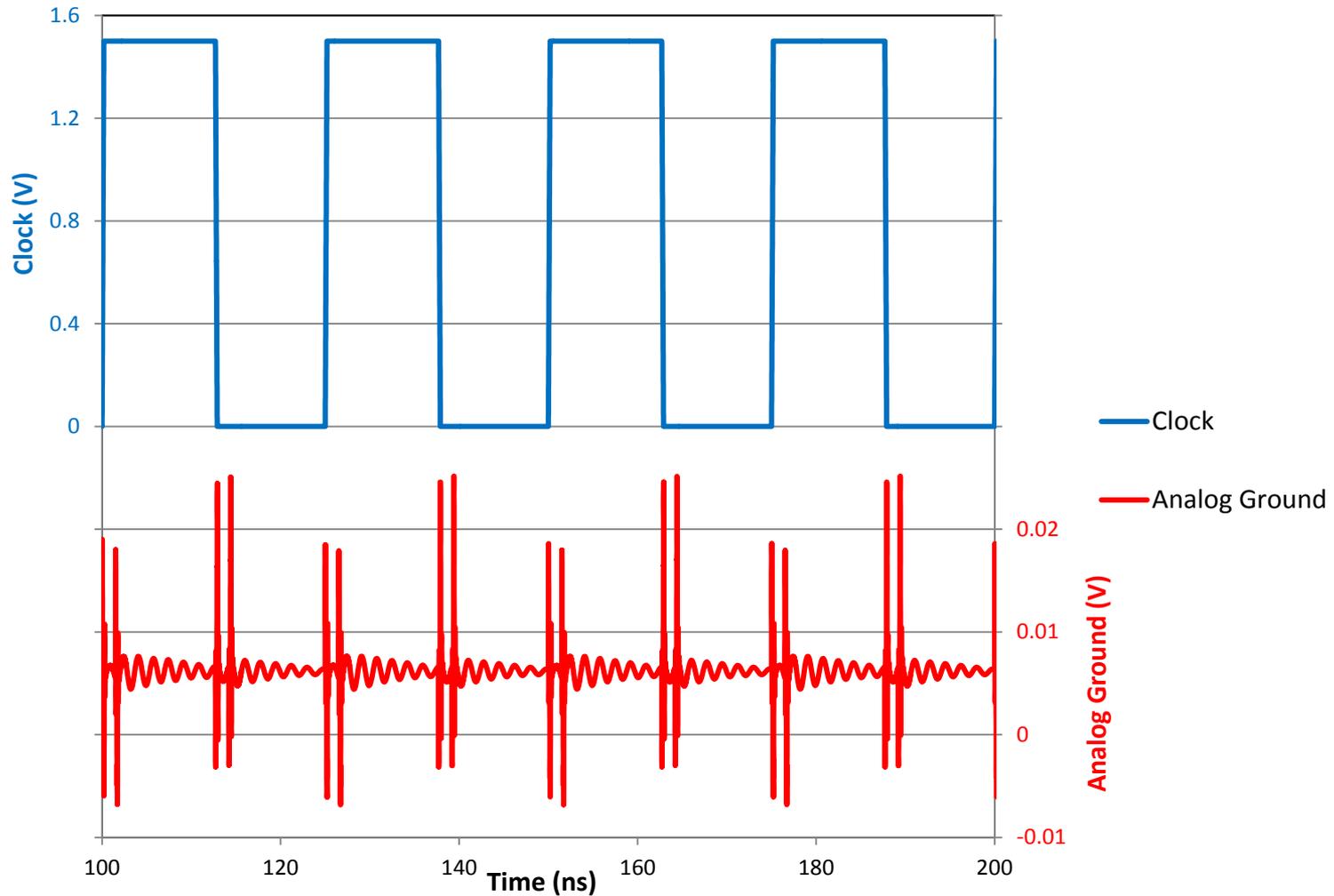


Pixel-to-pixel timing mismatch is simulated to be lower than 500ps for charges of $10ke^-$

Noise coupling digital->analog

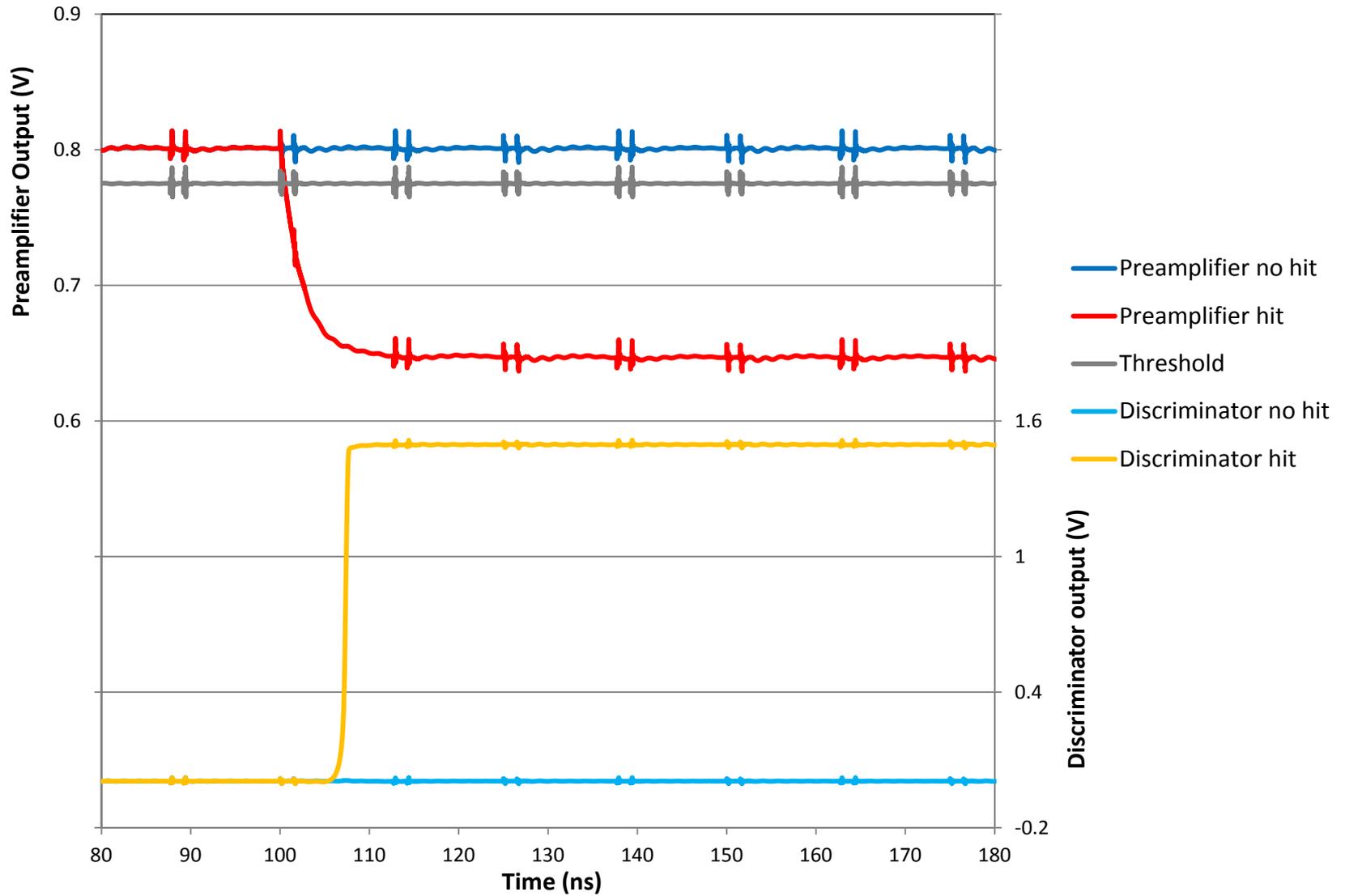


Digital noise



Simulation models include wirebond parasitics, decoupling capacitors, resistances and parasitic capacitances of the metal lines running along the columns in the pixel matrix.

Noise coupling



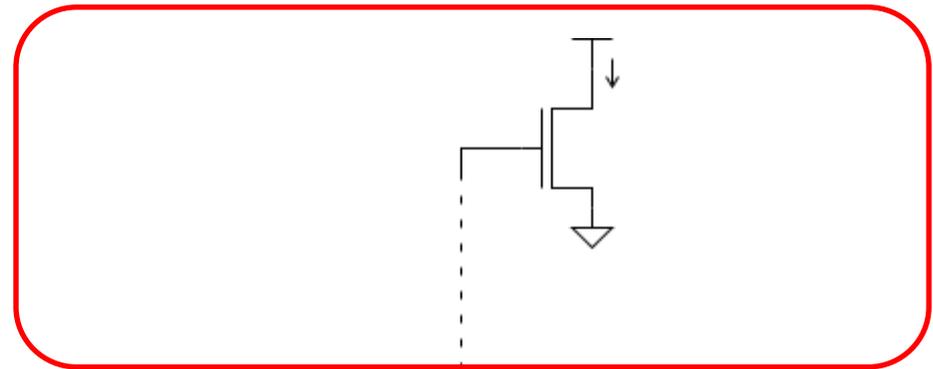
Power pulsing

Analog domain:
switch dynamically between nominal
and shutdown bias currents

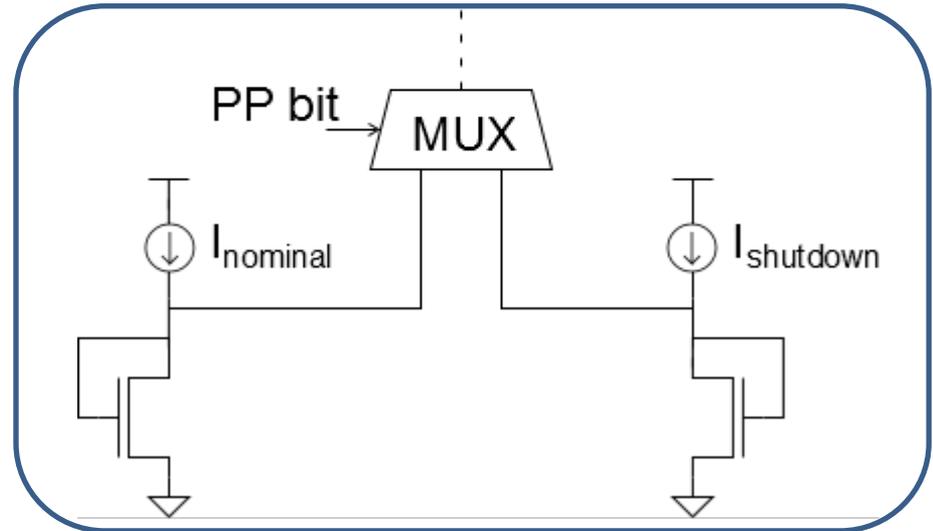
Digital domain:
gate the clock to the pixel array

Transition times programmable
between 800ns and 1.28ms

Pixel array



Periphery



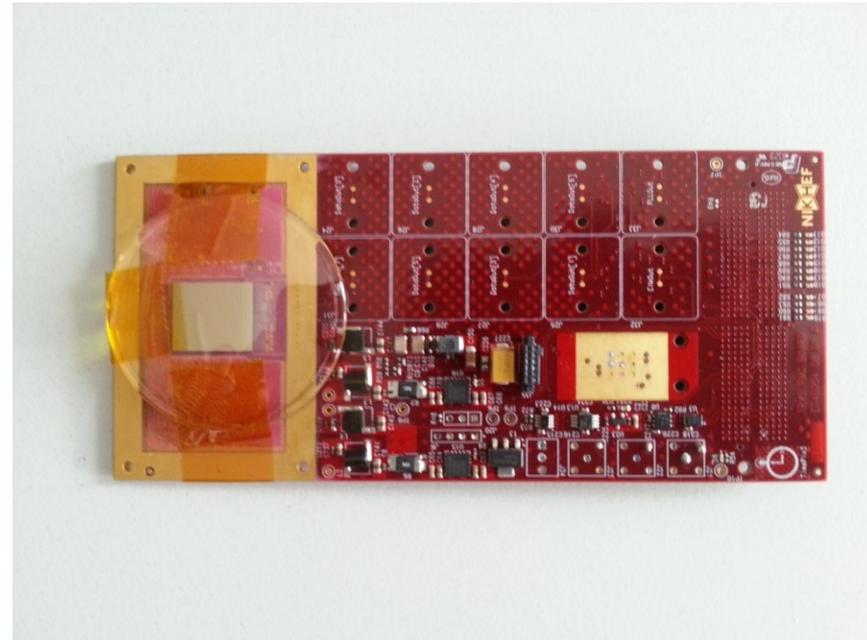
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Preliminary test results

2 chips under test
since beginning of September

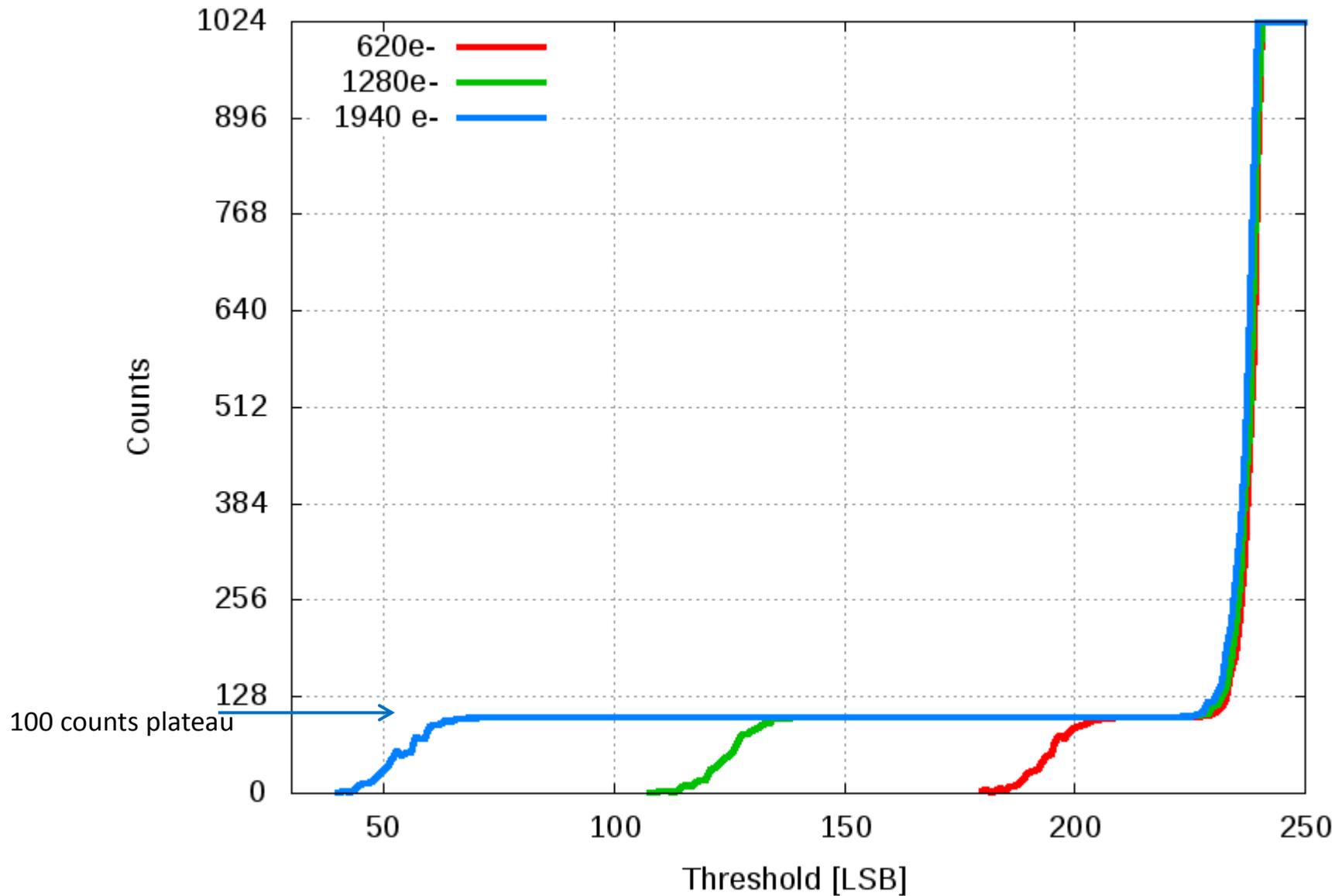
- Periphery tested at 95%, no issues detected
- Data readout functional at full speed (640MHz)
- Current consumption:
 - Analog 450mA
 - Digital 370mA (in data driven mode and no pulses injected)



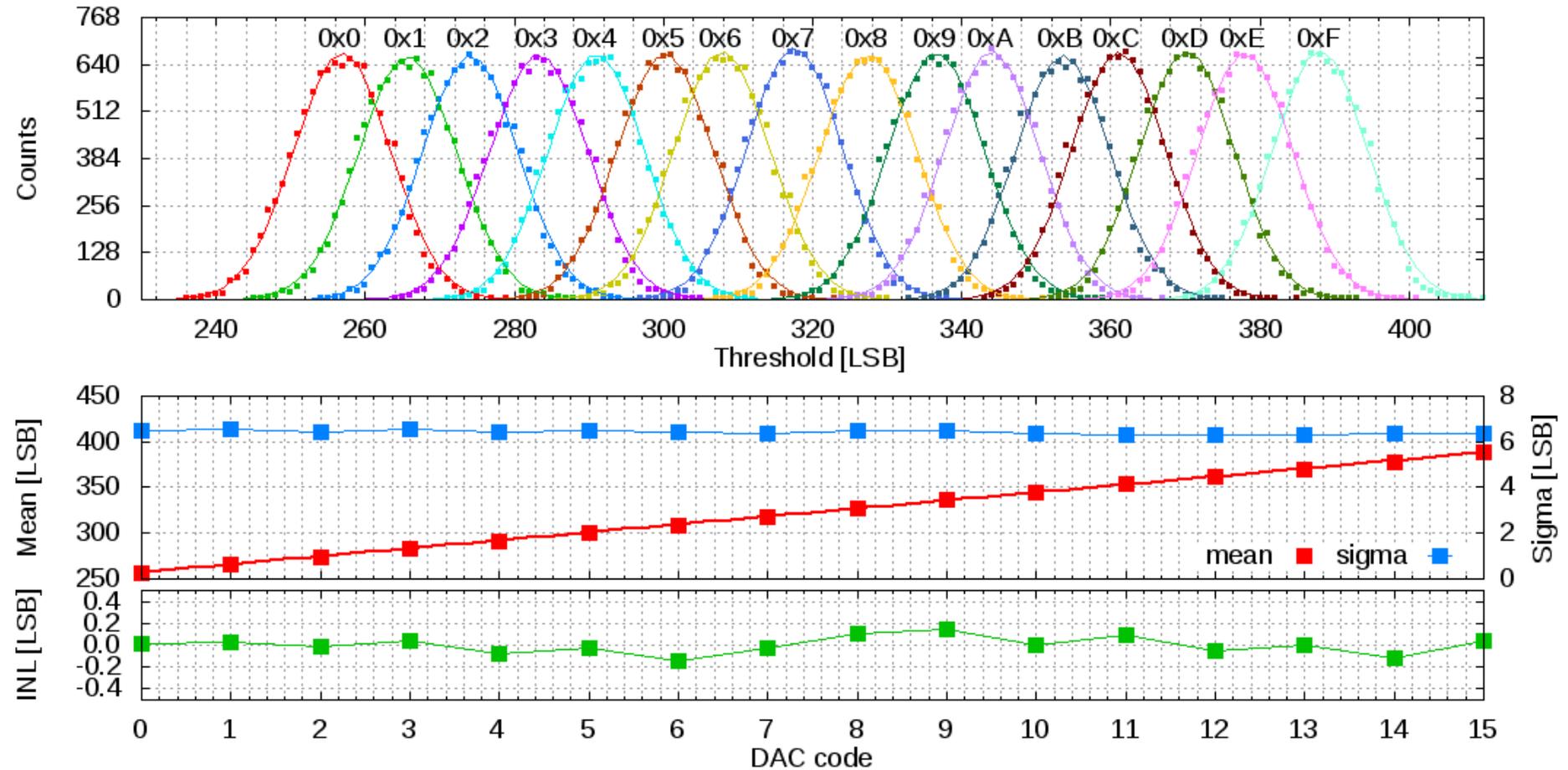
Credits:

Bas van der Heijden, Frans Schreuder, Henk Boterenbrood (NIKHEF)
Szymon Kulis (CERN)
for the SPIDR board, readout system and the plots in the next slides

S-curves: 100 pulses in Photon Counting + integral TOT mode



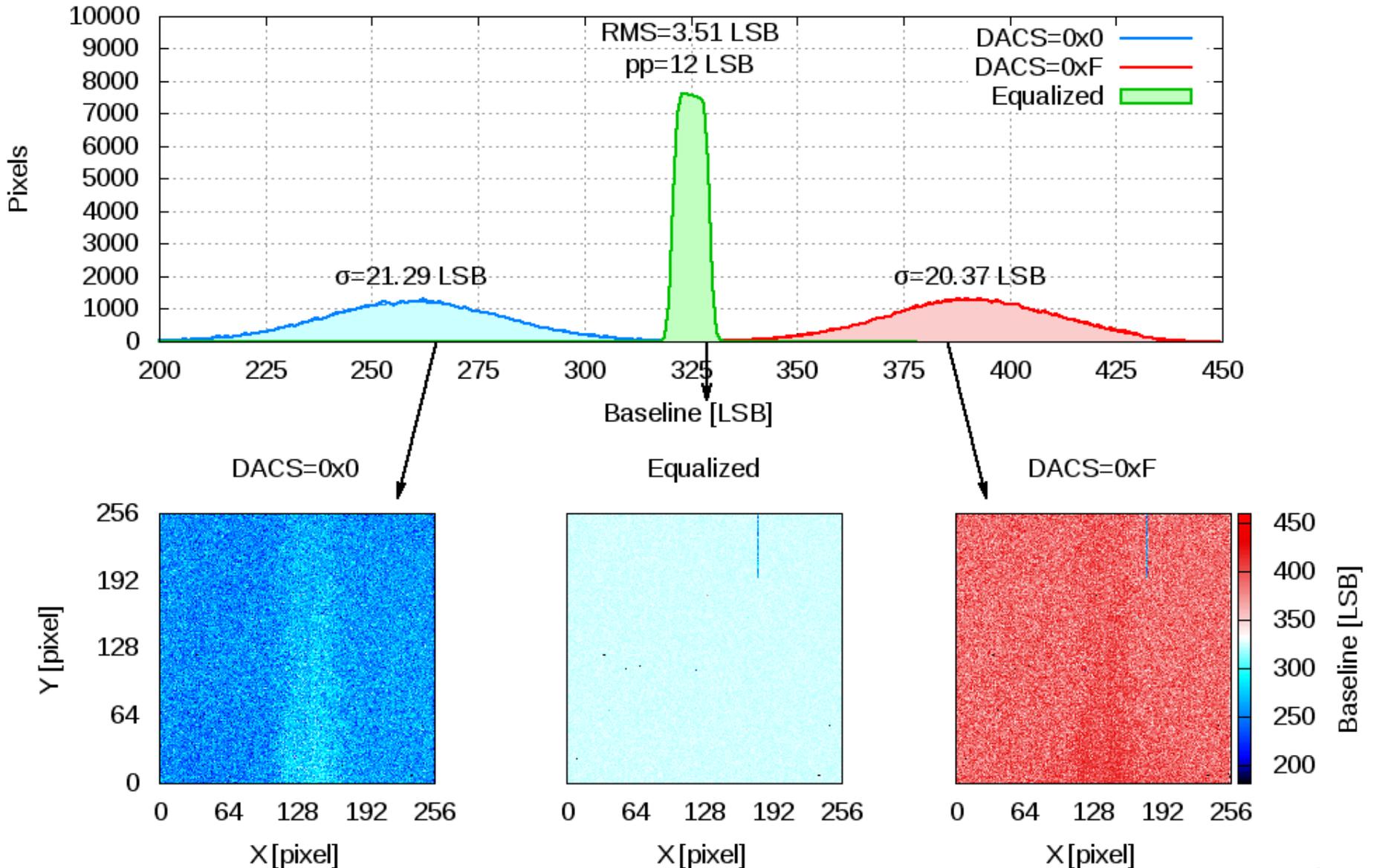
Scan of a pixel equalization DAC



4bit equalization DAC shows very good linearity, as expected.

Noise 6.5LSB: $\sim 65e^-$ (better than $75e^-$ expected), **assuming** $50\text{mV}/\text{ke}^-$ gain.

Equalization results



Mismatch: $178e^-$ before equalization, $30e^-$ afterwards.

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Smallpix (renaming pending)

		Notes
Applications	Vertex Detector	
	Dosimetry	
	Imaging & general purpose	
Goals	Decrease pixel size (40 μ m?) wrt Timepix3 and Medipix3	Still providing TOT and ToA
	Array of 250k pixels (if possible)	Suitable to system tests, e.g. power pulsing
Main features foreseen today	Full Through-Silicon-Vias (TSV) connectivity	Re-distribute periphery circuitry, active area approaching 100%
	Fast OR	Triggering capability
	Data compression	Per pixel and per column
	Superpixels 2x2	Share resources, increase counters' depth
Status	Reuse Timepix3 front-end	If it proves successful
	Redesign of building blocks (bandgap, ESD protections, ...)	Needed for TSV compatibility

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Summary

- Front-end designed and fabricated in the full-scale Timepix3 chip.
- Tests recently started. So far it looks functional:
 - Power ok
 - Noise $65e^-$ good
 - Mismatch $30e^-$ ok
 - Noise + mismatch = $\sim 71e^-$: minimum threshold around $430e^-$?
 - These are **preliminary** measurements!
- If no major issue shows up, this front-end can be re-used for the Smallpix chip. Layout to be modified to accommodate in a different form factor.

Thanks for your time and attention!

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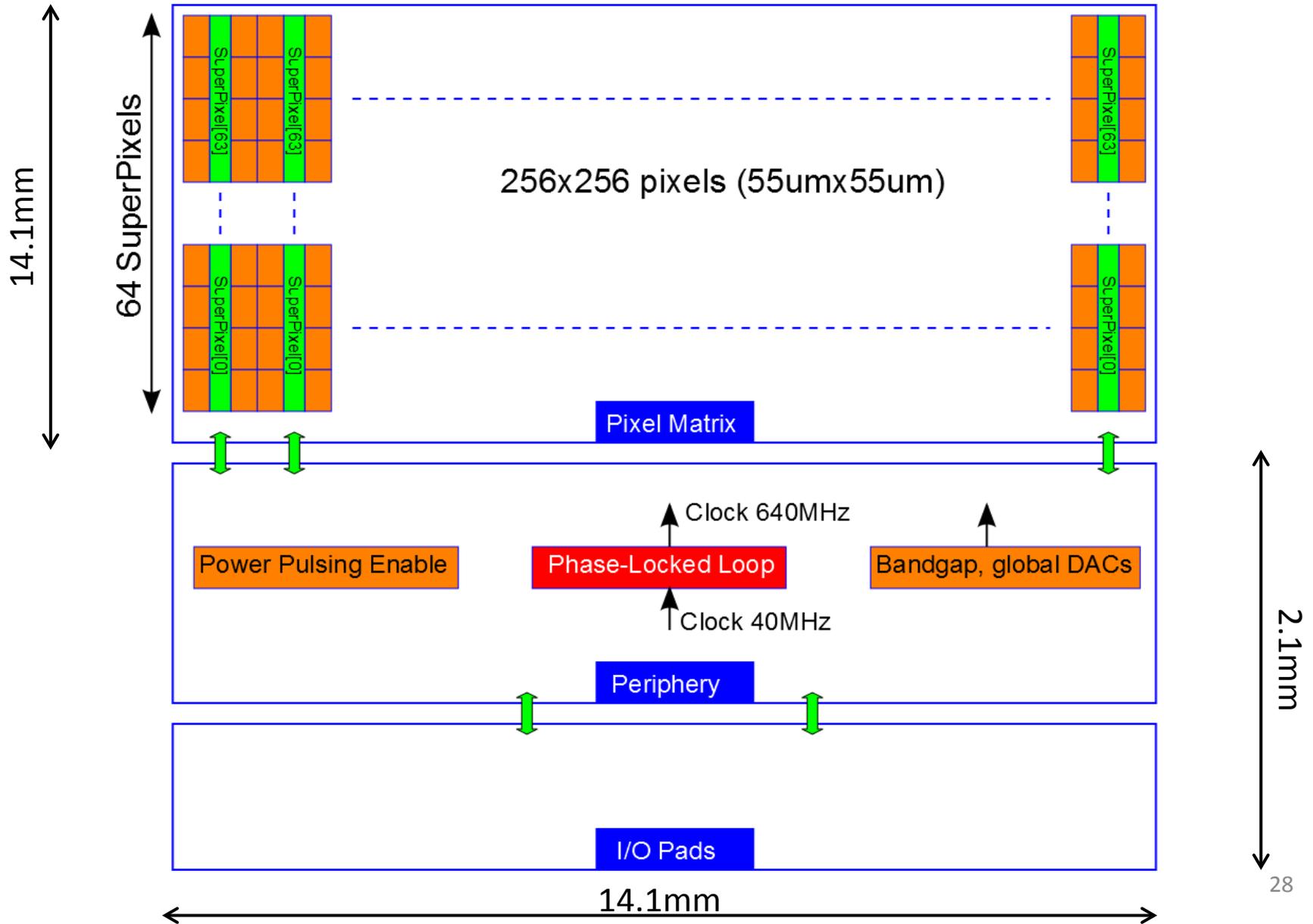
Massimiliano De Gaspari for the CERN Medipix team:

Jerome Alozy, Rafael Ballabriga, Michael Campbell, Erik Fröjd, John Idarraga, Szymon Kulis, Xavier Llopart, Tuomas Poikela, Pierpaolo Valerio, Winnie Wong.

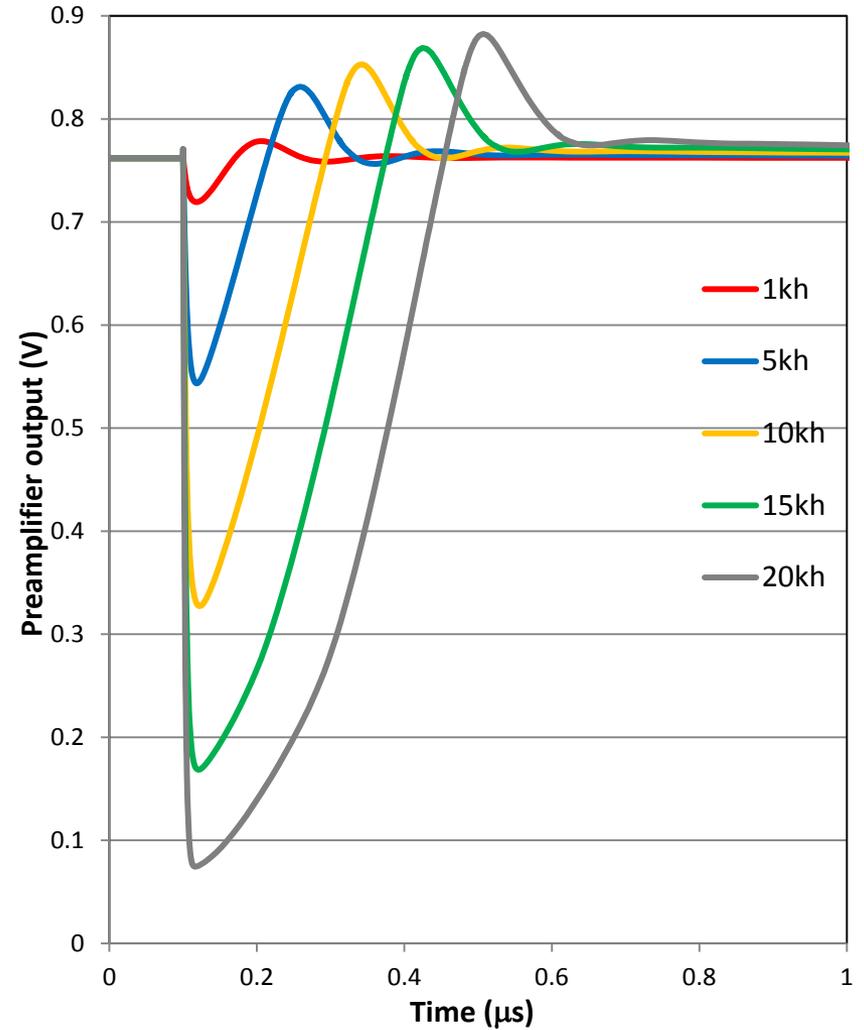
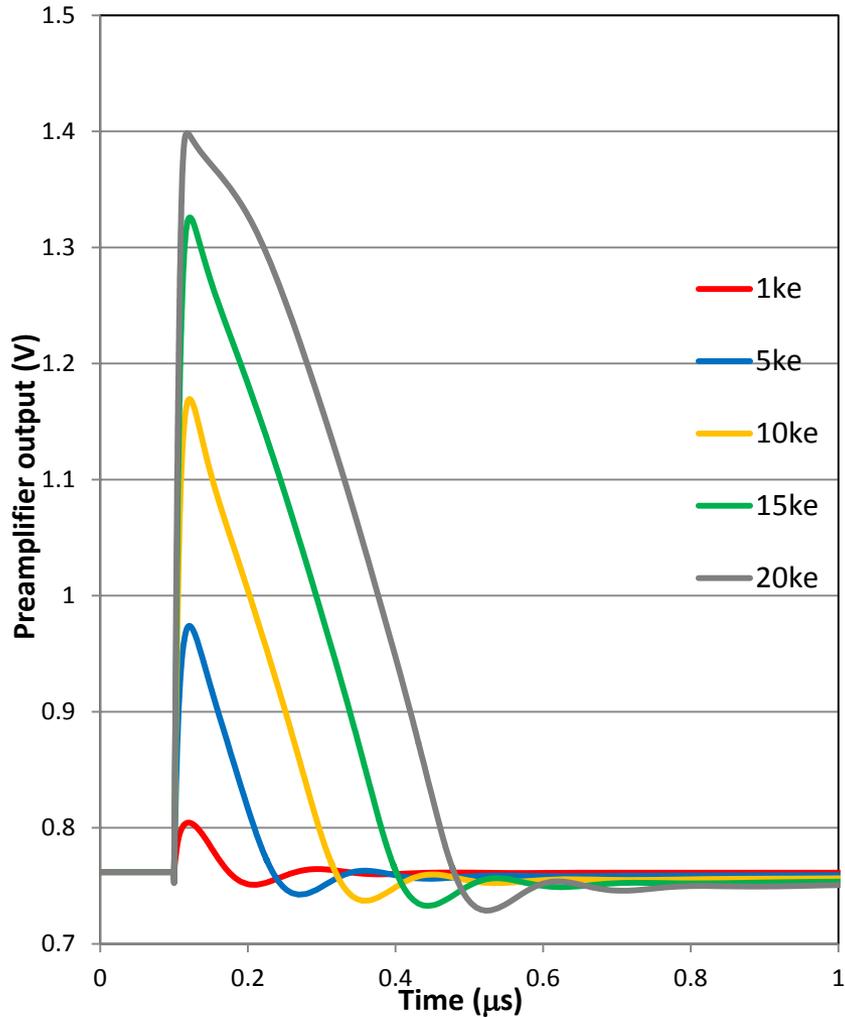
Outline

- Back up slides

Timepix3: floorplan



Examples: preamplifier output

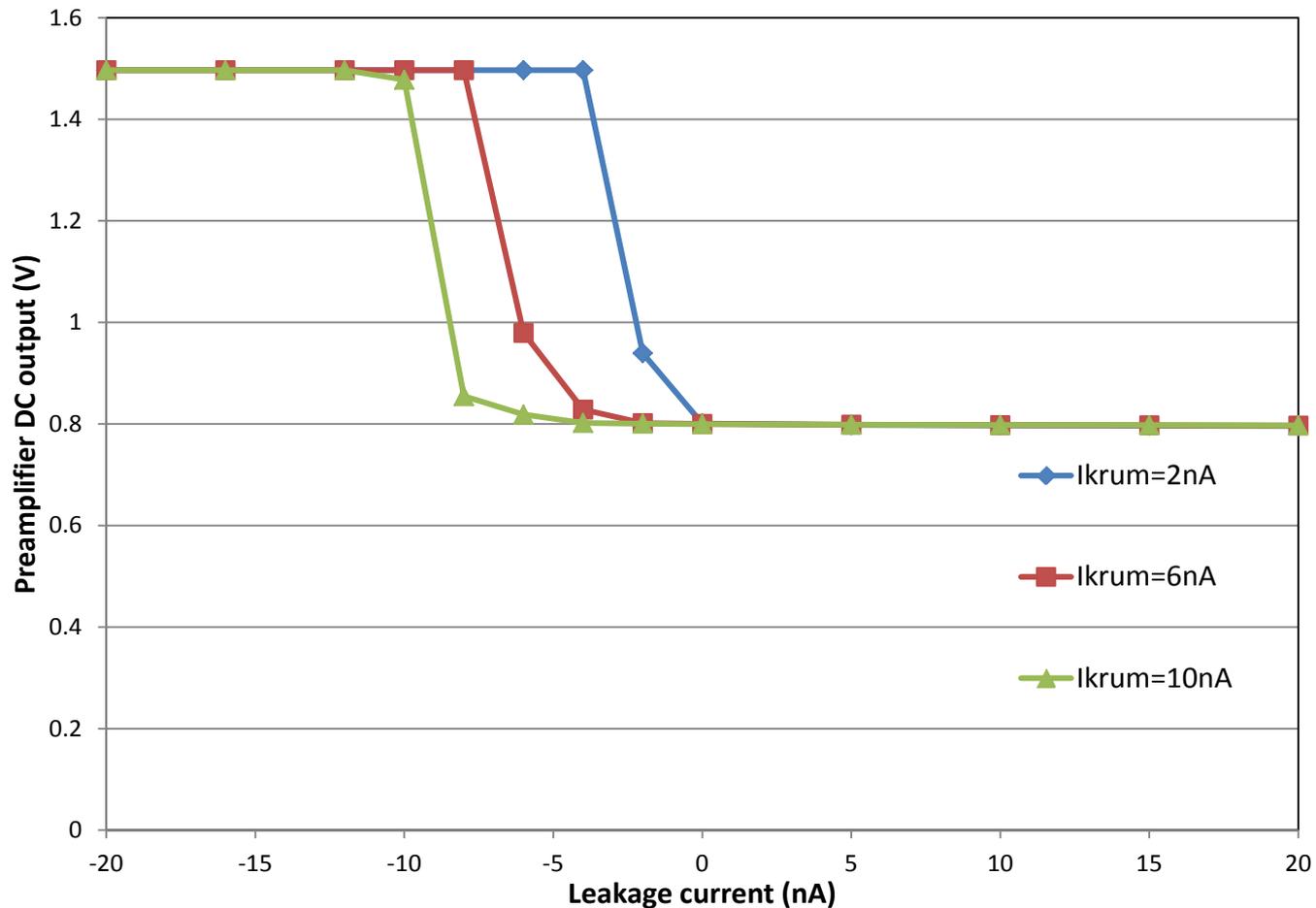


Preamplifier in saturation for input charges $>15\text{ke}^-$.

Preamplifier + leakage compensation

Krummenacher feedback:

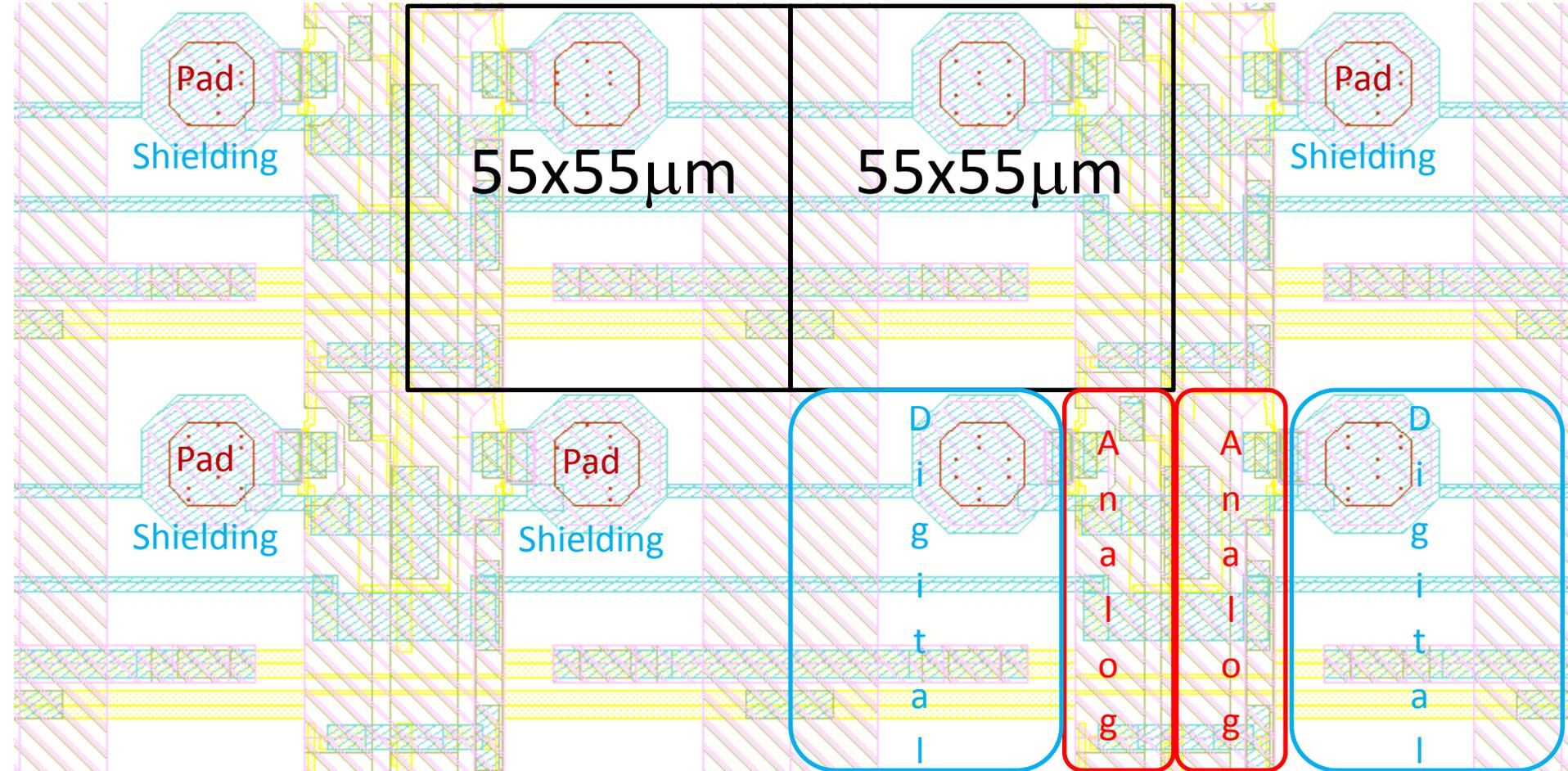
- Good compensation of positive leakage currents (holes)
- Compensation of electron currents depending on the available I_{krum} .



Noise coupling digital->analog

Limited area available: input pad on top of the digital pixel

Input pad: $12 \times 12 \mu\text{m}$ (was $20 \times 20 \mu\text{m}$ in previous chips)

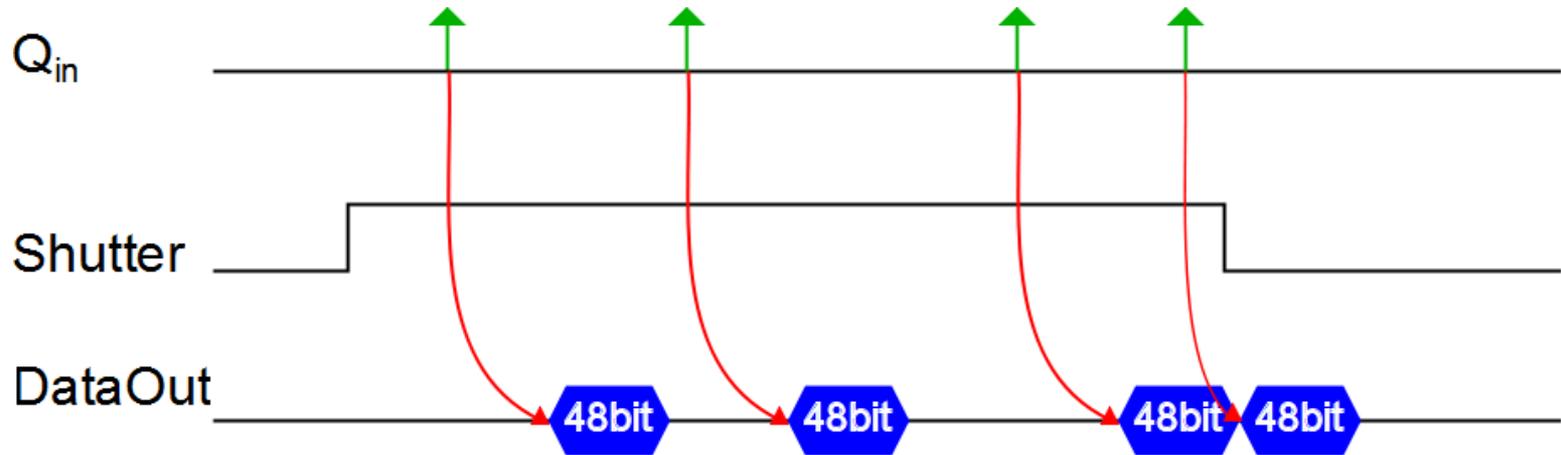


Studies and simulations have been carried out to quantify and minimize the noise injection into the sensitive analog nodes.

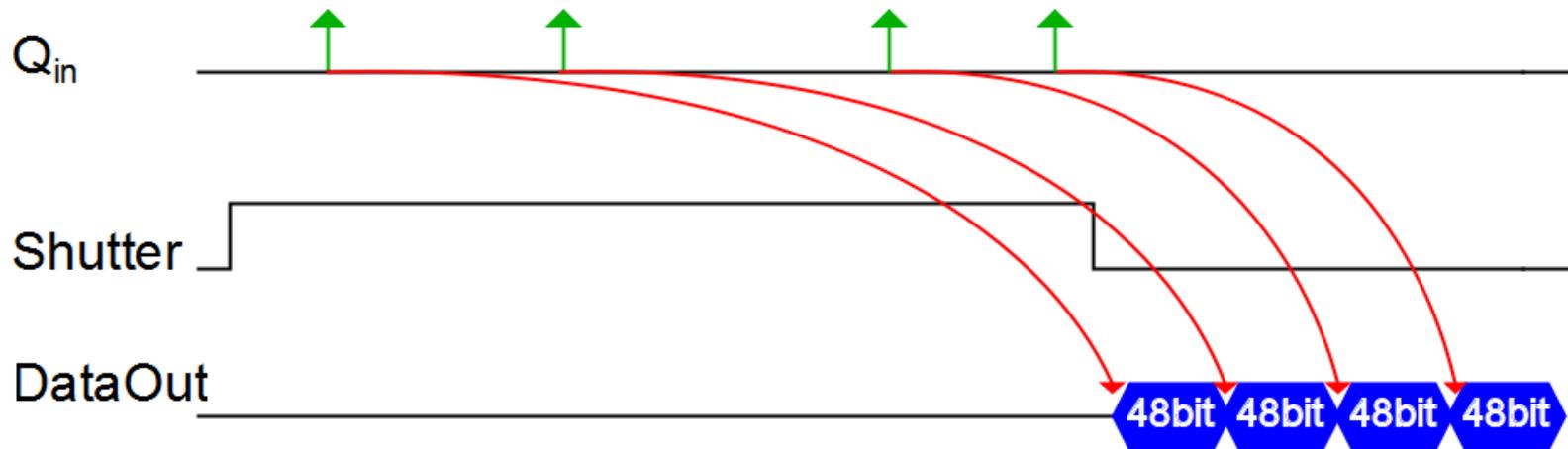
Timepix3: digital

- Digital pixels organized in double columns and superpixels 2x4 to optimize bandwidth.
- Simultaneous ToA & TOT measurement:
 - 10bit TOT@40MHz with pseudo-random encoding.
 - 14bit ToA@40MHz with Gray encoding.
- Photon Counting and integral TOT mode available:
 - 10bit PC with pseudo-random encoding.
 - 14bit iTOT with pseudo-random encoding.
- Using the VCOs → additional 4bit fine ToA@640MHz with binary encoding.
- 16 output phases of the PLL → delay clocks to the double columns in a staggered fashion.
- Packet-based readout with pixels active during readout: small readout associated dead-time of 375ns (for pixel data transfer into the SuperPixel)
→ Maximum dead-time free hit rate: 40Mhits/s /cm² (expected for randomly distributed hits).
- More information in these posters:
 - “Digital Column Readout Architectures for Hybrid Pixel Detector Readout Chips” by Tuomas Sakari Poikela.
 - “The Charge Pump PLL Clock Generator Designed for the 1.56 ns Bin Size Time-to-Digital Converter Pixel Array of Timepix3 Readout Chip” by Yunan Fu.

Timepix3: readout modes

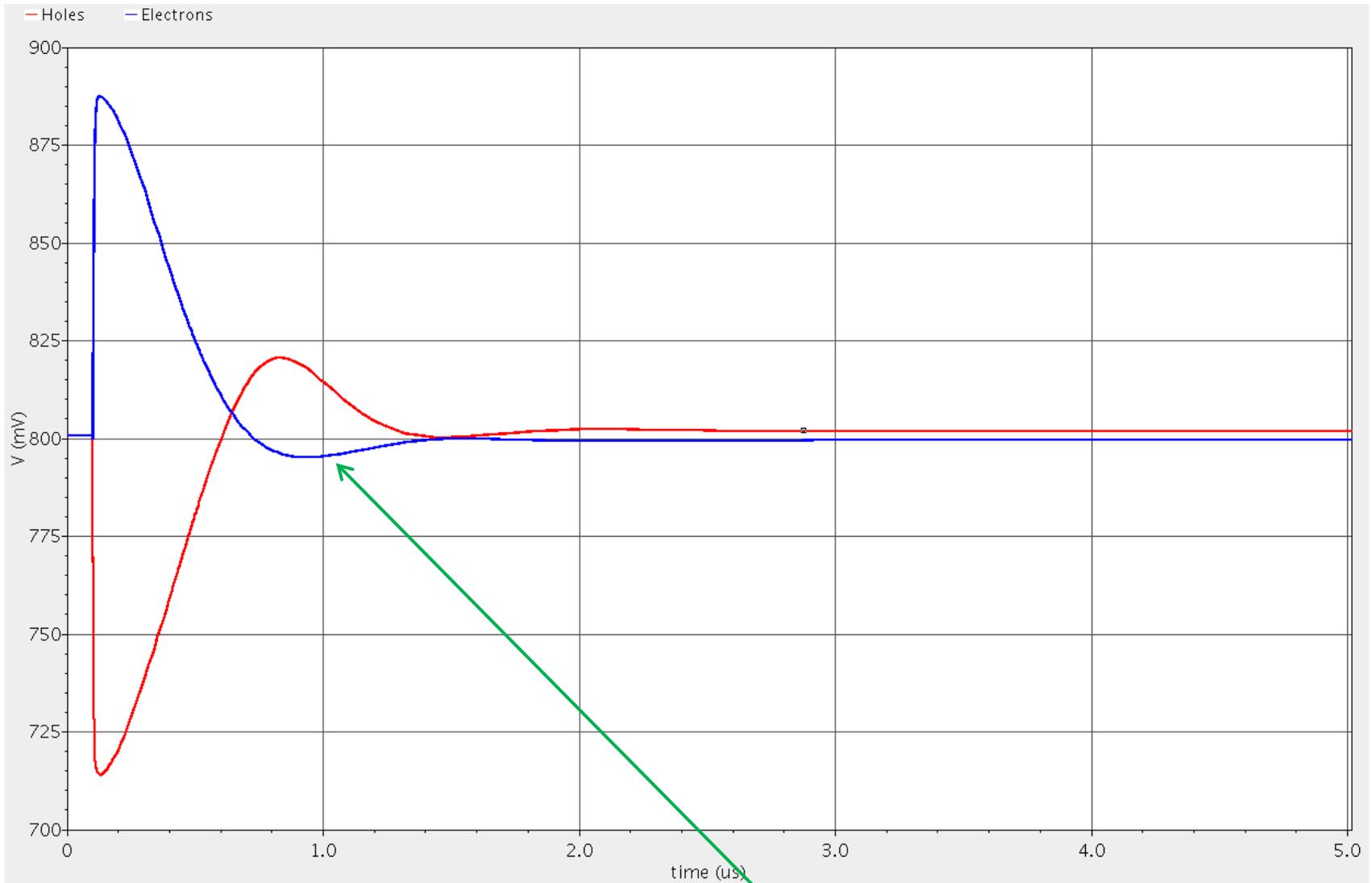


Data-driven readout mode.



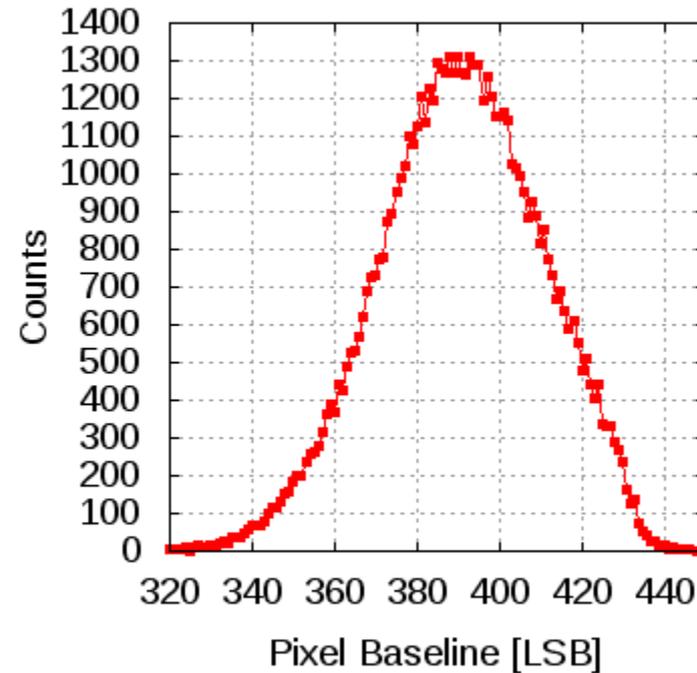
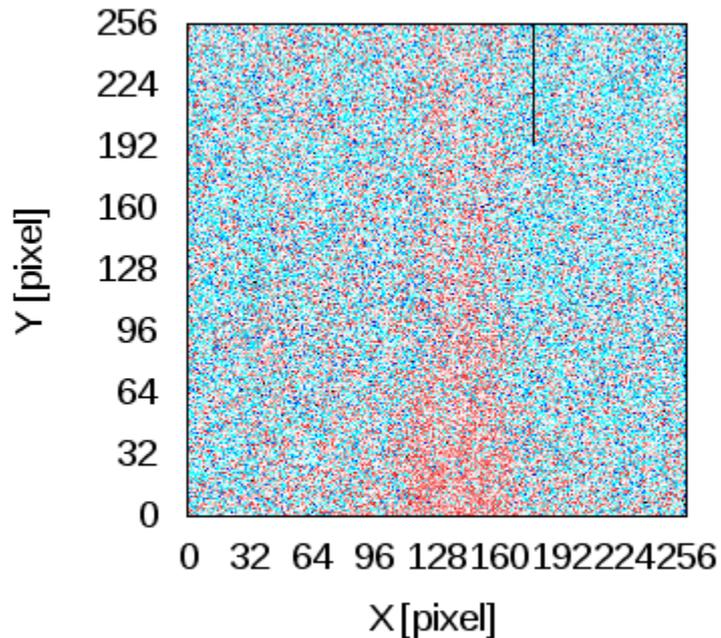
Sequential Read/Write mode.

Simulation with 1.7ke^- pulses



In simulation, we appreciate the different undershoots for electrons or holes.

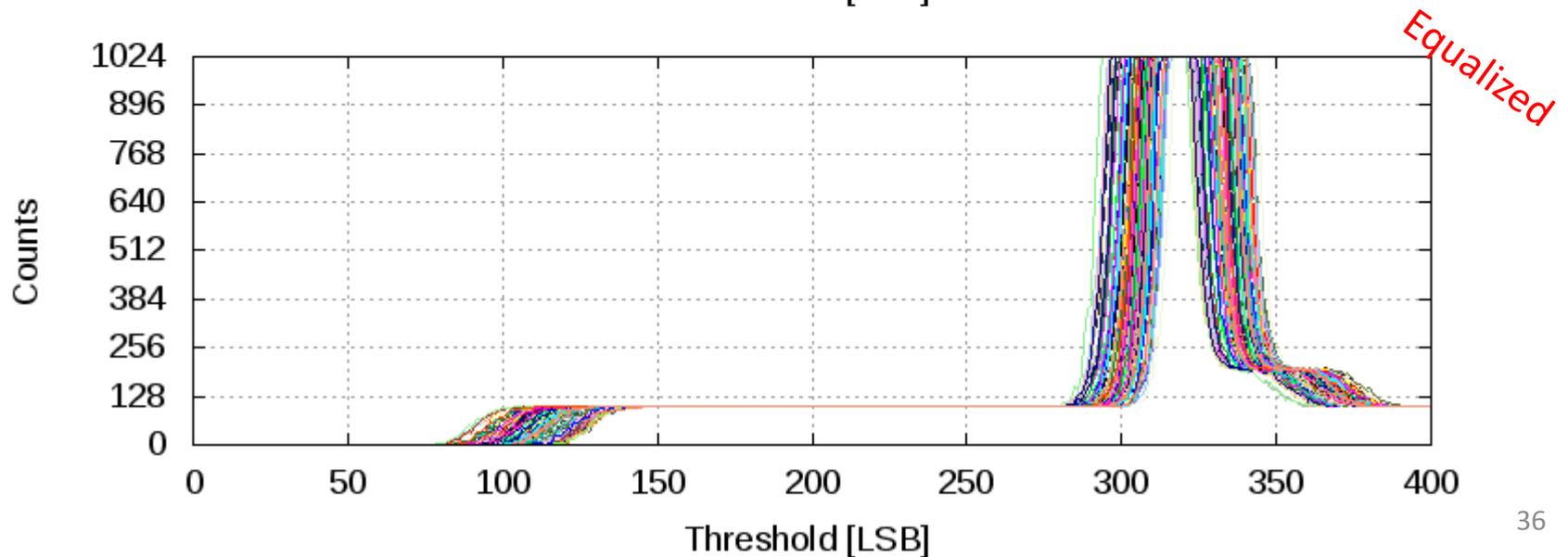
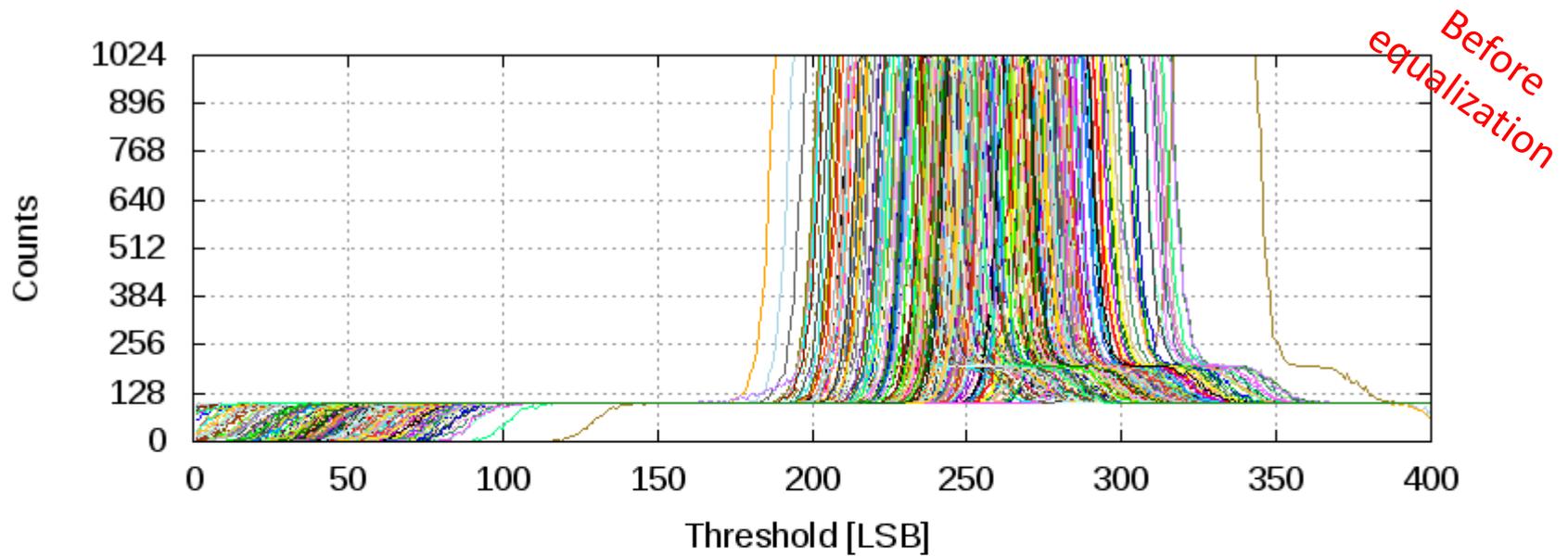
Uncalibrated baselines (DAC code 0xF)



Pixel-to-pixel baseline mismatch: $178e^-$ rms.

In simulation it was $160e^-$, but we know that for some components (compensation capacitors, gate-around transistors) the mismatch models are optimistic.

Overlapping all S-curves



Smallpix tentative floorplan 448x448

