Design of the analog front-end for the Timepix3 and Smallpix hybrid pixel detectors in 130nm CMOS technology

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Outline

• Introduction to Timepix3
• Front-end architecture
• Timepix3: first tests
• Smallpix
• Summary
**Timepix3**

### General features

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel #</td>
<td>256x256</td>
</tr>
<tr>
<td>Pixel size</td>
<td>55µm x 55µm</td>
</tr>
<tr>
<td>Design</td>
<td>CERN, NIKHEF, Bonn University</td>
</tr>
</tbody>
</table>

### Main applications

- Fast readout of solid-state pixelated sensors
- Readout of gaseous detectors (TPC)
- Vertex Locator for LHCb (further development into VELOpix)
- Power pulsing tests for the Linear Collider
- Dosimetry

### What’s new wrt Timepix1

- 2 main measurement modes:
  - simultaneous 10bit TOT and 18bit ToA
  - 10bit event counting and 14bit integral TOT
- TOT monotonic for large positive charges
- Fast ToA for time stamping with a precision of 1.56ns
- Data-driven readout: dead-time free, for a maximum hit rate of 40Mhits/s/cm²
- Shutdown/wake-up features for power pulsing tests on a full system
Timepix3: fast ToA measurement

40MHz clock always running (14bit ToA)
One 640MHz VCO per superpixel (2x4 pixels) active only when a discriminator fires (4bit fast ToA)

More information in these posters:

– “Digital Column Readout Architectures for Hybrid Pixel Detector Readout Chips” by Tuomas Sakari Poikela
– “The Charge Pump PLL Clock Generator Designed for the 1.56 ns Bin Size Time-to-Digital Converter Pixel Array of Timepix3 Readout Chip” by Yunan Fu
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The output of the discriminator is used to measure Time-Over-Threshold (proportional to the energy deposited in the pixel) and/or Time of Arrival (time stamping of the hit).
## Timepix3: front-end specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area</td>
<td>$55\mu m \times 13.5\mu m$</td>
<td></td>
</tr>
<tr>
<td>Signal polarity</td>
<td>Positive and negative</td>
<td></td>
</tr>
<tr>
<td>Detector capacitance</td>
<td>~$50fF$</td>
<td>25fF to 100fF</td>
</tr>
<tr>
<td>Leakage current</td>
<td>-5nA to +20nA</td>
<td></td>
</tr>
<tr>
<td>Amplitude linearity</td>
<td>Not required</td>
<td>Time measurement</td>
</tr>
<tr>
<td>TOT monotonicity</td>
<td>Yes, up to 300kh$^+$</td>
<td></td>
</tr>
<tr>
<td>ToA jitter and mismatch</td>
<td>Compatible with 1.56ns resolution</td>
<td>Gas detector applications</td>
</tr>
<tr>
<td>Time-to-peak</td>
<td>Target 25ns</td>
<td>In view of VELOpix</td>
</tr>
<tr>
<td>Noise + threshold mismatch</td>
<td>~$90e^-$</td>
<td>for a minimum threshold ~$500e^-$</td>
</tr>
<tr>
<td>Equalization DACs</td>
<td>4bit</td>
<td>Compensate pixel-to-pixel threshold mismatch</td>
</tr>
<tr>
<td>Power consumption</td>
<td>$12\mu W$/pixel</td>
<td></td>
</tr>
</tbody>
</table>
Timepix3: front-end architecture

PMOS diodes (TOT linearity)

Polarity switches

1.5V

2uA

V_{\text{threshold}}

Out_{\text{discr}}

2uA dyn

Preamplifier + Krummenacher feedback

Discriminator OTA + Equalization DAC (constant total current)

Discriminator 1\textsuperscript{st} stage

Discriminator 2\textsuperscript{nd} stage
# Timepix3: preamplifier

<table>
<thead>
<tr>
<th></th>
<th>Timepix</th>
<th>Timepix3</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Preamplifier</strong></td>
<td>Differential</td>
<td>Single-ended</td>
<td>More efficient power usage</td>
</tr>
<tr>
<td><strong>$C_{fb}$</strong></td>
<td>8fF</td>
<td>3fF</td>
<td>Larger gain</td>
</tr>
<tr>
<td><strong>Input pad size &amp; positioning</strong></td>
<td>20x20µm, over analog domain</td>
<td>12x12µm, over digital domain</td>
<td>Minimize parasitics, shielding to analog ground</td>
</tr>
</tbody>
</table>

![Diagram of the preamplifier circuit](Image)
TOT monotonicity

TOT monotonicity issue for large positive input charges:
$Q_{in} > 100k\mu$\text{A} $\rightarrow V(In) > V(NodeX) \rightarrow$ current through the wrong path

\[ \text{Added diode-connected PMOS transistors} \rightarrow \text{good current path} \]
Comparison between TOT with and without monotonicity PMOS diodes.
Fast ToA resolution

Time resolution of 1.56ns → low ToA jitter and mismatch

Pixel-to-pixel timing mismatch is simulated to be lower than 500ps for charges of 10ke⁻
Noise coupling digital->analog
Simulation models include wirebond parasitics, decoupling capacitors, resistances and parasitic capacitances of the metal lines running along the columns in the pixel matrix.
Noise coupling

Time (ns)

Preamplifier Output (V)

0.3

0.4

0.5

0.6

0.7

0.8

0.9

80 90 100 110 120 130 140 150 160 170 180

Discriminator output (V)

-0.2

-0.1

0.0

0.1

0.2

0.3

0.4

1.6

Threshold

Preamplifier no hit

Preamplifier hit

Discriminator no hit

Discriminator hit
Power pulsing

Analog domain:
switch dynamically between nominal and shutdown bias currents

Digital domain:
gate the clock to the pixel array

Transition times programmable between 800ns and 1.28ms
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Preliminary test results

2 chips under test since beginning of September

- Periphery tested at 95%, no issues detected
- Data readout functional at full speed (640MHz)
- Current consumption:
  - Analog 450mA
  - Digital 370mA (in data driven mode and no pulses injected)

Credits:
Bas van der Heijden, Frans Schreuder, Henk Boterenbrood (NIKHEF)
Szymon Kulis (CERN)
for the SPIDR board, readout system and the plots in the next slides
**S-curves:** 100 pulses in Photon Counting + integral TOT mode

![Graph showing S-curves with thresholds for different counts (620e-, 1280e-, 1940e-) and a 100 counts plateau.]
Scan of a pixel equalization DAC

4bit equalization DAC shows very good linearity, as expected.

Noise 6.5LSB: $\sim 65e^{-}$ (better than 75e$^{-}$ expected), assuming 50mV/ke$^{-}$ gain.
Equalization results

Mismatch:

Before equalization: $178e^{-}$

Afterwards: $30e^{-}$
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<thead>
<tr>
<th>Applications</th>
<th>Notes</th>
<th>Goals</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vertex Detector</td>
<td></td>
<td>Decrease pixel size (40µm?) wrt Timepix3 and Medipix3</td>
<td>Still providing TOT and ToA</td>
</tr>
<tr>
<td>Dosimetry</td>
<td></td>
<td>Array of 250k pixels (if possible)</td>
<td>Suitable to system tests, e.g. power pulsing</td>
</tr>
<tr>
<td>Imaging &amp; general purpose</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Main features foreseen today</th>
<th>Notes</th>
<th>Status</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full Through-Silicon-Vias (TSV) connectivity</td>
<td>Re-distribute periphery circuitry, active area approaching 100%</td>
<td>Reuse Timepix3 front-end</td>
<td>If it proves successful</td>
</tr>
<tr>
<td>Fast OR</td>
<td>Triggering capability</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data compression</td>
<td>Per pixel and per column</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Superpixels 2x2</td>
<td>Share resources, increase counters’ depth</td>
<td>Redesign of building blocks (bandgap, ESD protections, ...)</td>
<td>Needed for TSV compatibility</td>
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• Front-end designed and fabricated in the full-scale Timepix3 chip.

• Tests recently started. So far it looks functional:
  - Power ok
  - Noise 65$e^-$ good
  - Mismatch 30$e^-$ ok
  - Noise + mismatch = $\sim 71e^-$: minimum threshold around 430$e^-$?
  - These are preliminary measurements!

• If no major issue shows up, this front-end can be re-used for the Smallpix chip. Layout to be modified to accommodate in a different form factor.
Thanks for your time and attention!

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Massimiliano De Gaspari for the CERN Medipix team:
Jerome Alozy, Rafael Ballabriga, Michael Campbell, Erik Fröjdh, John Idarraga, Szymon Kulis, Xavier Llopart, Tuomas Poikela, Pierpaolo Valerio, Winnie Wong.
Outline

• Back up slides
Timepix3: floorplan

256x256 pixels (55umx55um)

14.1mm x 14.1mm x 2.1mm
Examples: preamplifier output

Preamplifier in saturation for input charges >15ke⁻.
Preamplifier + leakage compensation

Krummenacher feedback:
- Good compensation of positive leakage currents (holes)
- Compensation of electron currents depending on the available $I_{krum}$.
Noise coupling digital->analog

Limited area available: input pad on top of the digital pixel
Input pad: 12x12µm (was 20x20µm in previous chips)

Studies and simulations have been carried out to quantify and minimize the noise injection into the sensitive analog nodes.
Timepix3: digital

- Digital pixels organized in double columns and superpixels 2x4 to optimize bandwidth.
- Simultaneous ToA & TOT measurement:
  - 10bit TOT@40MHz with pseudo-random encoding.
  - 14bit ToA@40MHz with Gray encoding.
- Photon Counting and integral TOT mode available:
  - 10bit PC with pseudo-random encoding.
  - 14bit iTOT with pseudo-random encoding.
- Using the VCOs → additional 4bit fine ToA@640MHz with binary encoding.
- 16 output phases of the PLL → delay clocks to the double columns in a staggered fashion.
- Packet-based readout with pixels active during readout: small readout associated dead-time of 375ns (for pixel data transfer into the SuperPixel)
→ Maximum dead-time free hit rate: 40Mhits/s /cm² (expected for randomly distributed hits).
- More information in these posters:
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  - “The Charge Pump PLL Clock Generator Designed for the 1.56 ns Bin Size Time-to-Digital Converter Pixel Array of Timepix3 Readout Chip” by Yunan Fu.
Timepix3: readout modes

Data-driven readout mode.

Sequential Read/Write mode.
In simulation, we appreciate the different undershoots for electrons or holes.
Uncalibrated baselines (DAC code 0xF)

Pixel-to-pixel baseline mismatch: 178e⁻ rms.
In simulation it was 160e⁻, but we know that for some components (compensation capacitors, gate-around transistors) the mismatch models are optimistic.
Overlapping all S-curves
Smallpix tentative floorplan 448x448

Readout cells:
448x38um = 17.024mm

Distributed periphery:
7x256um = 1.792mm

Total height:
18.816mm