Upgrades to the ATLAS Level-1 Calorimeter Trigger

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Planned upgrades for ATLAS L1Calo

- LS1 (2013-2014)
  - Upgrade digital filter and bunch-crossing ID system to FPGAs (not covered in this talk)
  - Add **topology processing** capability at Level-1
- LS2 (2018)
  - New subsystems (**Feature Extractors, or FEX**) to perform egamma/tau/jet identification with higher granularity calorimeter data

Topology processing

- Current L1Calo system produces topology information
  - Sent only to high-level trigger

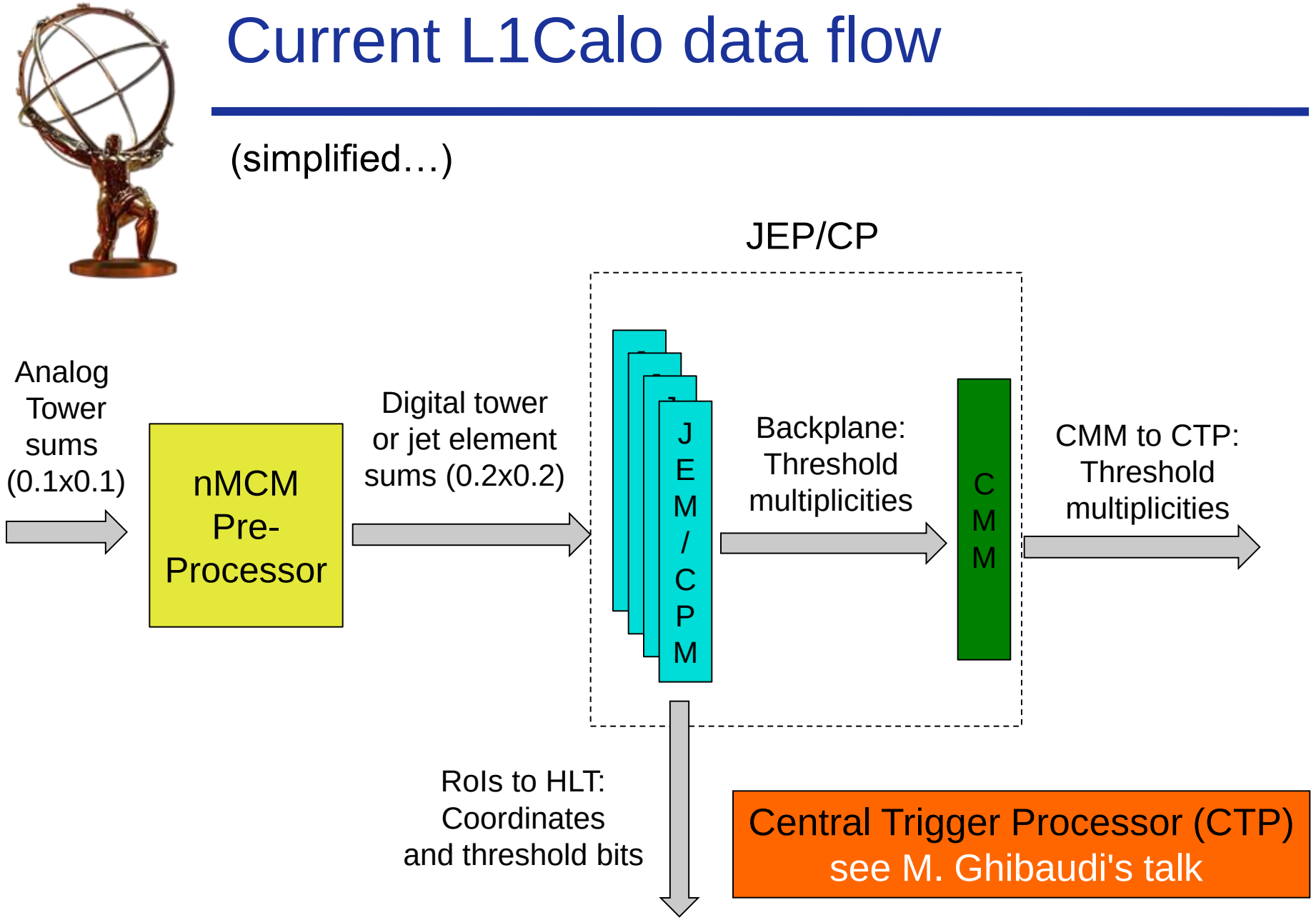
  (Regions of Interest, RoI)
  - L1 decision only uses object multiplicity

- Expect luminosity increase up to 2x design after LS1
  - nMCM provides better pile-up suppression
  - Cannot significantly improve Jet/egamma/Tau identification before LS2
  - Adding topology to L1 is the only major improvement available until then

Solution: Upgrade L1 real time data path to include **topology information**

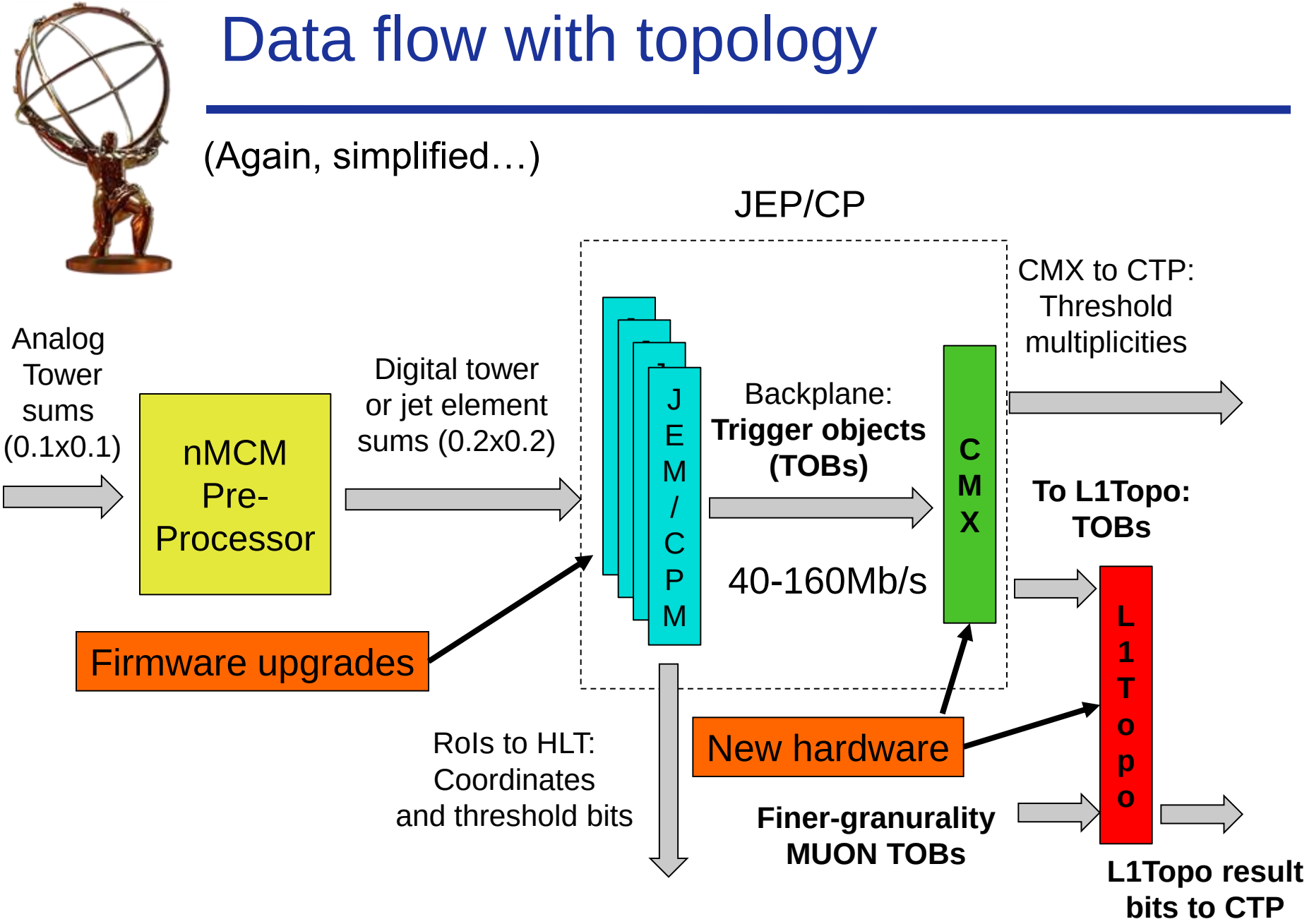
Current L1Calo data flow

(simplified…)



Data flow with topology

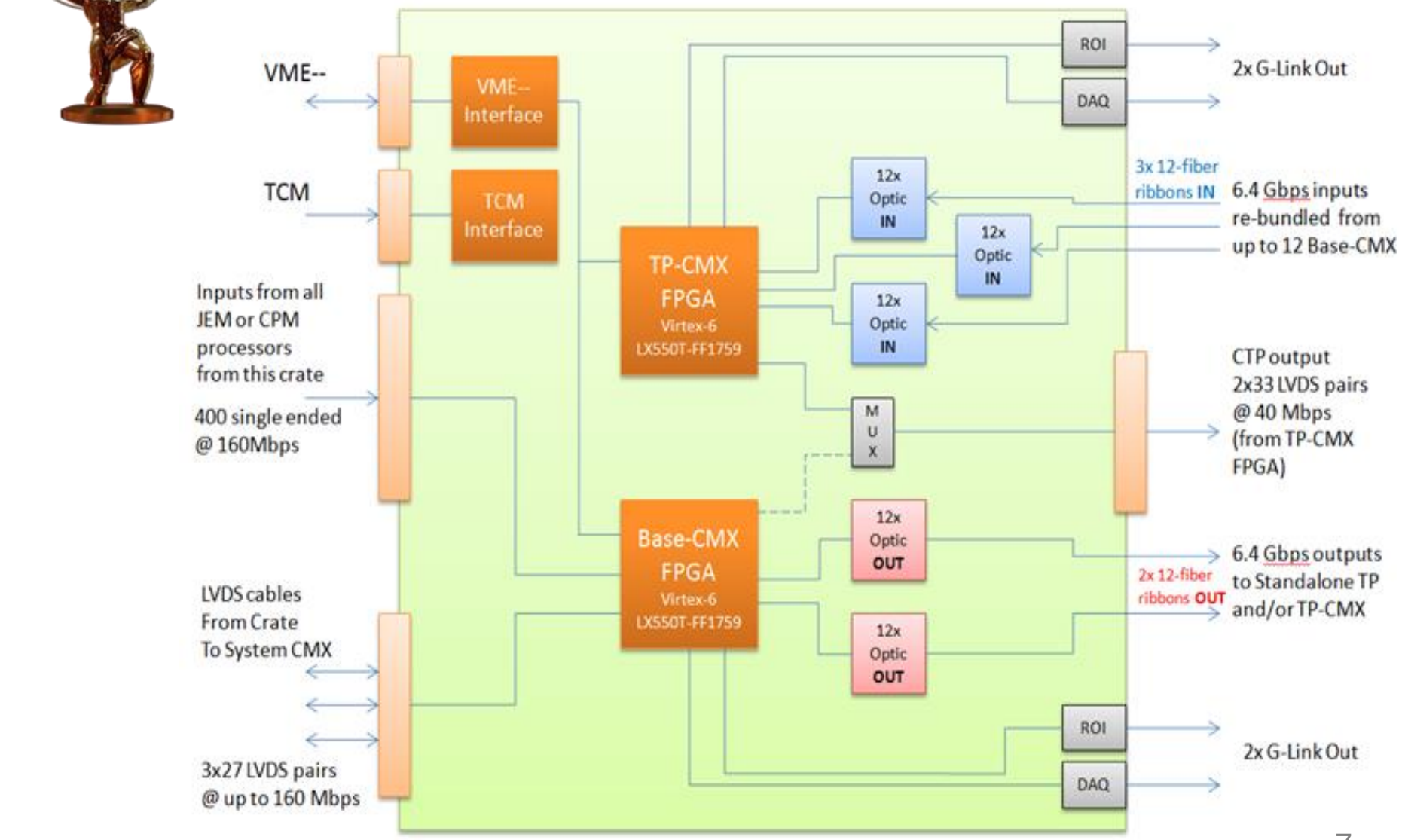
(Again, simplified…)



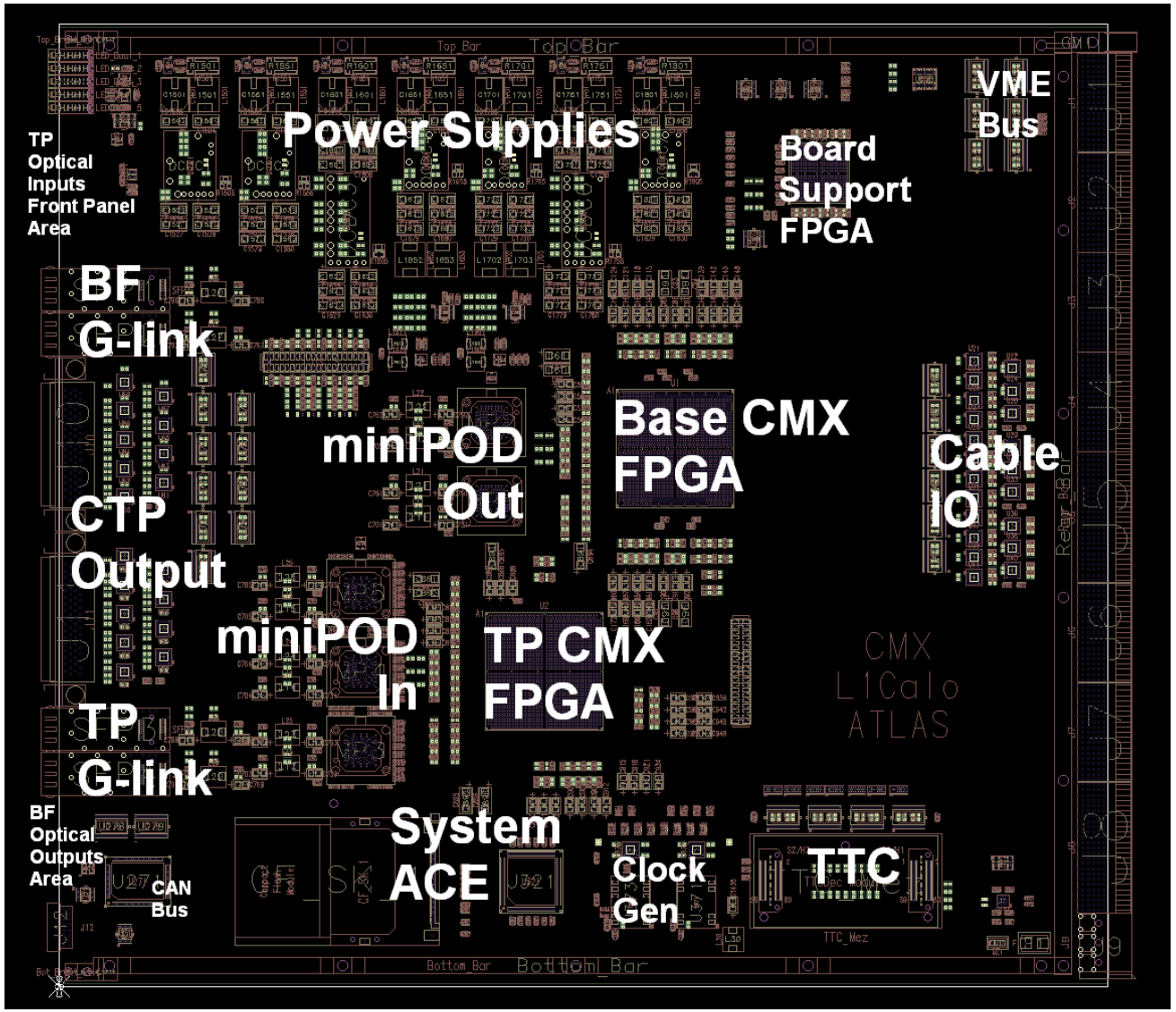
L1Calo CMX

- Full backward-compatibility with CMM
- Upgrade with higher capacity
- Inputs from JEM/CPM (40-160Mb/s)
  - Crate → System merging cables (40-160Mb/s)
  - Output to CTP
  - 40 Mbit/s (possible future upgrade to 80Mb/s)
- New functionality
  - High-speed optical transmission of TOBs to L1Topo
  - Up to 24 output fibers at 6.4Gb/s
  - Limited topology processing capability
    - Separate V6 FPGA
    - Up to 36 input fibers at 6.4Gb/s
    - Can be used as backup/supplement for L1Topo if needed

L1Calo CMX

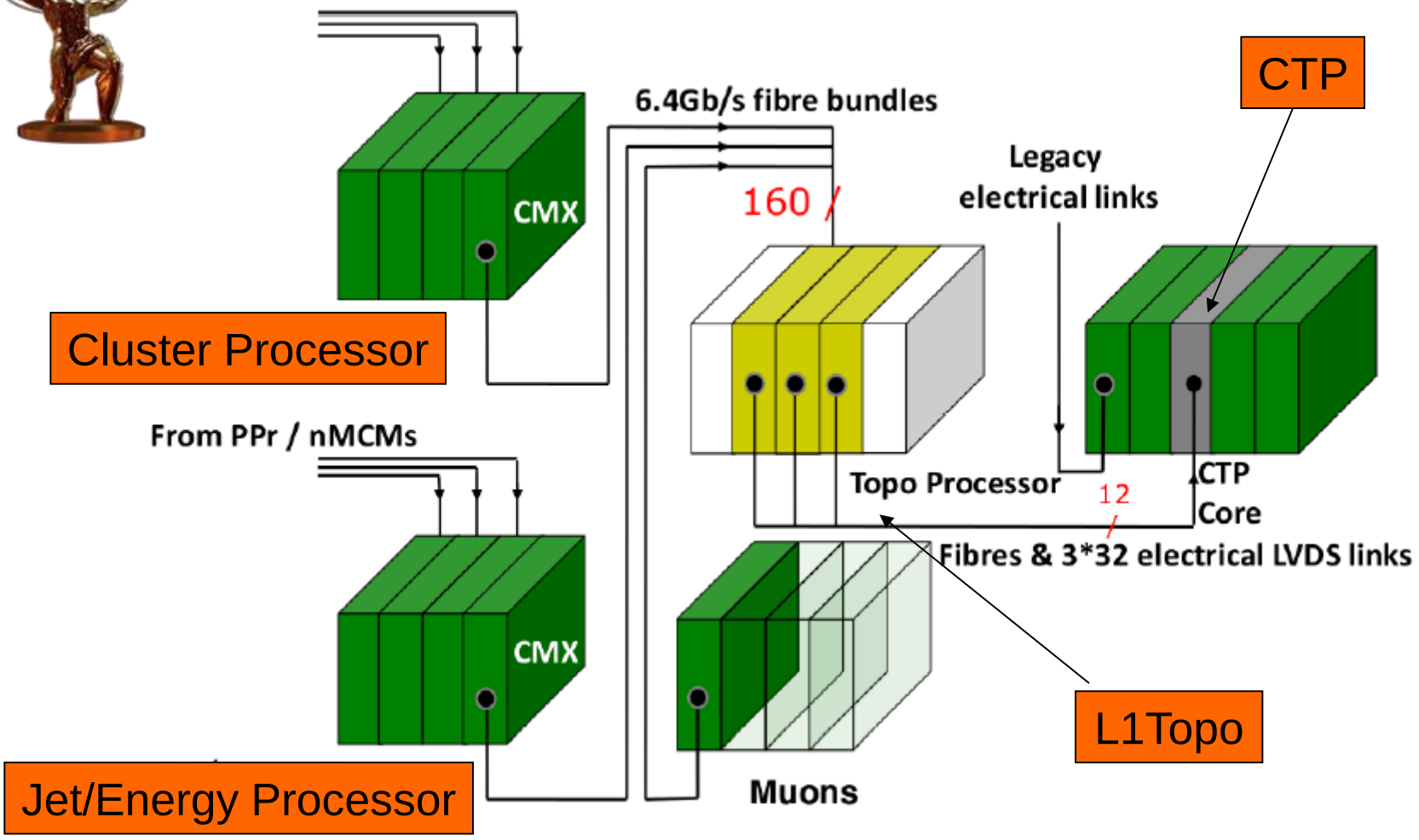

VME--
VME-- Interface
TCM
TCM Interface
Inputs from all JEM or CPM processors from this crate
400 single ended @ 160Mbps
LVDS cables From Crate To System CMX
3x27 LVDS pairs @ up to 160 Mbps
TP-CMX FPGA
Virtex-6 LX550T-FF1759
Base-CMX FPGA
Virtex-6 LX550T-FF1759
ROI
DAQ
12x Optic IN
12x Optic IN
12x Optic IN
3x 12-fiber ribbons IN
6.4 Gbps inputs re-bundled from up to 12 Base-CMX
2x G-Link Out
M U X
CTP output 2x33 LVDS pairs @ 40 Mbps (from TP-CMX FPGA)
12x Optic OUT
12x Optic OUT
2x 12-fiber ribbons OUT
6.4 Gbps outputs to Standalone TP and/or TP-CMX
ROI
DAQ
2x G-Link Out

CMX Layout



Prototype Submitted

L1Topo real-time data path



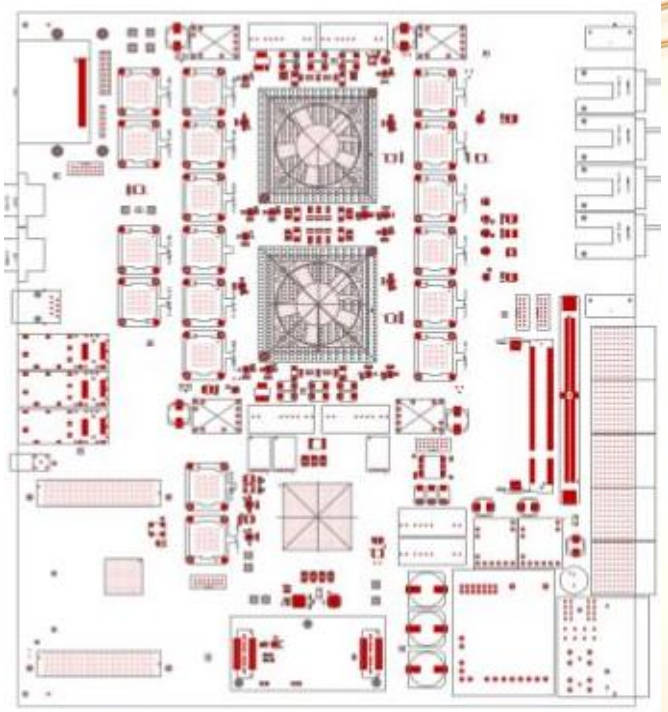
L1Topo requirements

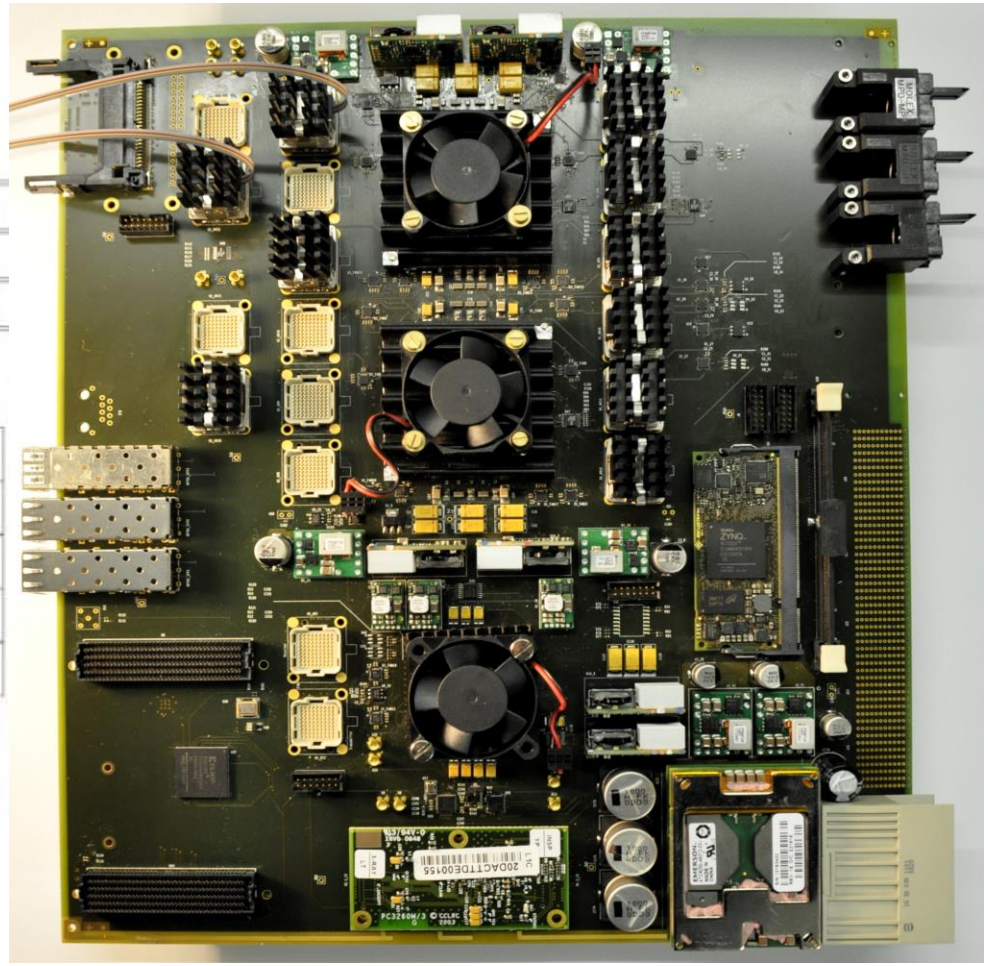
- High-speed optical input links
  - Accept TOBs from many sources
    - JEP/CP CMXs (LS1)
    - L1Muon
      - (Coarse in LS1, finer granularity in LS2)
    - eFEX, jFEX (LS2)
- Large amounts of programmable logic
  - Large TOB sort trees
  - Many topo algorithms running in parallel
- Sufficient output bits CTP
  - High-bandwidth output, with time multiplexing
- Scalable
  - Can add multiple modules running in parallel to provide additional logic for algorithm processing

L1Topo module

- High density 12-channel optical receivers (miniPODs)
  - Parallel fiber bundles from CMX, L1Muon, etc.
- Two high-end processors (Virtex – 7)
  - Total of 160 input fiber links
  - 238 parallel links between FPGAs for partial data sharing
- Both fiber-bundle and low latency LVDS outputs into CTPcore

L1Topo prototype





LS2 architecture

Muon detector

Digital Liquid Argon Calorimeter data

Analog trigger tower sums from calorimeters

Barrel sector logic

Muon Trigger

MuCTPi

Endcap sector logic

Feature extractors

FIne granularity

eFEX

DPS

jFEX

Coarse granularity

Central Trigger

L1Topo

CTP

C O R E

L1 accept

PreProcessor

CP

C M X

nMCM

JEP

JEM

C M X

L1Calo Trigger

Hadronic layer

Outputs to CTP

New/upgraded Hardware

TOBs

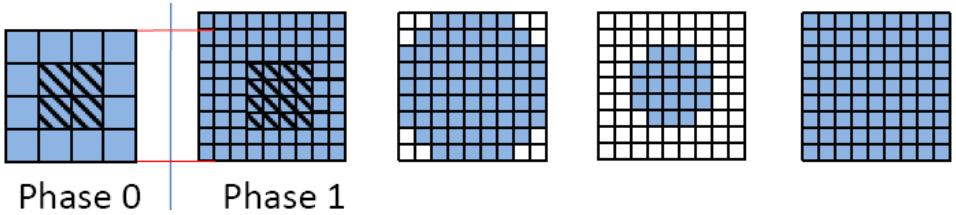
TOBs from eFEX and jFEX, finer-granurality MUON TOBs from upgraded MUCTPI

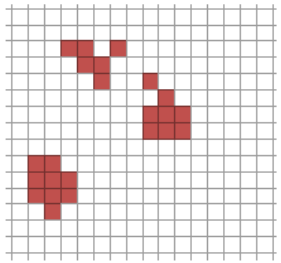
L1Calo LS2 upgrade

- Motivation
  - For post-LS2 running (2018), Lumi $>2.0 \cdot 10^{34} cm^{-2} s^{-1}$
  - Total trigger rate $\leq$ 100kHz
  - Trigger thresholds, the same level to maintain physics sensitivity to electroweak processes
- Constraints
  - LS2 upgrade has to stay within current level-1 latency envelope ~2.5μs.
  - Forward compatible with future upgrade (2022)
- Strategy
  - Using higher granularity trigger towers (digitised on detector), both laterally and in depth
  - Higher granularity allow better identification for egamma/tau/jet objects and improves energy resolution
  - Physics performance studies based on simulations give encouraging results

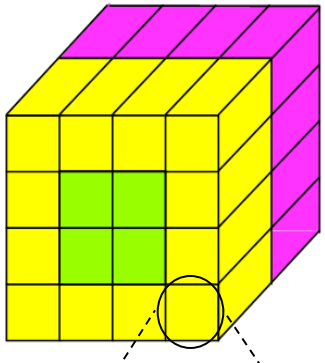
FEX calculations

Towers ROIs environment

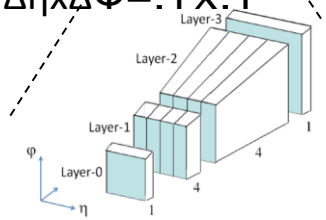




Current algorithm window



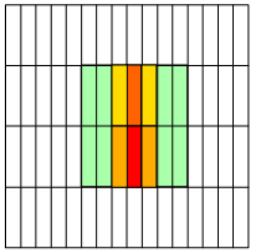
ΔηxΔΦ=.1x.1



LAr Supercell structure

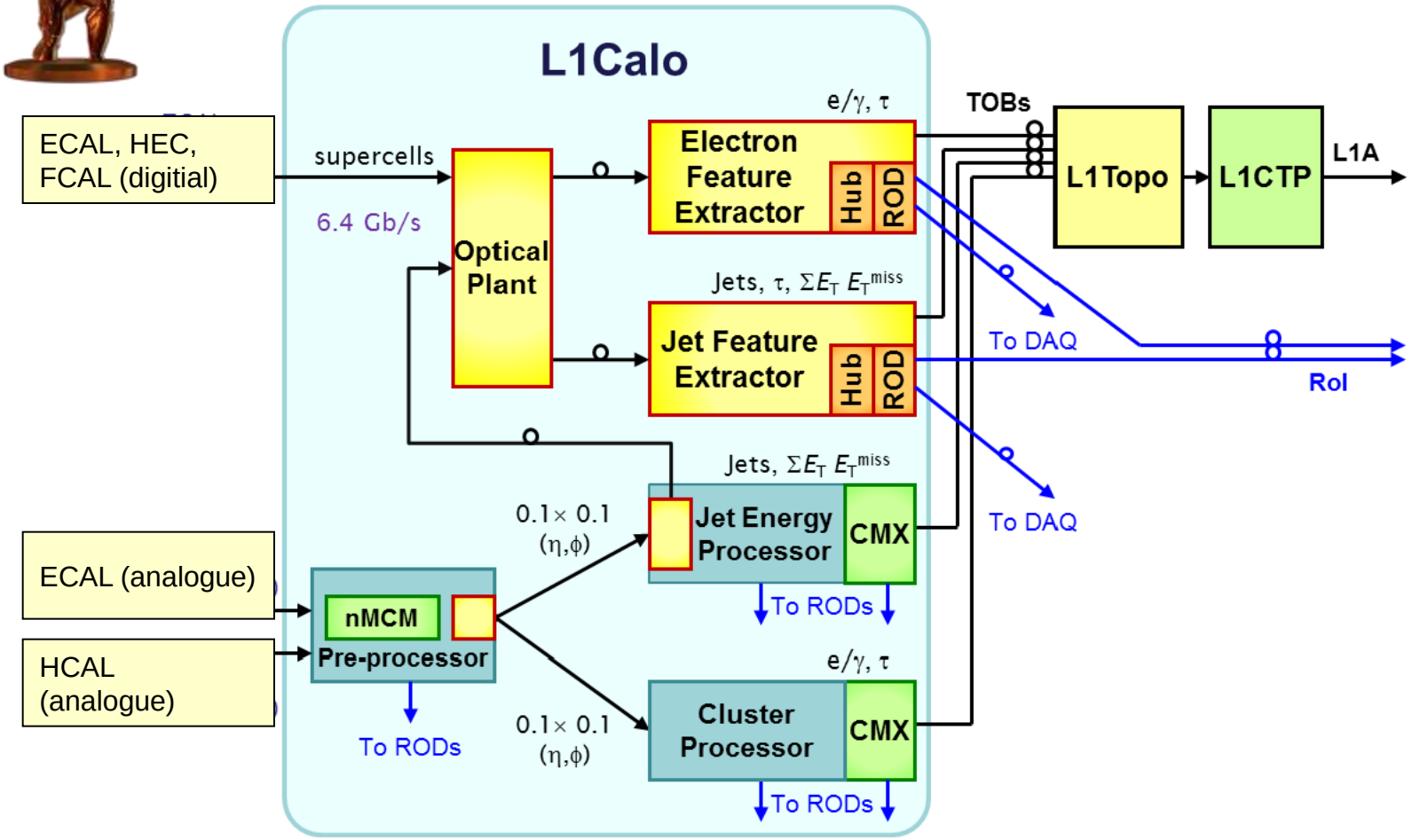
Motivation: improve e/jet identification power 'new Rcore algorithm' -> calculate shower width in middle layer

New Rcore algorithm
Operates on middle layer



ΔηxΔΦ=.025x.1

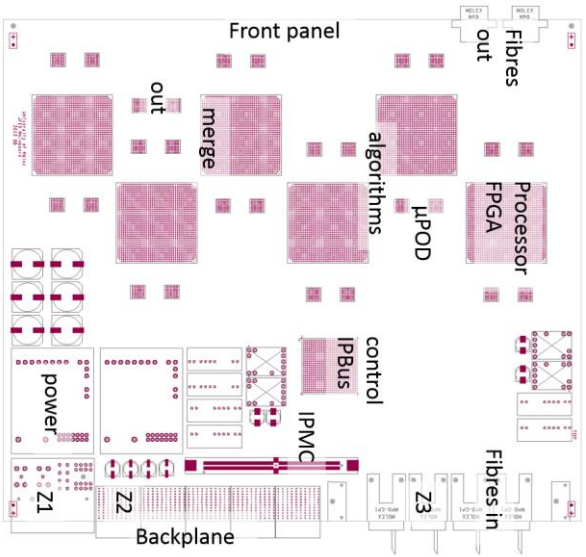
L1Calo at LS2

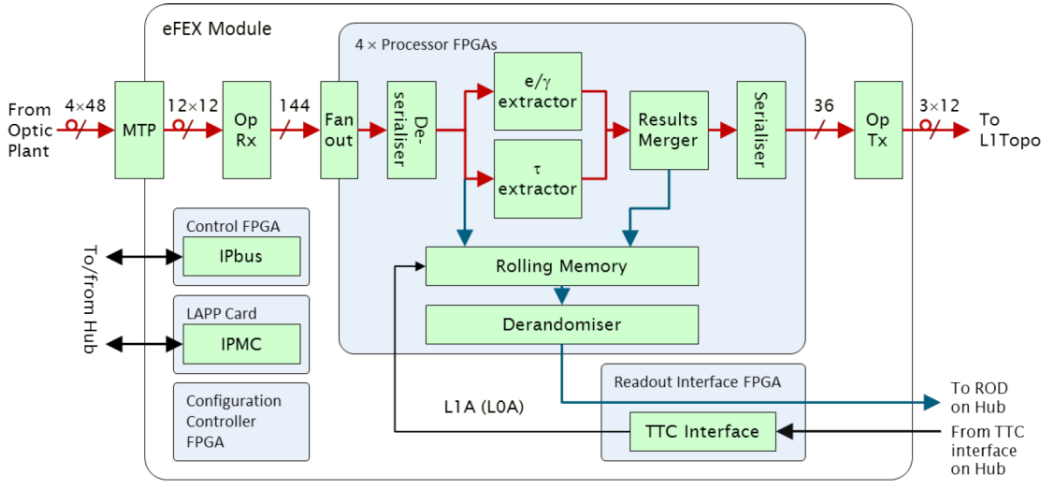


eFEX and jFEX module

- jFEX characteristics
- 288 input optical fibres
- 24 output fibers
- 6.4Gb/s (baseline)
- MicroPOD
- 6 big FPGAs per module
- ATCA based

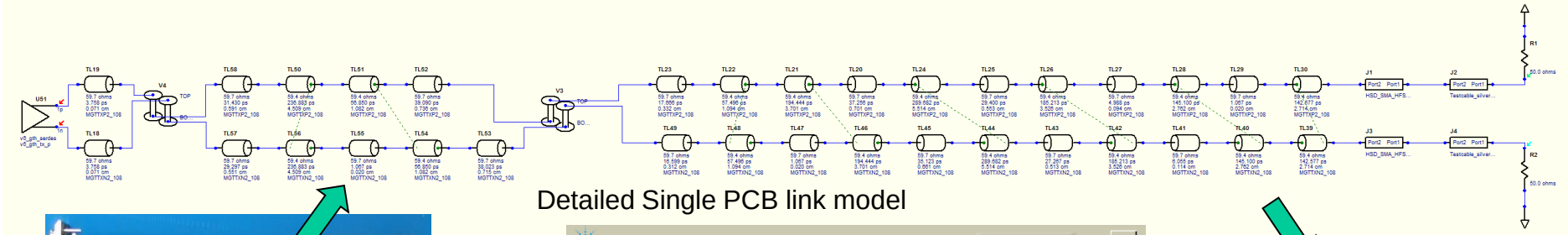
- eFEX characteristics
- 144 input optical links
- 36 output optical links
- 6.4Gbps (baseline)
- MiniPOD
- 4 big FPGAs per module
- ATCA based



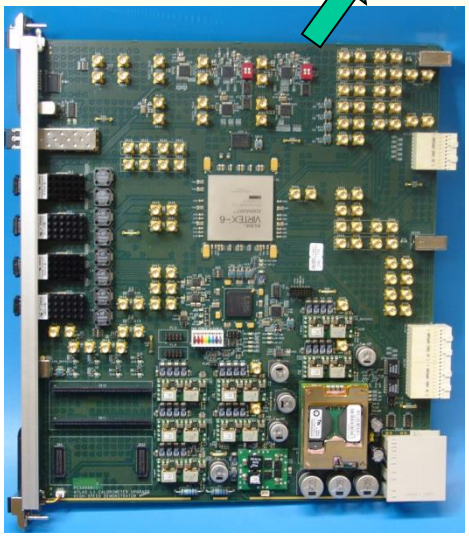


High speed link simulation

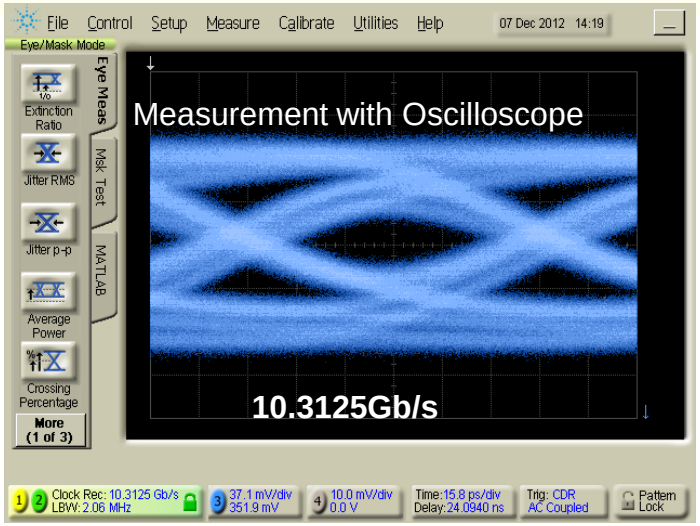
- Very good correlation between hardware measurement and PCB simulation achieved @ 10Gb/s
  - RAL high speed demonstrator with Virtex-6 GTH

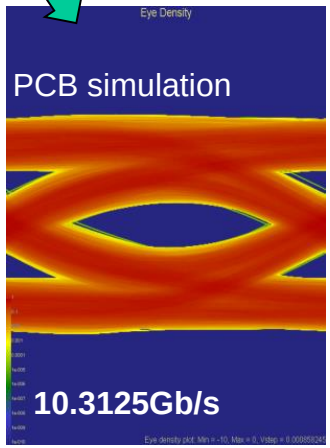


Detailed Single PCB link model



RAL High-speed Demonstrator

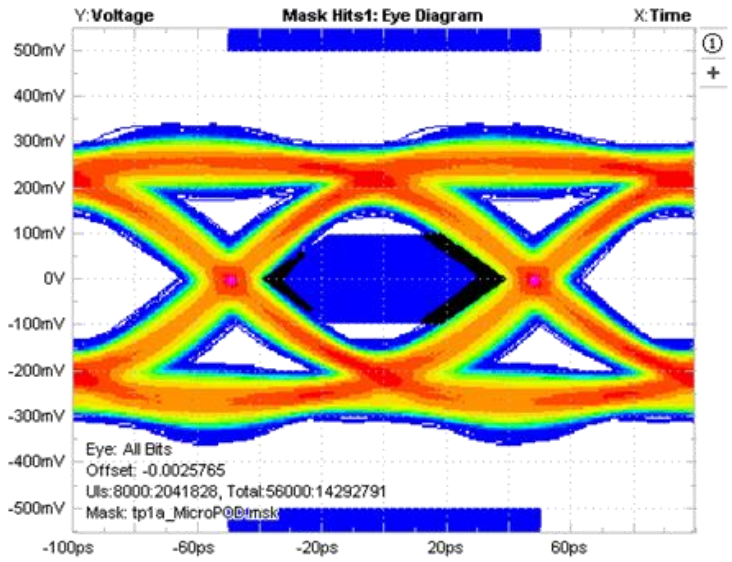




High speed link test

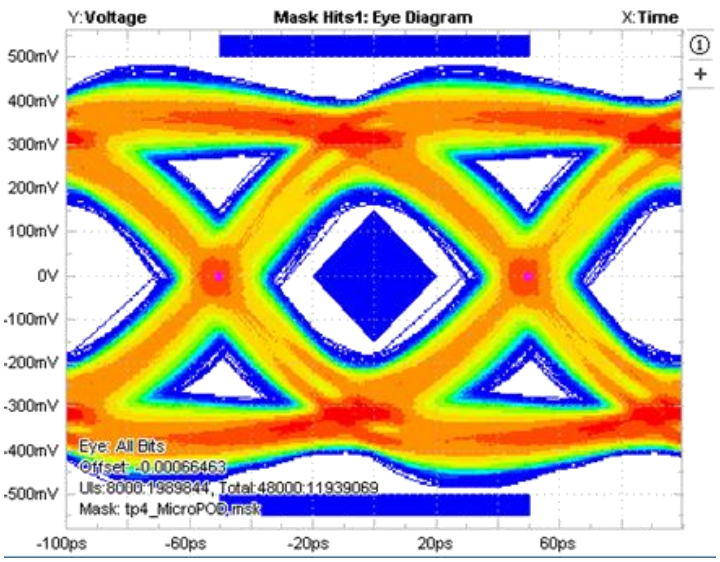
- Eye measurement @ 10Gb/s
  - Virtex-7 GTH + MicroPOD, joint BNL/RAL test

TP1



Pass, mask hit ratio 4.4x10E-5

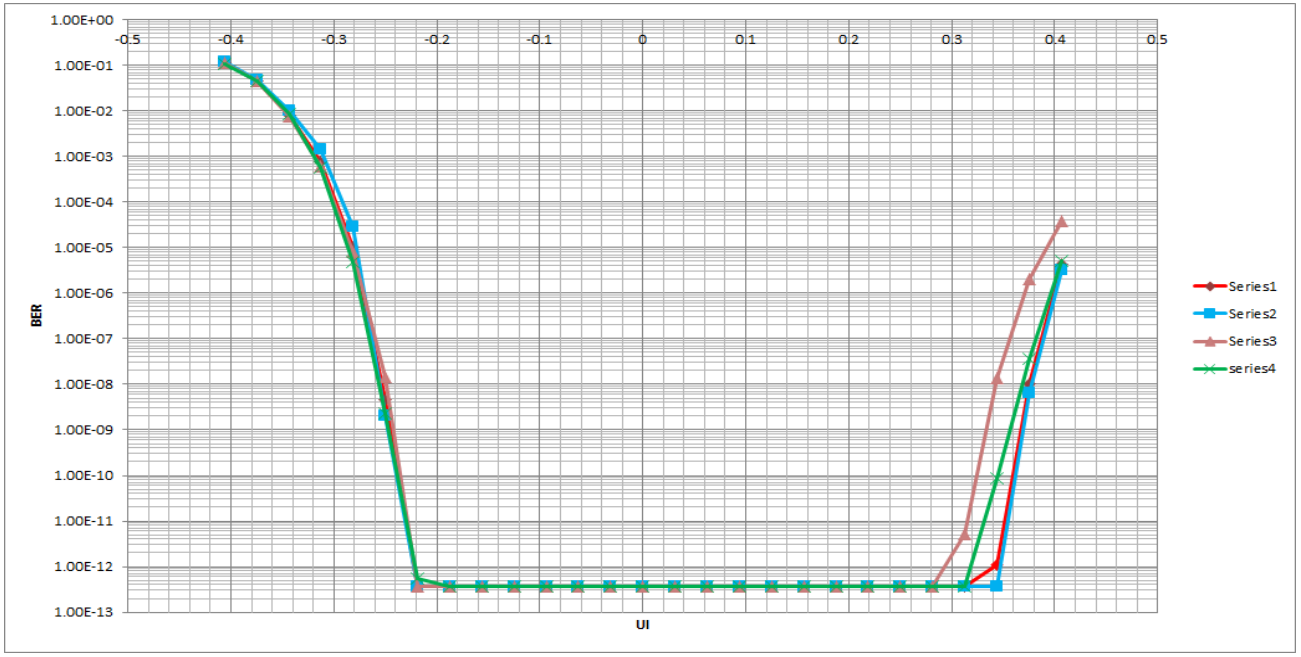
TP4



Pass, mask hit ratio 0

High speed link test

- Bit Error Rate measurement @ 10Gb/s
  - Virtex-7 GTH + MicroPOD, joint BNL/RAL test
  - ~50% margin @ 10E-12, excellent



Conclusions

- L1Calo on course for adding topology capabilities over LS1
  - CMX and L1Topo on schedule for installation and commissioning by end of 2014
- Designed with LS2 requirements in mind
  - Large number of high-speed input links
  - Large processor FPGAs
  - Scalable as needed
  - Room to receive TOBs from eFEX, JFEX and upgraded MUCTPI
- The FEX architecture is well understood and defined for ATLAS Level-1 Calorimeter Trigger Upgrade for phase-I
- Module specifications are on the way
- High-speed link tests achieved very encouraging results at 10Gb/s line rate
- High-speed PCB simulation achieved good correlations with hardware measurement at 10Gb/s line rate