Contribution ID: **33** Type: **Oral**

Real-time Topology Processing in the ATLAS Level-1 Calorimeter Trigger

Wednesday, 25 September 2013 11:35 (25 minutes)

In 2015 the Large Hadron Collider will run with increased center-of-mass energy and luminosity. To maintain trigger efficiency against increased pileup rates, event topology information will be added to the ATLAS Level-1 real time data path and processed by a new Topology Processor (L1Topo). In phase-I, a new digital readout for the Liquid Argon calorimeters will provide finer granularity and depth segmentation in the electromagnetic layer to new Level-1 feature extractors (FEX) for improved EM, tau and jet identification. We present the topology and phase-I trigger upgrades to the ATLAS Level-1 trigger.

Summary

Luminosity upgrades to the LHC will mean that the ATLAS Level-1 trigger must deal with higher pileup while maintaining manageable trigger rates and high efficiency. Over the 2013-14 shutdown, firmware and hardware upgrades to the existing Level-1 Calorimeter Trigger (L1Calo) will add object coordinates and ET to the real time data path, and a new topology processor (L1Topo) will be added to Level-1. EM and hadronic tower sums are received in L1Calo by the Preprocessor, which in turn feeds two parallel processor subsystems the Jet/Energy-sum Processor (JEM) and Cluster Processor (CP). Jets and EM/hadronic clusters are identified by Jet/Energy-sum modules (JEMs) or Cluster Processor modules (CPMs), respectively. Common Merger Modules (CMMs) receive CPM/JEM results over backplane links and produce system-wide results. The upgrade to L1Calo includes upgraded CPM and JEM firmware to send trigger object data across the backplane at increased data rates. The current CMMs will be replaced by new "CMX"modules capable of receiving and processing the high-speed backplane data, and sending them over high-speed optical links to a new topological processor (L1Topo) subsystem. L1Topo will be capable of performing geometrical cuts and correlations, as well as calculate such complex observables as invariant mass. Real-time L1Topo output will be sent to the Central Trigger Processor CTP, where the final Level-1 accept decision is taken. In addition to the L1Topo architecture, we present crucial aspects of topology algorithm development, including optimal bandwidth, FPGA resources and latency.

At phase-I in 2018, the luminosity of LHC will be increased to ˜ 3 × 1034cm-2s-1. To improve the ATLAS Level-1 Trigger performance at phase-I, changes are needed at both the ATLAS detector and the Level-1 Trigger system. New on-detector electronics, the digital Tower Builder Board, will be installed on the Liquid Argon Calorimeter to provide trigger higher-granularity calorimeter information. New algorithms running in additional hardware will be added to the existing Level-1 Trigger to process these data, which are expected to give the required trigger performance with higher LHC pileup of phase-I running. The new off-detector digital processing chain will consist of two subsystems: a Digital Processor System (DPS) will perform digital filtering on the new digital calorimeter data and a feature extractor subsystem with Electron and Jet processors (eFEX, jFEX) will identify calorimeter trigger signatures. The eFEX will be designed as a modular subsystem, housed in two ATCA crates and consisting of around 20 modules, each receiving data on about 200 optical fibres at 6-10 Gb/s. These input optical fibres will go through dense optical backplane connectors in the ATCA Zone-3 area and terminate on parallel embedded optical receivers near FPGAs on the main modules. Information describing objects identified by the FEX subsystems will be sent over optical fibres to a Topology Processor subsystem. We also present the motivation for architectural design choices, latest test results, and high-speed link simulations.

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Session Classification: Trigger

Track Classification: Trigger