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The CLARO-SiGe, a front-end ASIC for precise timing measurements at low power

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The CLARO-SiGe is a prototype ASIC for single photon counting with
pixellated photomultipliers, designed to sustain a high counting rate at low power.
Each channel is made of a charge amplifier to readout the current
pulses on a low impedance node and a discriminator with a settable
threshold to count the pulses above threshold.
The architecture of the whole channel is differential.
The threshold of the discriminator is set through a small current
injected through a dummy amplifier, which guarantees the simmetry of
the differential configuration.
Each channel has two discriminators which can be operated ad different speeds, in order to obtain the highest time resolution on the fast channel, while rejecting crosstalk signals thanks to the slower channel which is less sensisitive to crosstalk.
Counting rates up to 40 MHz can be sustained.
The overall power consumption is about 1 mW per channel.

Summary

The CLARO is an ASIC for single photon counting with pixellated
photomultipliers, designed to sustain a high counting rate at low
power.
It is primarily designed to readout multi-anode photomultipliers
(Ma-PMTs) in the upgraded LHCb RICH detectors.
The first 4 channel prototype, named CLARO-CMOS, was realized in a
0.35 CMOS technology, achieving a power consumption of about 1
mW/channel with counting rates up to 10 MHz.
A timing resolution down to 10 ps RMS for typical single photoelectron signals was demonstrated with the CLARO-CMOS on the test bench.
Another protoype was also designed in a 0.35 SiGe-CMOS technology,
named CLARO-SiGe.
Whereas the CLARO-CMOS has four channels, the CLARO-SiGe has only two channels. The main purpose of the design is to test the difference between the two technologies, namely the larger readout speed which can be achieved at the same power consumption with SiGe transistors with respect to 0.35 um MOS devices.
As in the case of the CLARO-CMOS, each channel is made of a charge
amplifier to readout the current pulses on a low impedance node and a discriminator with a settable threshold to count the pulses above
threshold.
From the point of view of channel architecture, the design features a number of improvements over the CLARO-CMOS.
The architecture of the whole channel is differential.
The threshold of the discriminator is set through a small current
injected through a dummy amplifier, which guarantees the simmetry of
the differential configuration.
The AC coupling between the amplifier and the discriminator which was present in the CLARO-CMOS was

also removed.
Each channel has two discriminators which can be operated ad different speeds, in order to obtain the highest time resolution on the fast channel, while rejecting crosstalk signals thanks to the slower channel which is immune to crosstalk.
Counting rates up to 40 MHz can be sustained.
The overall power consumption is about 1 mW per channel.

References:

CLARO-CMOS, a very low power ASIC for fast photon counting with
pixellated photodetectors
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