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Single event upsets in the readout control FPGA of the ALICE TPC detector during the first LHC running period

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This paper will present and discuss measurement results of single event upsets in the readout control FPGA of the ALICE Time Projection Chamber during the first LHC running period. The measurements have been performed during stable beam conditions for proton-proton, proton-lead and lead-lead collisions.

Summary

The use of programmable logic devices such as FPGAs is a very attractive solution for High Energy Physics applications. With the ability to be reprogrammed in the field, FPGAs offer the flexibility to continuously develop and update already deployed instrumentation. However, a major caveat of SRAM based FPGAs are their susceptibility to radiation. As the configuration of the FPGA is stored in SRAM memory, single event upsets in this configuration memory may lead to a malfunction of the FPGA design. In the main tracking detector of ALICE, the Time Projection Chamber, a total of 216 SRAM based FPGAs are used to control the read out of data from the detector. A dedicated reconfiguration solution has been implemented to continuously detect and correct any SEUs in the configuration memory of these FPGAs. During the first LHC running period this reconfiguration solution has detected and corrected thousands of single event upsets and a summary of these measurements will be presented. Previously presented measurement data collected during(s_NN)ˆ(1/2) = 7 TeV proton-proton collisions will in this paper be updated with new results from (s_NN)ˆ(1/2) = 8 TeV proton-proton collisions, (s_NN)ˆ(1/2) = 2.76 TeV lead-lead collisions, and the very recent (s_NN)ˆ(1/2) = 5.02 TeV proton-lead collisions. The results will be compared to available Monte Carlo simulation data and discussed in light of the expected operational conditions for post LS1 and LS2 running periods, and future upgrade plans for the readout electronics.

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