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A multichannel Time-to-Digital Converter ASIC with better than 3 ps-rms time resolution

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The development of a new multichannel, fine-time resolution time-to-digital converter (TDC) ASIC is currently under development at CERN. A prototype TDC has been designed, fabricated and successfully verified with demonstrated time resolutions of better than 3ps-rms. Least-significant-bit (LSB) sizes as small as 5 ps with a differential-non-linearity (DNL) of better than +/- 0.9 LSB and differential-non-linearity (INL) of better than +/- 1.3 LSB respectively have been achieved. The contribution describes the implemented architecture and presents measurement results of a prototype ASIC implemented in a commercial 130 nm technology.

Summary

Very high time resolution detectors are getting ever increasing attention in the HEP community. Novel sensor designs have demonstrated time resolutions in the sub 10 ps-rms domain. To extract the full potential of such new sensor designs, fine-time resolution measurements in the ps regime have become necessary. A new multichannel, fine-time resolution time-to-digital converter targeted to full-fill the requirements of upcoming HEP detectors like the ATLAS AFP, CMS HPS or LHCb TORCH and many other HEP R&D programs is currently under development in the microelectronics section (PH-ME) at CERN. For one single design to be suitable for a larger set of applications a high degree of flexibility is required.

The TDC architecture is based on a Delay-Locked-Loop (DLL), with 32 elements, running with a 1.56 GHz clock frequency generating 20 ps LSB sizes. To achieve 5 ps LSB sizes, in a successive stage, a resistive time-interpolation concept is employed. Only one instance of the DLL and time interpolation circuit is implemented per ASIC and shared across all the channels. Distribution buffers are implemented to distribute the fine-time code of the interpolator to the respective channels. An on-chip adjustment feature is provided to compensate for device mismatches introduced by the fine-time interpolator and the distribution buffers. The adjustment only needs to be applied to a set of channels, avoiding the need for per-channel calibration.
To limit the susceptibility to power supply noise, the architecture has been developed to sustain fast signal slopes and short signal propagation paths of all timing critical signals. Process-voltage-temperature (PVT) variations are compensated by the feedback mechanism of the DLL. This auto-adjust feature of the DLL also gives raise to trade-off time-resolution against power consumption by changing its input clock frequency, offering less demanding applications to profit from a lower power consumption. A clock synchronous counter is added to extend the dynamic range of the interpolator.

A prototype, implemented in a commercial 130 nm technology, has been designed, fabricated and successfully tested. The fine-time interpolator together with 8 channels with different configurations have been implemented. To characterize the linearity of the TDC, a code density test has been performed. After calibration a differential-non-linearity (DNL) and integral-non-linearity (INL) of +/- 0.9 SLB and +/- 1.3 LSB has been achieved. The single-shot precision of the TDC has been evaluated by means of a time-difference measurement for different wire length differences. Across the whole measurement series a single-shot precision of better than 2.44 ps-rms has been demonstrated. The full prototype consumes between 34 mW/channel to 42 mW/channel. Lowering the input clock frequency to 781 MHz (= 10 ps LSB sizes), the power consumption can be reduced to 21 mW/channel and 26 mW/channel respectively. The architecture exhibits a time shift of -0.19 ps/mV and a temperature dependence of 0.44 ps/deg. With the measurement precision of the test setup, inter-channel crosstalk between two neighboring channels has been evaluated to be below +/- 1 LSB.

The prototype circuit has been found to be a suitable candidate for a full TDC development meeting the special requirements of next generation HEP detector designs. The delicate time interpolation circuit, will only need

minor changes to be expanded from 8 channels to a larger set of channels. To allow to run at lower input clock frequencies (e.g. 40 MHz) and increase the dynamic range of the demonstrator ASIC a PLL and a counter will be added to such a new ps resolution TDC.

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