Contribution ID: **63** Type: **Poster**

SALT - new silicon strip readout chip for the LHCb Upgrade

Wednesday, 25 September 2013 16:35 (1 minute)

The LHCb detector, operating at the LHC proton-proton collider, has finished its Run I period. After more than two years of collision data taking the experiment accumulated corresponding integrated luminosity of around 3.1 fb-1. The full recorded data sample will be used by physicsts to search for New Physics and precise measurement of CP-violation in heavy flavor quark sector. Despite its superb performance it is clear that the LHCb experiment is statistically limited for a number of important
decay channels (such as Bd->K*mumu or Bs->phiphi). This, in turn, is related to the current data acquisition architecture which can acquire data at the top rate of 1.1 MHz at the instantaneous luminosity
close to 4x10ˆ32 [cm-2s-1]. The LHC machine is already capable of delivering more than one order of magnitude higher luminosity that is presently used by the LHCb. This fact led the LHCb Collaboration to preparing a proposal regarding an upgrade of the LHCb spectrometer
that would allow it to exploit higher luminosities (up to 2x10ˆ33), greatly improve the trigger efficiencies for both hadronic and leptonic decay modes. The upgrade will allow the experiment to collect about 50 fb-1 of data. One of the most important topic of the LHCb upgrade is design
and implementation of new front-end electronics allowing a full detector read-out at the bunch-crossing rate of 40 MHz. This will be further augmented by a software trigger that will be capable of processing the data at the same rate. This talk presents a novel design of the common readout chip for silicon strip detectors which will be able to digitise the analogue signal on-detector and subsequently perform digital processing and zero-suppression.

Summary

New front-end readout chip - SALT (Silicon ASIC for LHCb Tracking), is being currently designed by the Krakow group and will be used in the tracking system of the modernised LHCb experiment.
The new chip must perform synchronously full processing and zero suppression of the raw data stream. This is a novel approach to the design of custom readout electronics circuits intended for the experimental High Energy Physics application. The SALT ASIC (Application Specific Integrated Circuit) can be used to instrument all silicon micro-strip sub-detectors of the upgraded LHCb spectrometer. Additionally, its back-end part may be employed in the readout systems of the scintillating fiber tracker
and the new RICH detector. This note aims at providing a detailed description of the digital processing chain that needs to be implemented within the chip.
Silicon microstrip sensors are being considered for the upgrade of the VELO (VErtex LOcator), TT (Trigger Tracker) and IT (Inner Tracker) subsystems. It is therefore crucial for the LHCb upgrade that a FE readout chip
suited to this detector technology is developed. The R&D eort has indeed already started. Specications for the chip design have been devised for the VELO, TT and IT strip detector options. The chip will integrate 128 individual readout channels implemented in the IBM 130 nm CMOS technology. From the operational point of view each channel will consist of an AC-coupled analogue FE amplier-shaper, followed by a
6-bit ADC. The ASIC functionality will include zero-suppression and an interface with the GBT chip that will handle the high speed off-detector data transmission. A slow control block will be part of the design.
Commonalities with a SiPM (Silicon Photon Multiplier) FE readout chip for scintillating bres will also be studied. Apart perhaps from the analogue FE part, the two applications might be able to share a large part of

the chip design and developments. A first version of the 6-bit ADC and analogue FE block were recently submitted for manufacturing as part of a multi-project wafer.

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Session Classification: Poster