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# The new NA62 LKr readout: first tests and future perspectives

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The NA62 experiment at the CERN SPS (Super Proton Synchrotron) accelerator aims at studying ultra-rare kaon decays. The high resolution Liquid Krypton (LKr) calorimeter, built for the NA48 experiment, is a crucial part of the NA62 photon-veto system. However, the back-end electronics of the LKr calorimeter has to be redone in order to accommodate the new requirements. The exhaustive specification was prepared and the decision to sub-contract the development and production of the acquisition board to industry was taken in 2011.
This paper presents the primary test results of the Calorimeter REAdout Module (CREAM) prototype delivered by the manufacture in March 2013. All essential features, analog performance, trigger properties, data processing and readout, are covered.

## Summary

The CREAM is a 1-slot wide VME 6U form-factor module. One module houses 2×16 channels 40 MS/s ADC with a 14-bit dynamic range and an ENOB greater than or equal to 10-bit. The external reference sampling clock will be provided by the Timing, Trigger and Control (TTC) system designed for the LHC experiments. Each of the CREAM input channels consists of an AC-coupled differential line receiver and a pulse shaper. A 14-bit DAC allows tuning the DC offset of each channel in order to correctly adjust the pedestals and to preserve the dynamic range. The signal is shaped before the ADC input into a differential semi-Gaussian signal with a 40 ns rise time and a 70 ns full width at half maximum (FWHM). During the data acquisition, the CREAM inputs are continuously digitized and written into an on-board pipeline memory. When the L0 trigger occurs, the control logic freezes the corresponding data samples from all channels and copies them into another memory partition for a possible readout in case a L1 trigger is received. The L0 trigger latency should not exceed 10 ms and the module must be able to store locally up to 400×10ˆ3 14-bit samples per channel. The size of the data buffer is defined by the L0 trigger rate (nominally 1 MHz), the number of samples per event and by the duration of the data-taking phase (accelerator burst time, typically up to 10 s with a period of up to 50 s). For this reason, an 8 GB DDR3 SODIMM module was chosen to ensure necessary storage capacity for data from 16 channels, and fulfil form factor requirements. The data acquisition is performed via a 1 Gbit Ethernet link and, for test purposes, a low rate optional readout via a VME64 compliant interface is foreseen. Since for each event a large fraction of channels will only contain pedestal counts, various zero suppression algorithms are foreseen to reduce the data flow to the experiment event building farm.
In addition to the data processing and readout, digitised signals from the selected channels are summed up to build a Trigger SUM (Super-Cell) and sent to the experiment trigger system. The selection of the channels contributing to a particular Super-Cell, as well as the shape of Super-Cells (4x4 or 2x8), is programmable. The Trigger SUMs are readout via 4 differential 640 Mbit/s serial links sharing one standard Ethernet cable. All control, processing and communication functionalities of the board are implemented in a reconfigurable FPGA device. The ‘basic’firmware should not use more than 40% of device capacity, in order to allow the integration of new data processing and/or trigger algorithms during the lifetime of the experiment.
In total, about 450 CREAM modules should be produced, tested and installed, in order to have the entire LKr calorimeter readout system operational by mid-2014.

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