Contribution ID: **177** Type: **Oral**

A Real-time Histogramming Unit for Luminosity and Beam Background Measurements for each Bunch Crossing at the CMS Experiment

Thursday, 26 September 2013 16:05 (25 minutes)

The Real-time Histogramming Unit (RHU) is a VME board for sampling and processing discriminated signals from detectors in real time and free of dead-time. The RHU is used at the CMS experiment to measure the arrival time of signals from the BCM1F detectors relative to the orbit trigger of the LHC at CERN. The RHU incorporates a FPGA, 21MBit memory and an embedded Linux system for readout. For each input channel a histogram is produced by the FPGA algorithm in real time that contains the hits per bunch over several orbits. A postmortem buffer can be used for data analysis after a beam dump.

Summary

The Real-time Histogramming Unit (RHU) is a VME board for sampling and processing discriminated signals from detectors in real time and sending data via network. The RHU is used at the CMS experiment to measure the time of signals from the BCM1F detectors relative to the orbit trigger of the LHC. The detectors are installed close to the interaction point inside the CMS detector to measure both collision products and beam halo. The RHU incorporates a FPGA with 5MBit internal memory, 16MBit external memory and a single board computer (SBC). The FPGA of the RHU reads out the detector channels and samples the hits with a frequency of 160MHz, synchronous to the LHC bunch clock. For each channel a histogram is produced in real time that contains the hits as a function of time collected over several orbits mapped on the time of an orbit. The histograms have a binning of 6.25ns and contain 14256 bins. The external memory is used to store the last 50 orbits of sampling data in a ring buffer. When a beam dump occurs, the RHU stops sampling and the postmortem data can be read out for analysis. Every 2048 orbits, the histogram buffers are read out via the Linux based SBC and are transferred via network to the Luminosity DAQ. To avoid dead time, the histogram buffers are implemented as a dual buffer system and sampling continues while software reads out the data. The SBC is connected via a static memory interface to the FPGA for read out and has a bandwidth of 20MByte/sec. The SBC incorporates a 32Bit ARM926 Core at 400MHz and 128MB of RAM. A Linux Kernel driver has been implemented to achieve full performance at the interrupt-based read out. In the user space, a TCP server waits for connections and sends the data to connected clients. A software framework has been developed to allow access to the data of the RHU via network and can be used with ROOT programs for data analysis. The framework uses shared memory to allow multiple clients on the same machine to reuse the network connection to the RHU device and to save bandwidth.
Results on the performance of prototypes used in the last running period are presented.

Primary author: PENNO, Marek (Deutsches Elektronen-Synchrotron (DE))

Co-authors: DABROWSKI, Anne (CERN); STICKLAND, David Peter (Princeton University (US)); Mr HENSCHEL, Hans Henschel (DESY); Dr LEICH, Holger (DESY); LEONARD, Jessica Lynn (Deutsches Elektronen-Synchrotron (DE)); Dr CASTRO CARBALLO, Maria Elena (Deutsches Elektronen-Synchrotron (DE)); LOHMANN, Wolfgang (DESY)

Presenter: PENNO, Marek (Deutsches Elektronen-Synchrotron (DE))

Session Classification: Programmable logic, design tools and methods