The LOC project status and SMU’s plan in ASICs

Jingbo Ye for the LOC project at SMU
The project is actually lead by Datao Gong
For details on recent LOC results please see this talk at TWEPP: https://indico.cern.ch/contributionDisplay.py?sessionId=17&contribId=164&confId=228972

There are two developments:

- The dual channel serializer:
  - **LOCs2**: 2×8 Gb/s 16:1 serializer, prototype, tested to design goals.
    - **LOCx2**: 2×5.12 Gb/s 8:1 serializer for ATLAS LAr phase-1, low latency, low power, with framing, CRC, and scrambling. In design. Will be QFN-88 packaged. Transmits any 12-bit serial output ADC data.

- The VCSEL drivers:
  - **LOCld1**: 8 Gb/s VCSEL driver with I2C, QFN-24, tested to design goals. This is a generic VCSEL driver with SLVS inputs. With VCSEL at 8 Gbps < 200 mW.
  - **LOCld4**: 4-ch open-drain array VCSEL driver. Tested but with problems.
  - **LOCld8**: 8-ch array VCSEL driver, try to fix problems identified with LOCld4. submission Dec. 2013.
Future plans:

- **serializer:**
  - Follow the SOS technology (PC process, 180 nm) to move to 10 Gb/s per channel.
  - Join CERN for 65 nm development.

- **VCSEL drivers:**
  - Probe the speed of open-drain array VCSEL driver with the current GC process.
  - LOCld12: 12-ch array VCSEL driver to complete the LOCld4,8, and 12 series.
  - Join CERN for 65 nm development.
Backup slides
LOCs2 design features

- Two (2) channel 16:1 serializer sharing one LCPLL; Each channel operates at 8 Gbps.
- LVDS 16-bit × 2 data and 500 MHz clock inputs.
- Input data can be latched with either edges of the internal clock.
- Output CML signal > 200 mV over a 100 ohm differential load.
- LC-tank PLL with loop bandwidth programmable from 1.3 to 6.8 MHz.
- Power consumption 1.2 Watt.
LOCs2 test setup

- The LOCs2 die is wire-bonded to a PCB. A QFN packaged version will be tested soon.
- Input PRBS $2^7-1$ data from the Kintex-7 board; Output serialized data to a high-speed oscilloscope for jitter and eye measurement.
LOCs2 eye diagrams

- LOCs2 works from 6.6 to 8.5 Gbps, limited by the LCPLL tuning range.
- Measured power consumption is 1.25 watt at 8 Gbps, matching simulation.
LOCs2 bathtub curve

- The bathtub curve of LOCs2 at 8 Gbps.
- At $10^{-12}$ the eye has an opening of about 60 ps.
• Measure jitter with a 50 Gs/s real time oscilloscope.
• Measure the total jitter (pk-pk) of the serial output bit stream to be about 30 ps with the input PRBS $2^7$-1 parallel data. RJ about 1 ps.
• Measure the PLL jitter through a clock signal divided-by-8 from the VCO clock; Only random jitter is significant in this case and it is measured to be below 1 ps.
• 8-Gbps single channel VCSEL driver with active shunt peaking.
• I2C slave and DAC module (thanks to Sandro Bonacini and Paulo Moreira) for remote configuration.
• Programmable: VCSEL bias and modulation currents; peaking strength.
• VCSEL bias and modulation currents refer to a constant current source, not sensitive to transistor threshold voltage change caused by radiation.
LOCld1 lab test

• LOCld1 is wire-bonded to a PCB for this test. A QFN-24 packaged version will be tested soon.
• Input 200 mV PRBS signal from signal generator and from LOCs2.
• Output signal to oscilloscope through SMA connectors for electrical test, to a VCSEL for optical signal test.
• VCSEL modulation current programmable (4 bits) up to 7.6 mA. VCSEL bias current programmable (4 bits) up to 8 mA.
LOCld1 eye-diagrams

RJ = 0.89 ps DJ = 11.7 ps TJ = 21.8 ps

5 Gbps

RJ = 0.9 ps DJ = 15.5 ps TJ = 26.0 ps

8 Gbps

9 Gbps

10 Gbps
LOCld1 irradiation tests

LOCld1 test board

Test system

LOCld1 test board in X-ray chamber

LOCld1 has been verified to meet ATLAS LAr front-end electronics TID requirement. LOCld1 has also been tested in a neutron beam of 800 MeV. No bit error is found in the data transmission, and in its I2C configuration circuit.
LOCld4 design

- 4-channel 8 Gbps VCSEL array driver, taken advantage of one submission with spare design area in one corner.
- Design: active shunt peaking + open-drain last stage
- Design VCSEL modulation current 6 mA
Input: Diff 200mV (peak-peak) at 5Gbps
Output: Bias-Tee PE1606 (100k ~ 12.4GHz) pulling up to 3.3V
5 Gbps eye-diagram looks good, but amplitude is only 200 mV
Problem identified, next design to be submitted in Dec. 2013
LOCx2 dedicated to ATLAS LAr

- LOCx2 is a 2-channel full functional 5.12 Gbps transmitter for ATLAS LAr trigger upgrade in phase I.
- LOCx2 interfaces to 8 channel 12 or 16 bits ADC serial outputs with the full digital block LOCic.
- LOCic and the new LCPLL will be submitted December 2013.
- LOCx2 is planned to be packaged in QFN-88 (10 mm × 10 mm).
LOCic design

- Simi-manual layout based on foundry's digital library plus a pipeline technique are used to research the speed of 640 MHz.
- The design is optimized to reduce transmission latency (to transmit trigger data) and overhead.
- 12-bit BCID is encoded in the data frame.
- CRC-8 code is added to detect transmission error; Scrambler is included to transfer DC-balanced data.
- Design is in final checking stage.
LOCic design

LOCic layout
LC-PLL for LOCx2

- 2.56 GHz LC-tank PLL with 2.56 GHz and phase adjustable 640 MHz and 40 MHz clock outputs.
- The Input reference clock is 40 MHz; Loop bandwidth is programmable from 500 KHz to 2 MHz
LC-PLL for LOCx2

LCPLL layout
LOCs2 and LOCld1 package

- 10 dies of LOCld1v2 are packaged in 5mm x 5mm 24-pin QFN.
- 10 dies of LOCs2 are packaged in 12mm x 12mm 100-pin QFN.
- The test boards of packaged chips are ready for test

(Put packaged chip photo here)