DOE CDRD for High Rate Data Links for Collider Experiments

FERMILAB, U. MINNESOTA,
ARGONNE LAB, OHIO STATE U., SMU

A three (3) year program: 2012/13-2015 (wishful).

FNAL: Coordinate irradiation testing at FNAL MTA beamline location, provide testing services for array modules, try to engage a corporate vendor (i.e. Reflex Photonics) to work with on array based transmitters.

SMU: Qualify commercial laser driver array ASICs. Design array based module (based on POD design concept) and fabricate prototypes for testing.

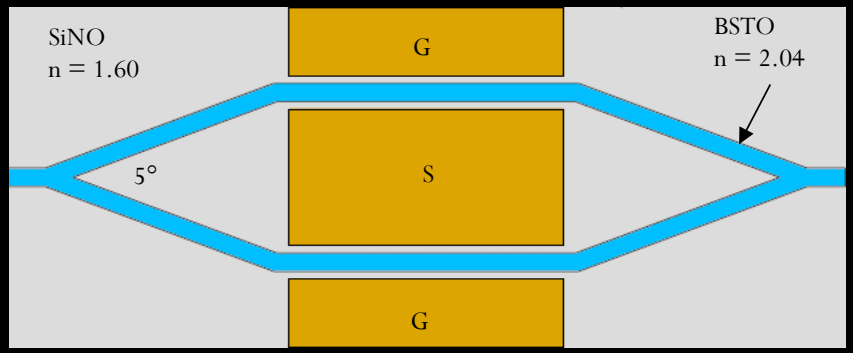
OSU: Design, fabricate, and test a multichannel VCSEL array driver capable of 10 Gbps/channel.

Minnesota: Develop and characterize materials (i.e. BaSTO, Barium Strontium Titanate) for fabrication of a rad hard Mach Zehnder Modulator. Fabrication of prototypes of the modulator.

ANL: Qualification of commercial light modulators; develop polarization control methods to control laser input polarization for modulators.

BSTO (Barium Strontium Titanate) M-Z Modulator Progress

U of Minnesota collaboration with A. Block, A. Gopinath, E. Kleinsasser, B. Stadler (Electrical & Computer Engineering) and R. Rusack (Physics) to make a low-mass high bit rate Mach-Zehnder modulator.



Advantage of this oxide is that r_{xx} (Pockels coefficient) is a factor of 5 or more large than lithium niobate. Device will be smaller → Less mass and higher bit rates.

Modulation depends only on optical transmission at 1310/1550 nm → should be rad hard. TBD

Motivation

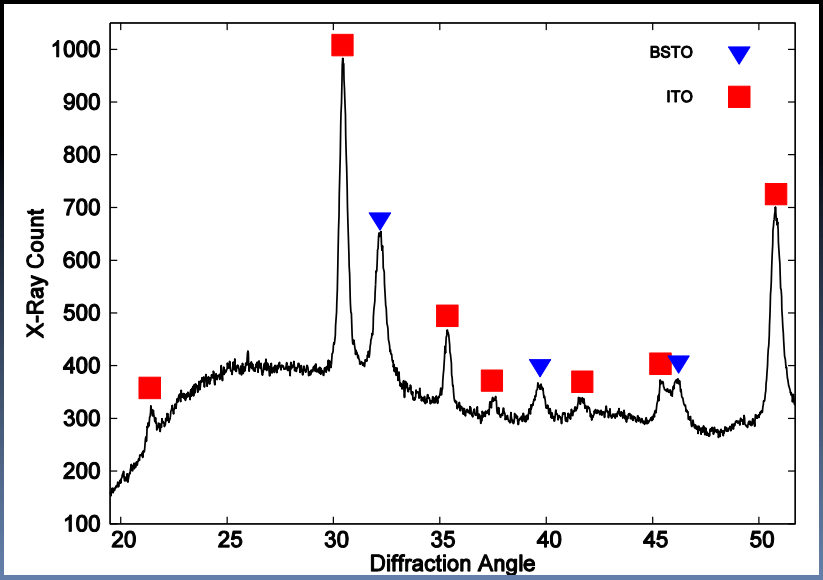
Barium Strontium Titanate is a Perovskite crystal with a Pockels coefficient (r_{xx}) > 150 pm/V. We will grow by sputtering and pattern a waveguide in the film.

Change in index *n* is given by $\Delta n = -1/2 n^3 r_{xx} xE$

- Electro-optic coefficient r_{xx} for BSTO 150pm/V to 570pm/V. ($LiNbO_3$ r_{xx} ~30pm/V)
- For r_{xx} of 150pm/V, active length around 3-6mm with push-pull voltage ~4V.
- Device size ~1cm long.
- 40Gbps operation feasible.
- Like $LiNbO_3$, BSTO should be radiation hard. TBD

Status

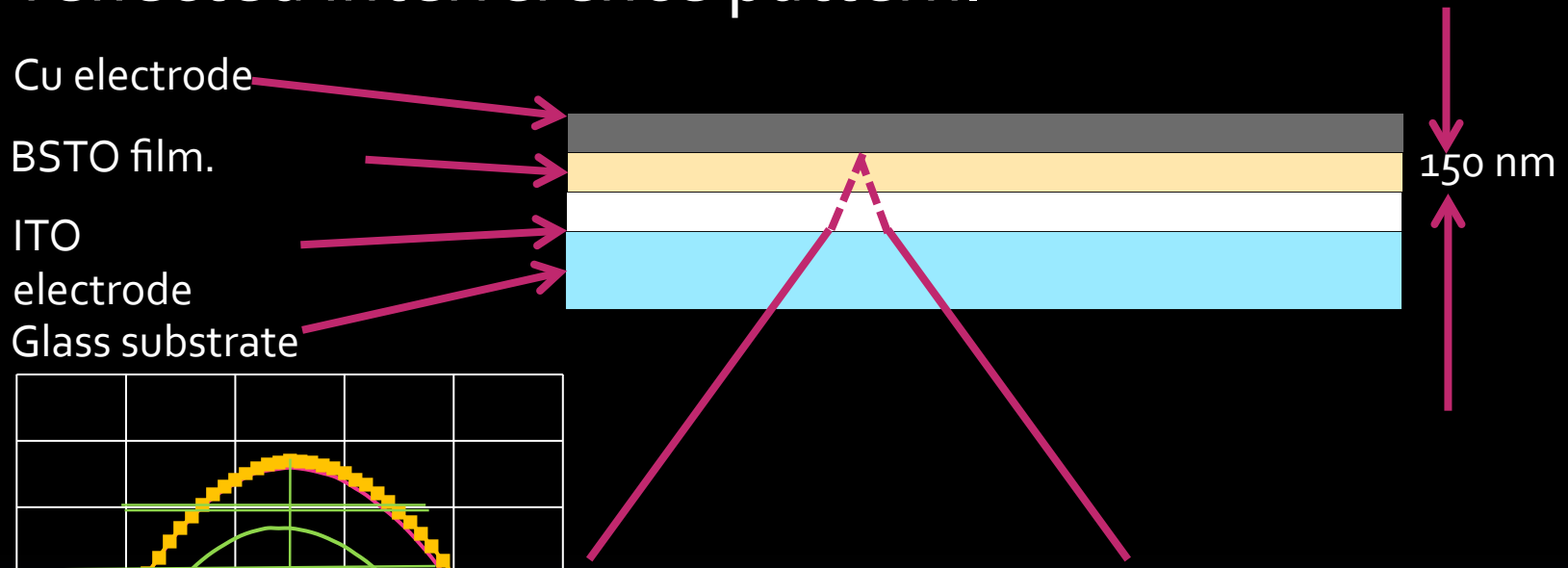
- Film production:
  - Now have consistent recipe for BSTO growth. Stoichiometry and crystal structure reproducible. Have grown films on Silicon, Glass and ITO (Indium Tin Oxide).
  - X-ray patterns match standard crystal patterns and stoichiometry measured with WDXS.*

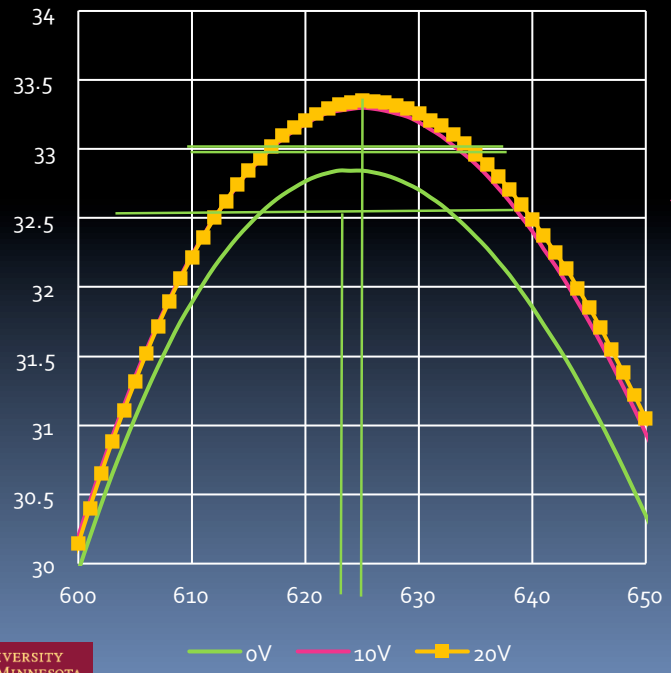


*Wavelength dispersive X-ray Spectroscopy

Measurement of Δn

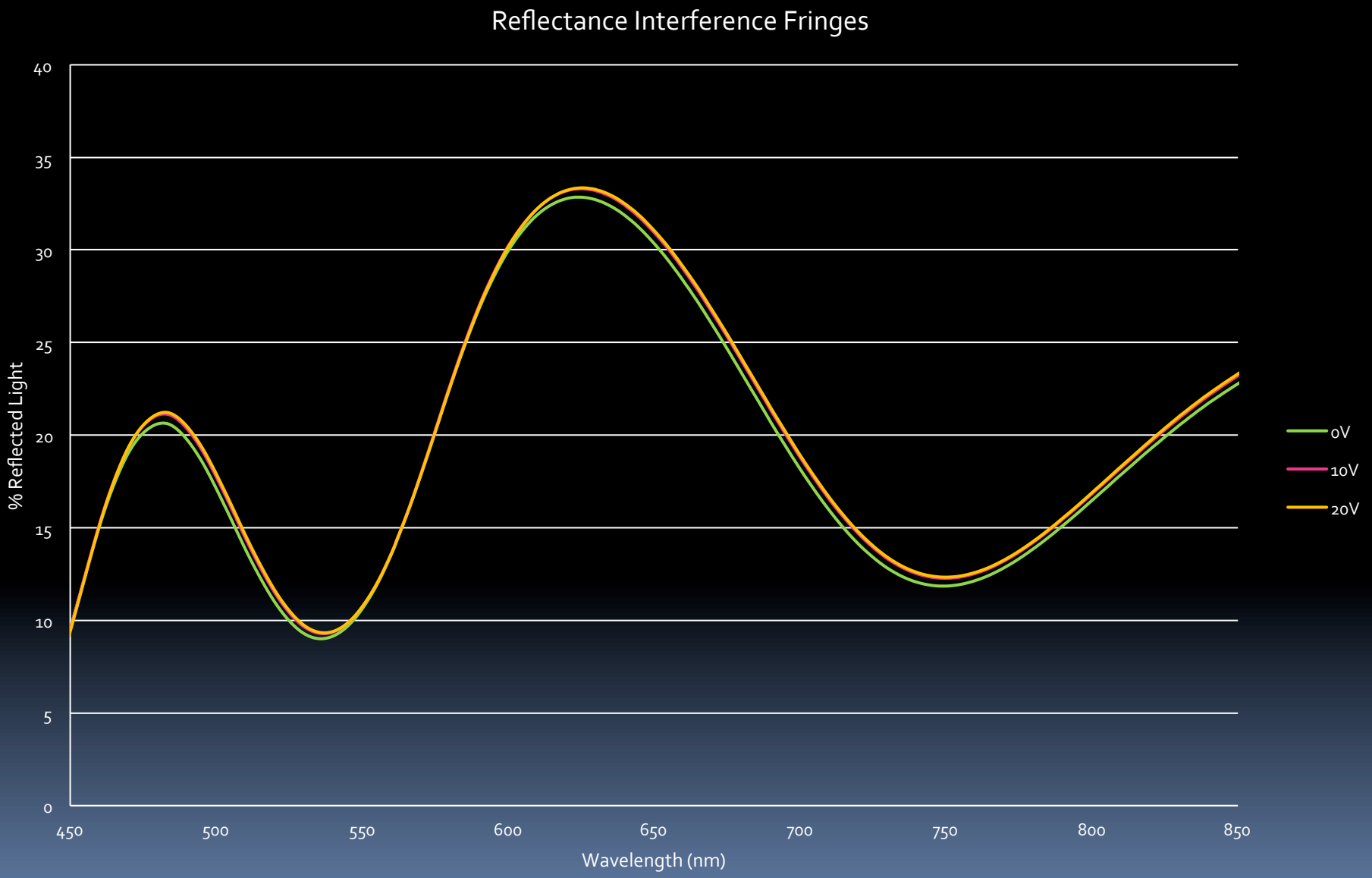
Measure change in index by measuring shift in reflected interference pattern.





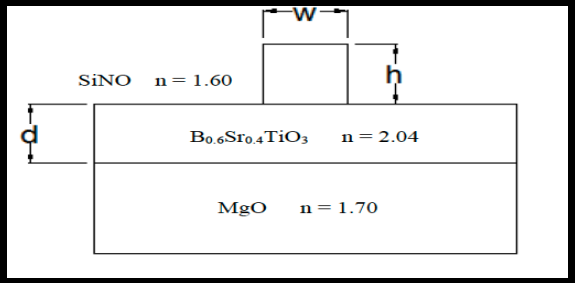
- With this we measure that the shift in *n* saturates at 1%.
- This is a large shift compared to other standard materials.

Reflectance Pattern

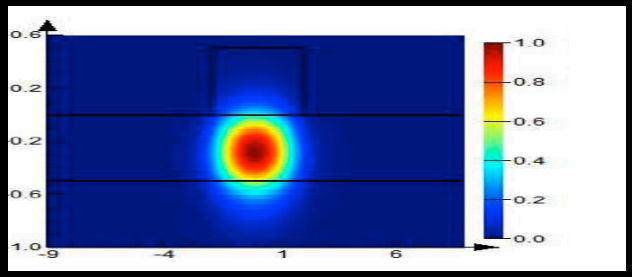


Status of Waveguide Design.

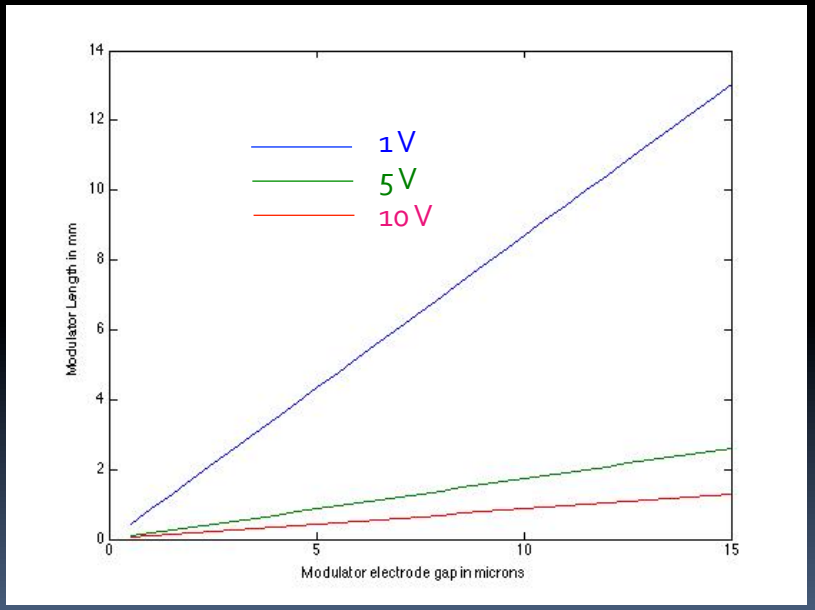
Waveguide modeling with Finite Difference Time Domain Solutions 3-D simulation package.



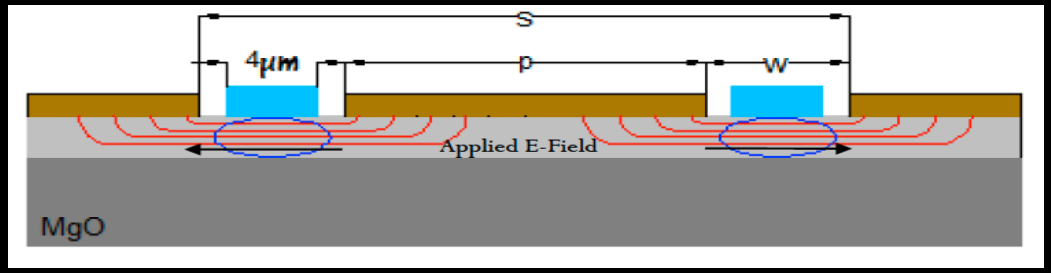
d =0.5micron



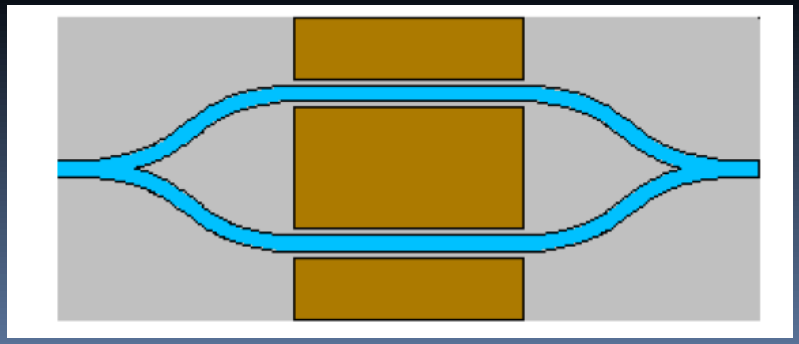
Fundamental mode



Approximate design length 5 – 6mm.



Section of modulator layout



Detailed design in progress.

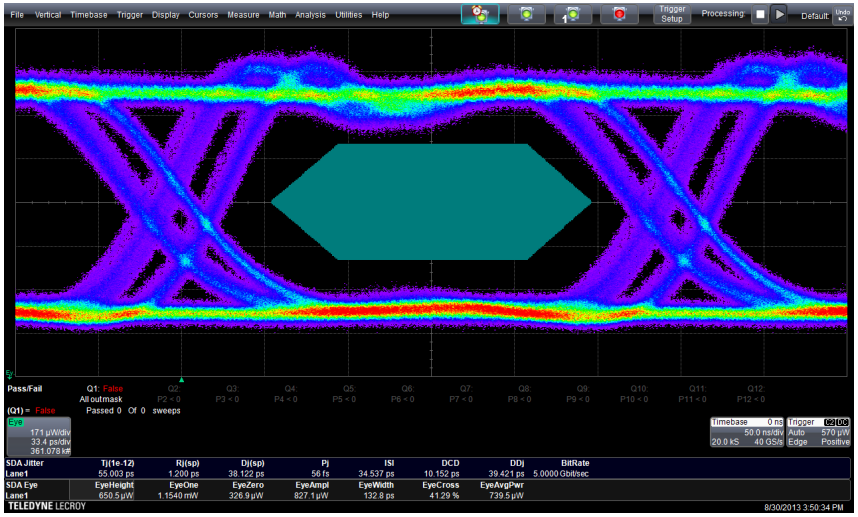
OSU 10 Gb/s Array Driver

D. Shane Smith, K.K. Gan, Jason R. Moore

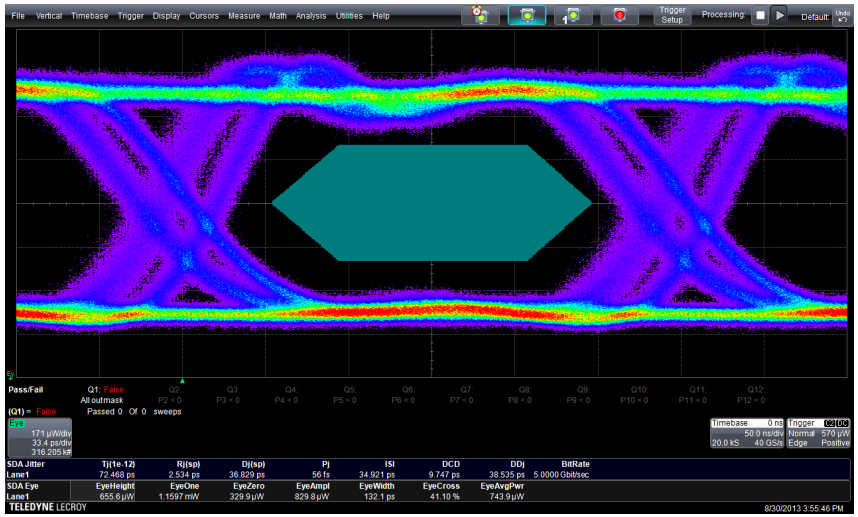
OSU 5 Gb/s VCSEL Array Driver

- 130 nm CMOS, 8 Channels + 4 optionally used spares
  - Works like a crosspoint switch: an input signal from any of the 8 inner channels can be routed to any of the spare VCSEL channels
- 5 Gb/s optical eyes satisfy the IEEE spec.
  - jitter increases with all channels active but still passes mask test

one active channel



all channels active



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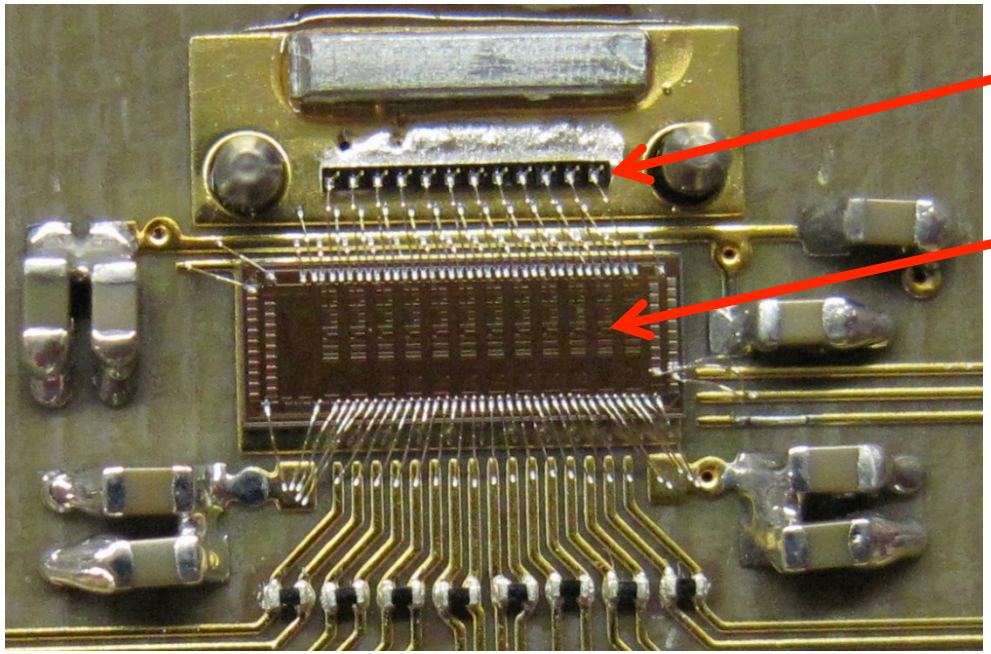
OSU 5 Gb/s VCSEL Array Driver

- Irradiated two array drivers + ULM 10 Gb/s VCSELs (like shown below) to 1.51×10^{15} 24 GeV protons / cm^2 (33 Mrad in GaAs)
- Preliminary tests show problems operating at 5 Gb/s unless VDD increased (4 Gb/s is fine)
- Suspect VCSEL damage (threshold shifts) to be the cause of reduced speed, need to confirm this with a separate irradiation



ULM 10 Gb/s VCSEL Array

130nm VCSEL Driver Array

10 Gb/s VCSEL Driver Design

- From extracted layout simulations, 10 Gb/s in 130 nm CMOS is possible but marginal
  - Includes CML receiver + driver stage (full chip)
- Presently working on porting design to TSMC 65 nm CMOS
  - Learning the TSMC 65 nm flow and process
  - Have a preliminary layout and extracted simulation of the driver stage

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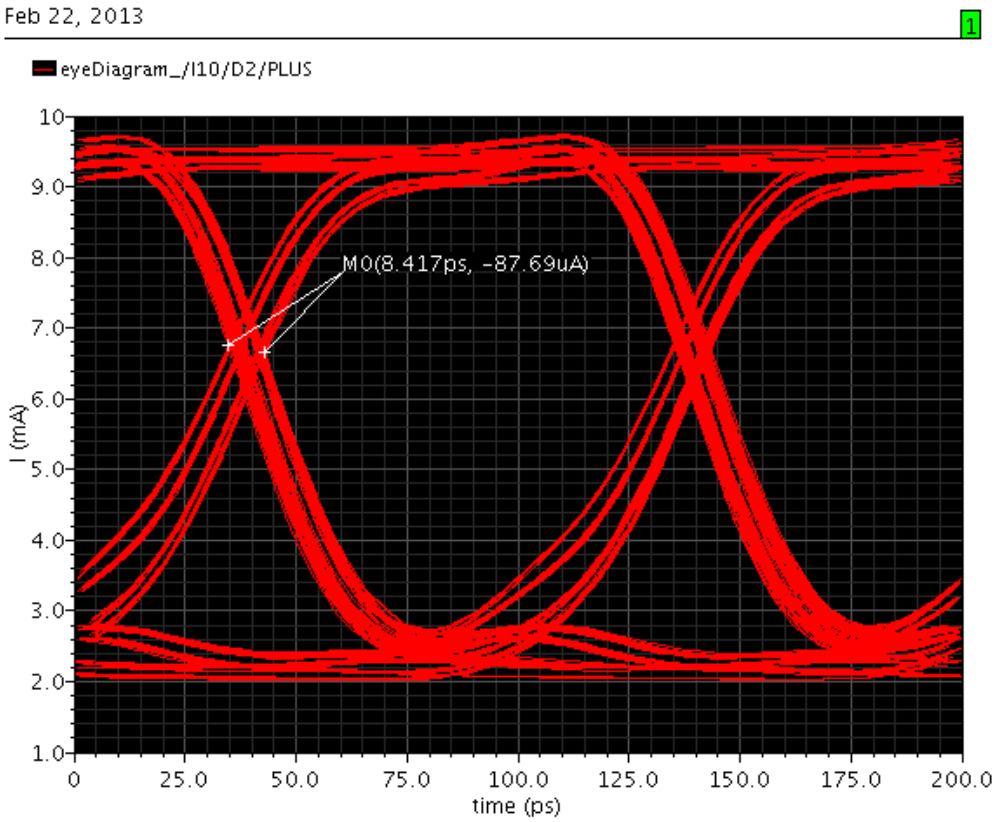
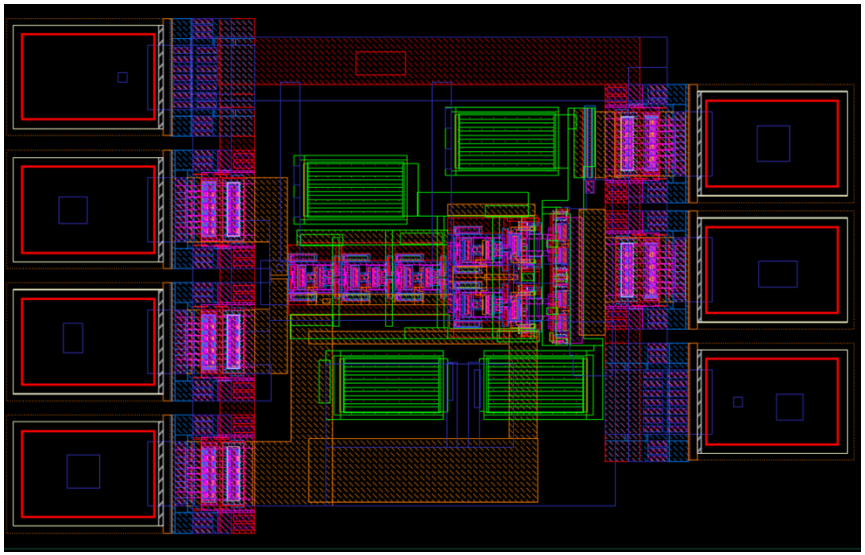
130 nm 10 Gb/s VCSEL Driver

Full Chip Extracted Layout Simulation





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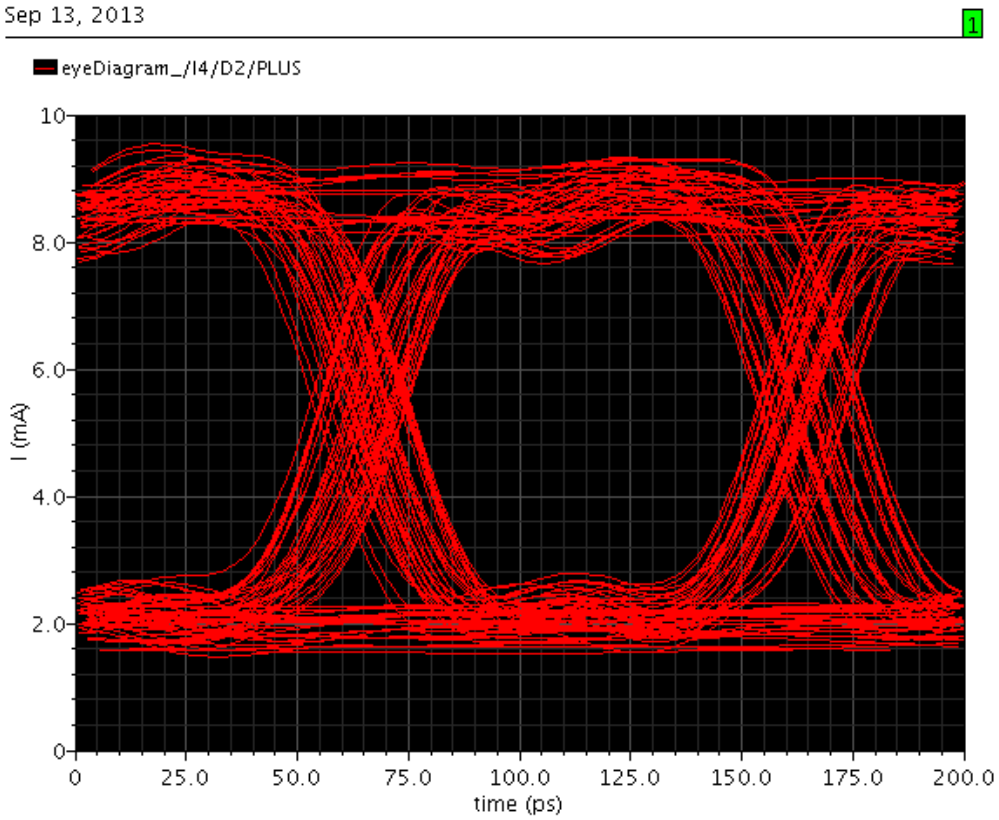
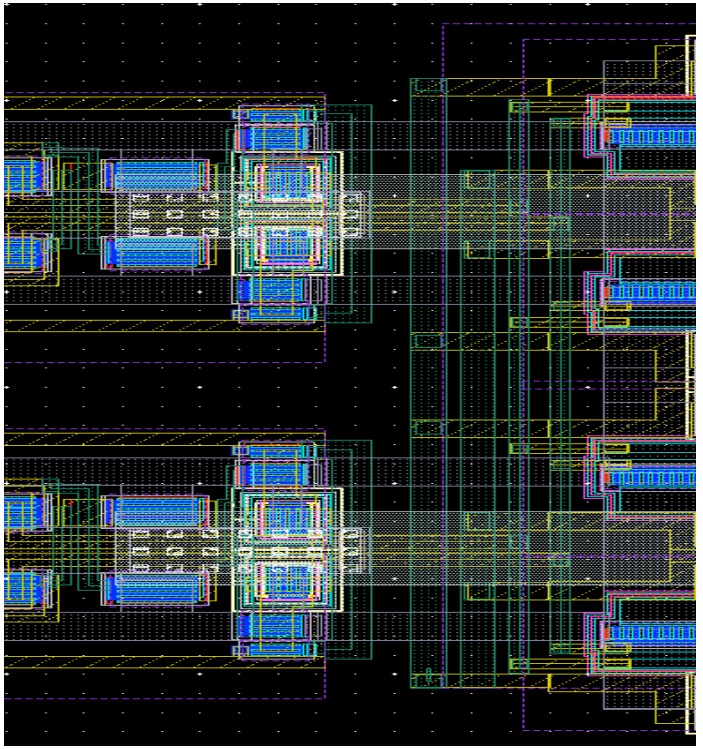
65 nm 10 Gb/s VCSEL Driver

Driver Stage Only, Extracted Simulation (Preliminary)





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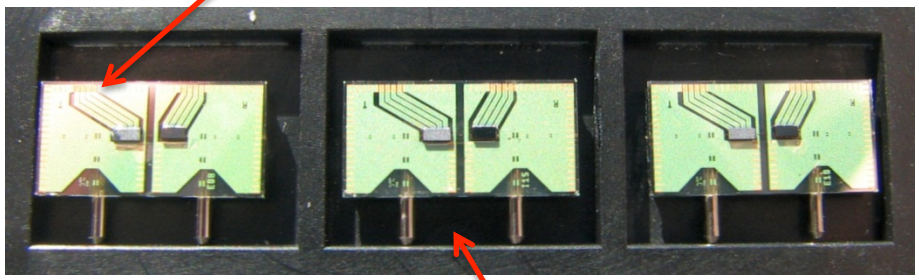
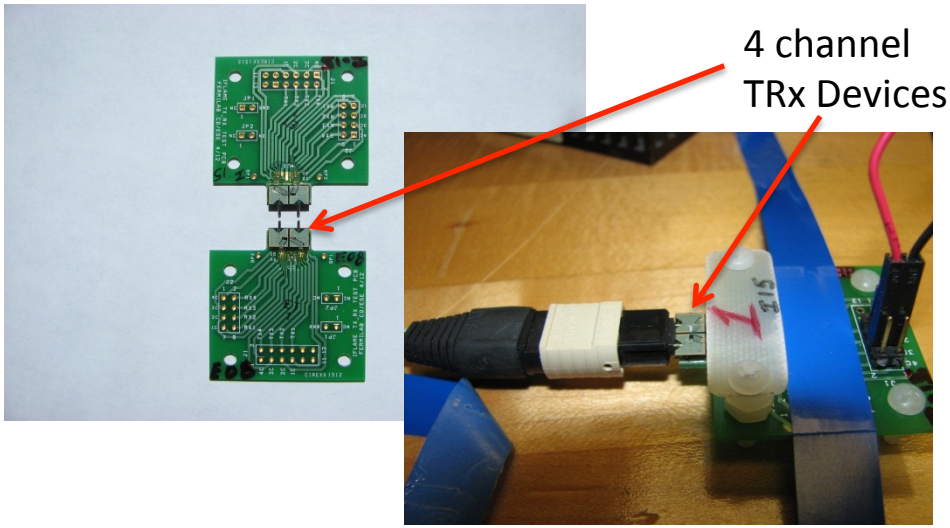
High Data Rate Links for Collider Experiments
Rad Hard Array Transmitter Devices - COTS

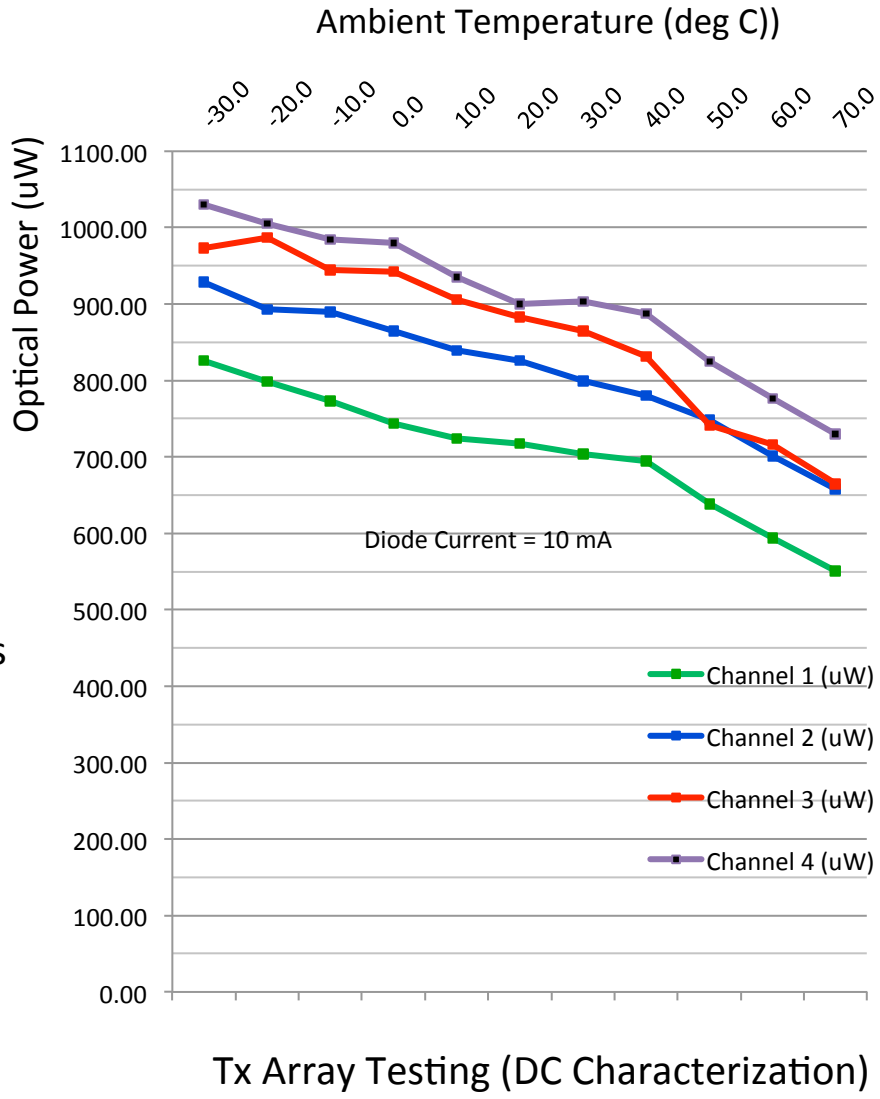
VCSEL Electrical Interface (Tx)



MT Optical Connection



Fermilab Array Test Cards



Tx Array Testing (DC Characterization)

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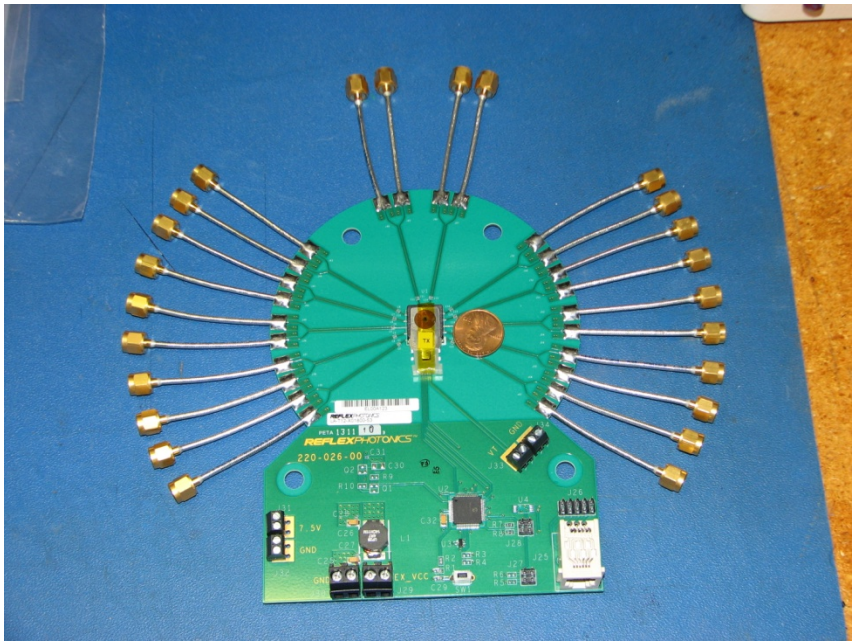
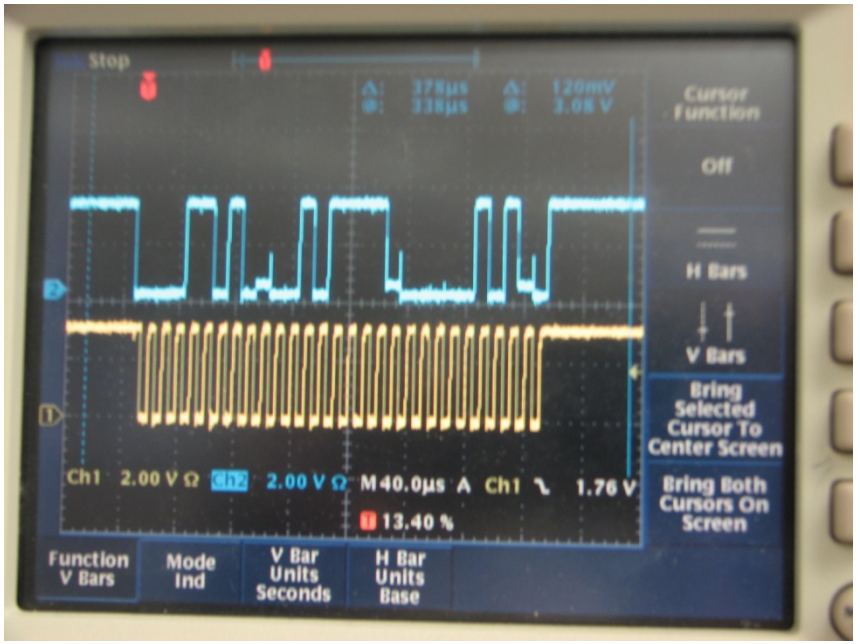
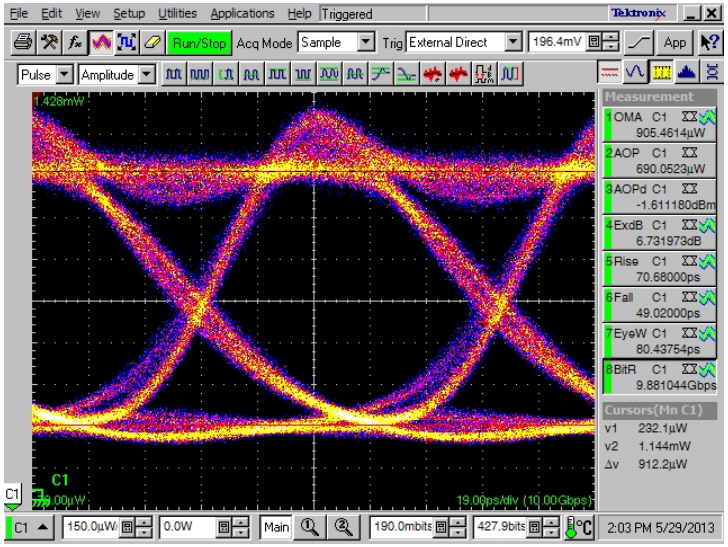
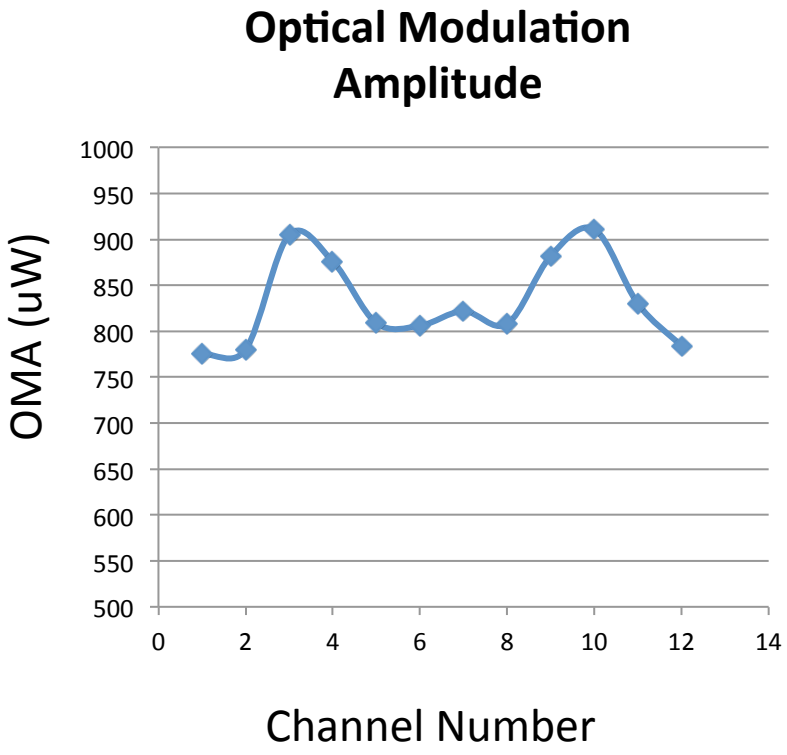
Rad Hard Array Transmitter Devices - COTS

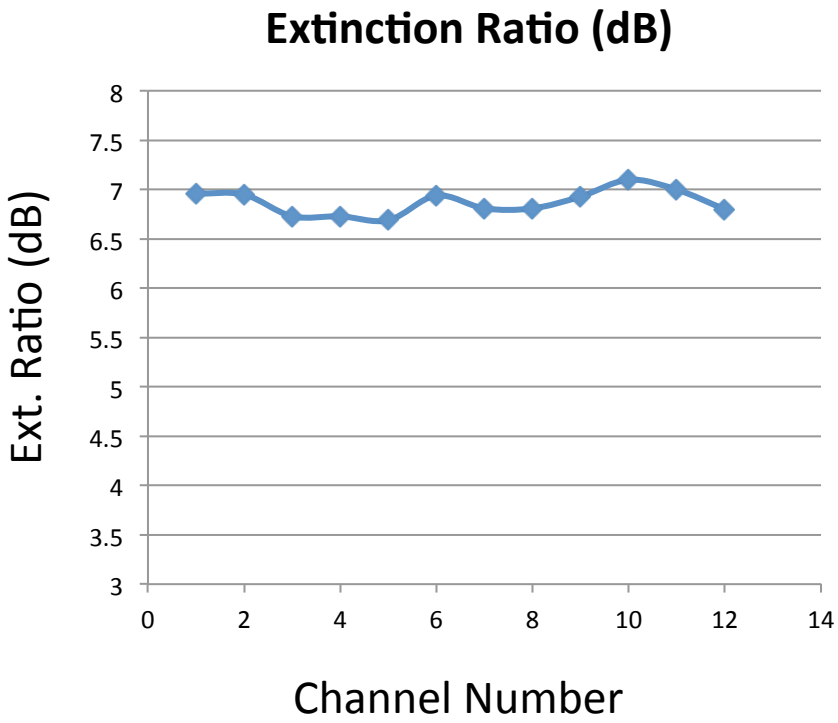






Vendor 2 Optical Engine

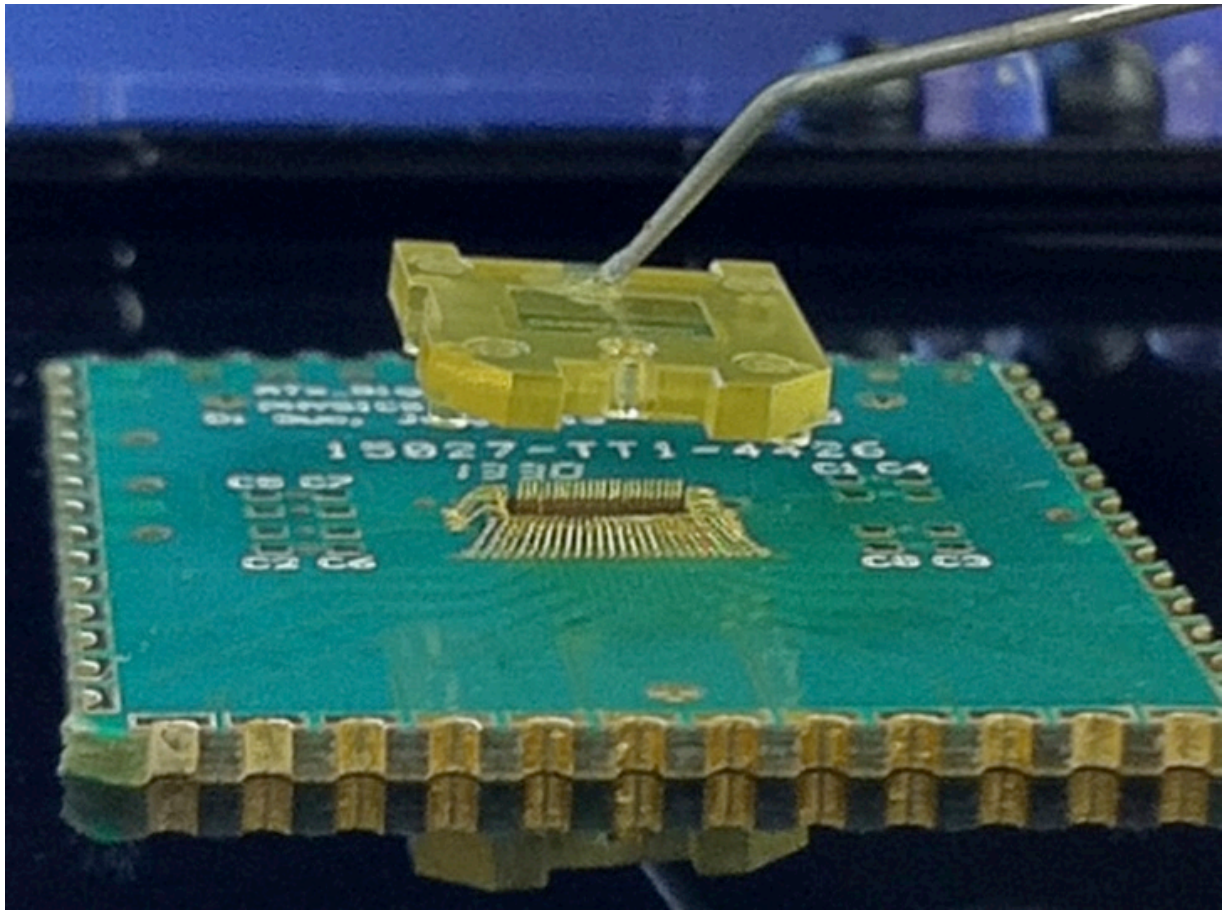


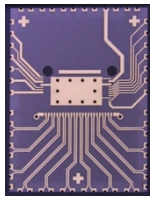


SMU: array VCSEL based optical transmitter ATx

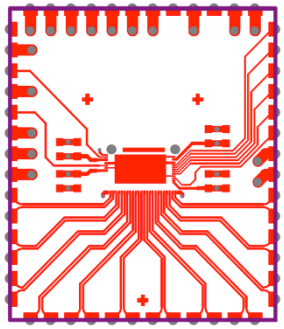
For details please see TWEPP poster:
https://indico.cern.ch/contributionDisplay.py?contribId=163&confId=228972&sessionId=9

Optical coupling with array VCSEL using MOI (USCONEC). Experimenting with ceramic and FR4 substrates.



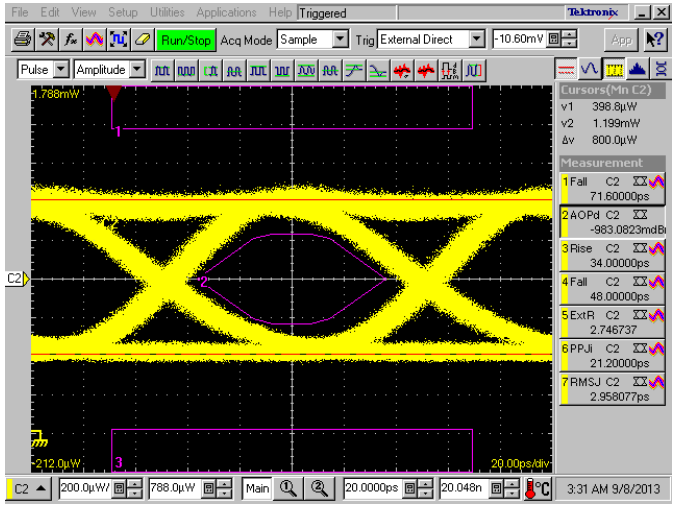


Ceramic substrate
0.98 cm x 1.30 cm

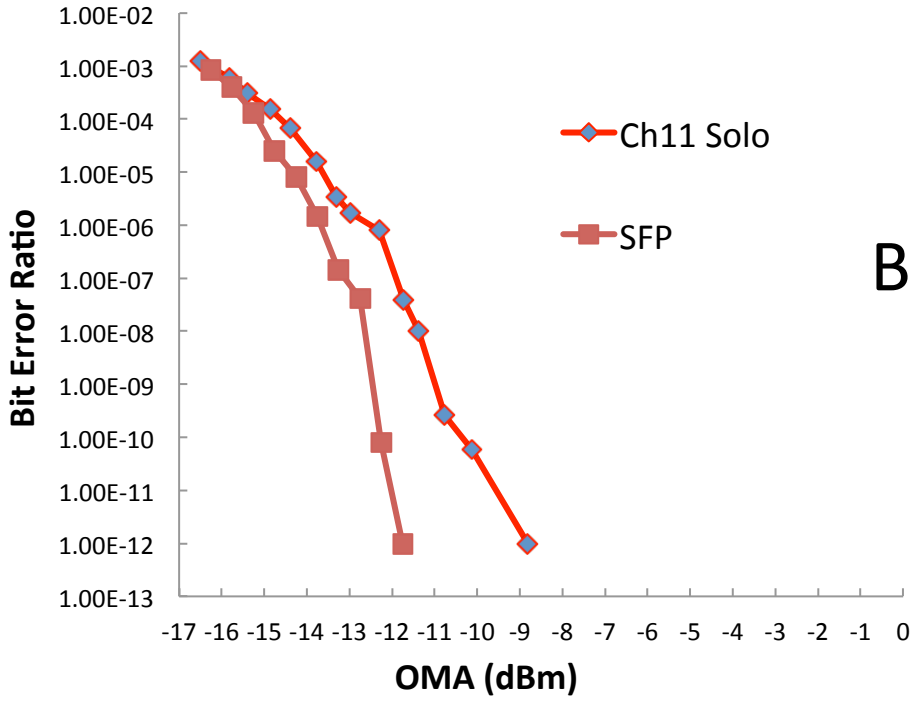


FR4 sunstrate
1.9 cm x 2.2 cm

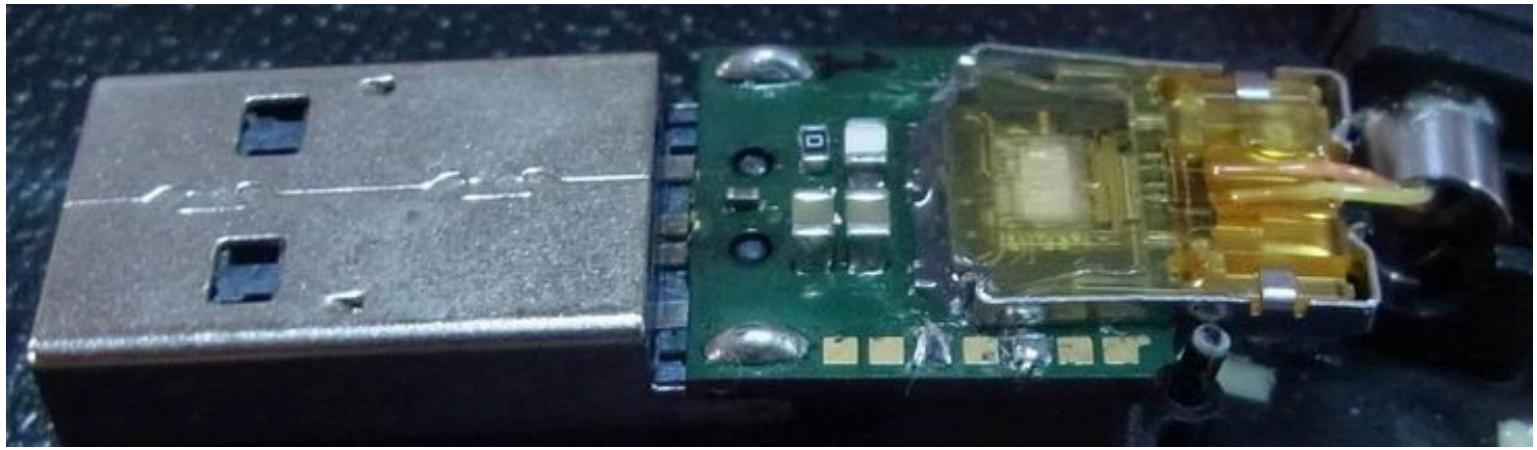
Preliminary results



10 Gb/s optical eye with COTS VCSEL driver



BER compared with SFP

problems encountered and future work plans

- Still working on a viable optical coupling solution.
- Electrical and optical cross talks.
- Working on a rad-tol driver ASIC (LOCld4, 8 and 12).
- LOCld8 will be submitted Dec. 2013.
- FR4 substrate for quick tests, ceramic substrate (about 1 cm x 1 cm) as final product.
- Rely on industry to solve the problem of operating VCSELs in ambient room environment.
- May also work with industry on optical coupling: