

# Optoelectronics Working Group Short Summary

**17:00** [GBT Project Status](#)

**Presenter(s):** Filip Francis TAVERNIER (*CERN*)

**Room:** Room, Congress Center

**Location:** Perugia, IT

**17:20** [VTRx Project Status](#)

**Presenter(s):** Dr. Jan TROSKA (*CERN*)

**Room:** Room, Congress Center

**Location:** Perugia, IT

**17:40** [LOC Project Status](#)

**Presenter(s):** Jingbo YE (*Southern Methodist University, Department of Physics*)

**Room:** Room, Congress Center

**Location:** Perugia, IT

**18:00** [US-CDRD Opto Project Status](#)

**Presenter(s):** Jingbo YE (*Southern Methodist University, Department of Physics*)

**Room:** Room, Congress Center

**Location:** Perugia, IT

**18:20** [Si-photonics at ANL](#)

**Presenter(s):** Alexander PARAMONOV (*Argonne National Laboratory (US)*)

**Room:** Room, Congress Center

**Location:** Perugia, IT

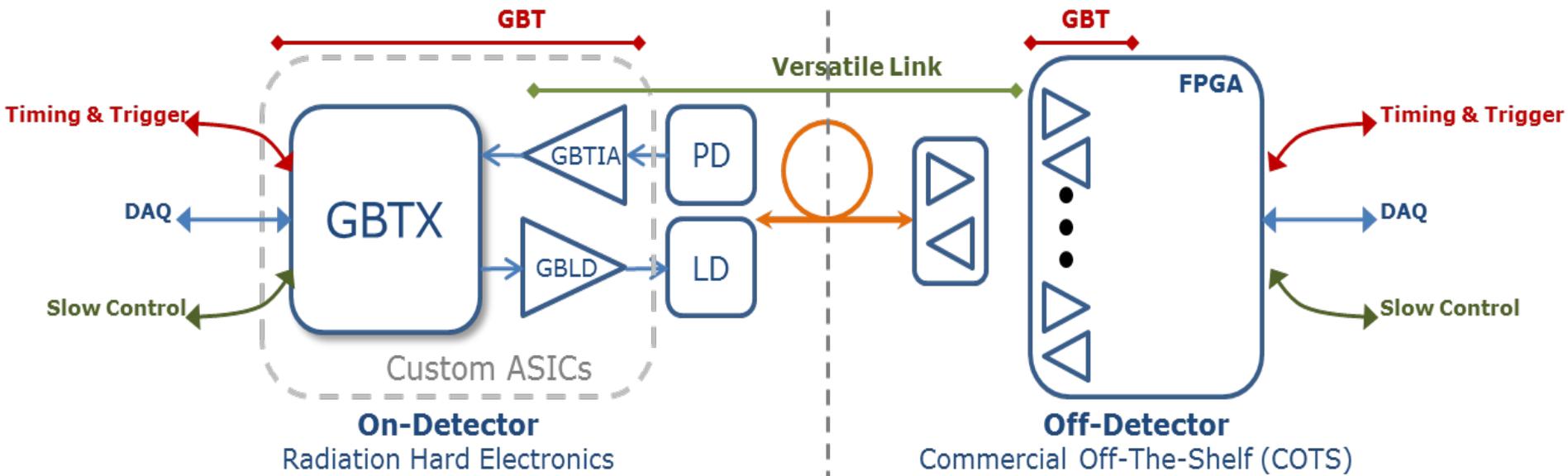
**18:30** [Si-photonics at CERN](#)

**Presenter(s):** Sarah SEIF EL NASR (*University of Bristol (GB)*)

**Room:** Room, Congress Center

**Location:** Perugia, IT

# 1. Rad Hard Optical Link (1/3)



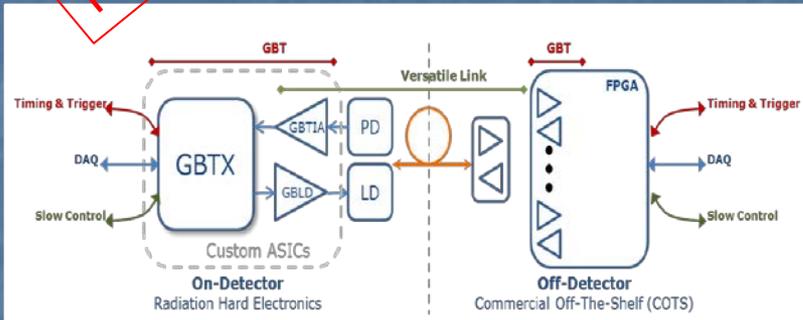
## ■ GBT

- GBTX, GBLD, GBTIA, GBT-SCA, GBTIP, GBT-FPGA

## ■ VL

- VTRx / VTTx, passives, backend

# Rad Hard Optical Link (2/3)



- |                   |    |                      |
|-------------------|----|----------------------|
| ■ GBTX            | OK | short iteration 2014 |
| ■ GBLD, GBTIA     | OK | prod 2014            |
| ■ GBT-SCA         |    | Submit Nov 2013      |
| ■ GBTIP, GBT-FPGA |    | Available            |
| ■ VTRx/VTTx       | OK | prod 2014            |

# Rad Hard Optical Link (3/3)

- VTRx / VTTx production = ~20'000 pcs

Radn Grade & User	TOSA		ROSA		Latch		VTRx		VTTx
	SM	MM	SM	MM	SM	MM	SM	MM	MM
Cal LHCb		16900		2900		9900		2900	7000
Cal HCAL	200	4400	200	400	200	2400	200	400	2000
Tk PIXph1	3000								
Cal ATLAS SmWh		1850		650		1250		650	600
Cal ATLAS LArg		150		150		150		150	
<b>Totals</b>	<b>3200</b>	<b>23300</b>	<b>200</b>	<b>4100</b>	<b>200</b>	<b>13700</b>	<b>200</b>	<b>4100</b>	<b>9600</b>

*Complete*
*MS ongoing*
*Pre-Prod*
*Eval.*

- Pledges so far
  - ALICE is now also showing interest, likely to represent a large (30-50%) extra number of links

# ATLAS Calorimeters

- LAr
  - 5.12Gbps
  - Direct interface to ADC
  - Mechanical constraints on FE board
  - Limited number of I2C lines
- TileCal

# LAr Calorimeter: LOC & MTx

For details on recent LOC results please see this talk at TWEPP:

<https://indico.cern.ch/contributionDisplay.py?sessionId=17&contribId=164&confId=228972>

There are two developments:

- The dual channel serializer:

- ✓ LOCs2: 2×8 Gb/s 16:1 serializer, prototype, tested to design goals.
- LOCx2: 2×5.12 Gb/s 8:1 serializer for ATLAS LAr phase-1, low latency, low power, with framing, CRC, and scrambling. In design. Will be QFN-88 packaged. Transmits any 12-bit serial output ADC data.

- The VCSEL drivers:

- ✓ LOCl1: 8 Gb/s VCSEL driver with I2C, QFN-24, tested to design goals. This is a generic VCSEL driver with SLVS inputs. With VCSEL at 8 Gbps < 200 mW.
- ? LOCl4: 4-ch open-drain array VCSEL driver. Tested but with problems.
- LOCl2: 2-ch TOSA VCSEL driver for MTx. Submission: Dec. 2013.
- LOCl8: 8-ch array VCSEL driver, try to fix problems identified with LOCl4. submission Dec. 2013.

Opto MTx development ongoing, derived from CERN SF-VTRx

# TileCal

Sasha Paramonov

- Validated Molex/Luxtera QSFP 4x10G TRx
  - Si-Photonics

# US Opto CDRD

**FNAL:** Coordinate irradiation testing at FNAL MTA beamline location, provide testing services for array modules, try to engage a corporate vendor (i.e. Reflex Photonics) to work with on array based transmitters.

**SMU:** Qualify commercial laser driver array ASICs. Design array based module (based on POD design concept) and fabricate prototypes for testing.

**OSU:** Design, fabricate, and test a multichannel VCSEL array driver capable of 10 Gbps/channel.

**Minnesota:** Develop and characterize materials (i.e. BaSTO, Barium Strontium Titanate) for fabrication of a rad hard Mach Zehnder Modulator. Fabrication of prototypes of the modulator.

**ANL:** Qualification of commercial light modulators; develop polarization control methods to control laser input polarization for modulators.

# Si-Photonics at CERN

Sarah Seif El Nasr-Storey

## Conclusions & Future Work



- Starting to investigate the potential of using silicon-based optoelectronic devices in HEP like environments, starting with the impact of radiation on the DC characteristics of some si-based optoelectronic components :
- ICE-DIP <http://openlab.web.cern.ch/ice-dip> , an Intel-CERN Doctoral Student Industrial Program ( within the FP7 framework ) :
  - project dedicated to the use of silicon photonics technology in data transfer systems.
  - Early Stage Researcher starting next week, spending time between CERN , Dublin City University, and Intel
  - ESR will work with Intel on designing the building blocks of a si-photonics link, where the effect of the harsh radiation environment at the HL-LHC will be investigated and used to modify the design
- Difficulties in pig-tailing the devices has meant that only DC tests have been possible so far. Should receive some pig-tailed samples of SOI-based modulators to irradiate at a total fluence test at the end of this year.
- Simulation tools are available which allow us to predict the effect of radiation on these types of devices, make use of the wide knowledge base available for radiation damage in silicon

# Summary of the Summary

- Rad Hard Optical Link common project is converging
  - Prod in 2014
- One size does not fit all
- Additional longer term developments
  - Arrays, 10G, new materials
- 4 groups working on Laser drivers in 3 technologies