
Microelectronics User Group Meeting Wrap-Up

TWEPP 2013, Perugia, IT
26/9/2013

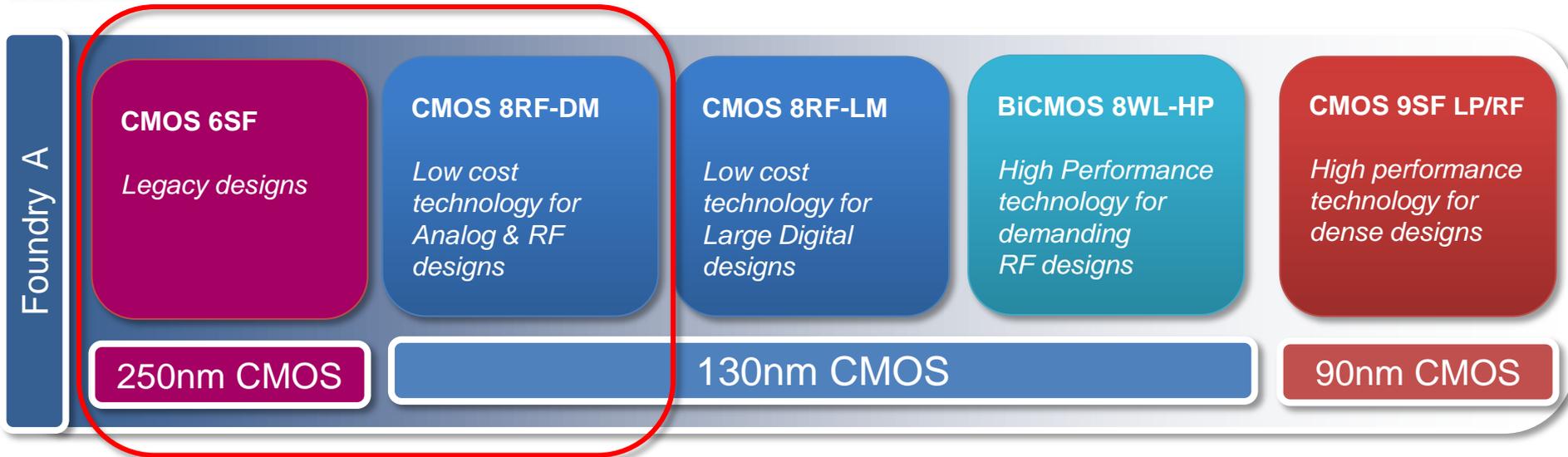


Agenda

- “News on foundry access services via CERN”
by Kostas Kloukinas (CERN) (15’)
- “Status of 65nm technology access, distribution and IP block development .”
by Sandro Bonacini (CERN) (25’)
- “Open Discussion”
- “CAE Tools for the European HEP community”
by ”EUROPRACTICE UK (10’)



Supported Technologies



Active technology nodes:

- Legacy technology: CMOS6SF 250nm
- Mainstream technology: CMOS8RF 130nm
 - 95% of ASIC projects on DM variant
- Advance technology: CMOS 65nm
 - For LHC upgrade applications.
- Alternate technology: CMOS 130nm



Foundry Services News

■ Contract with Foundry A

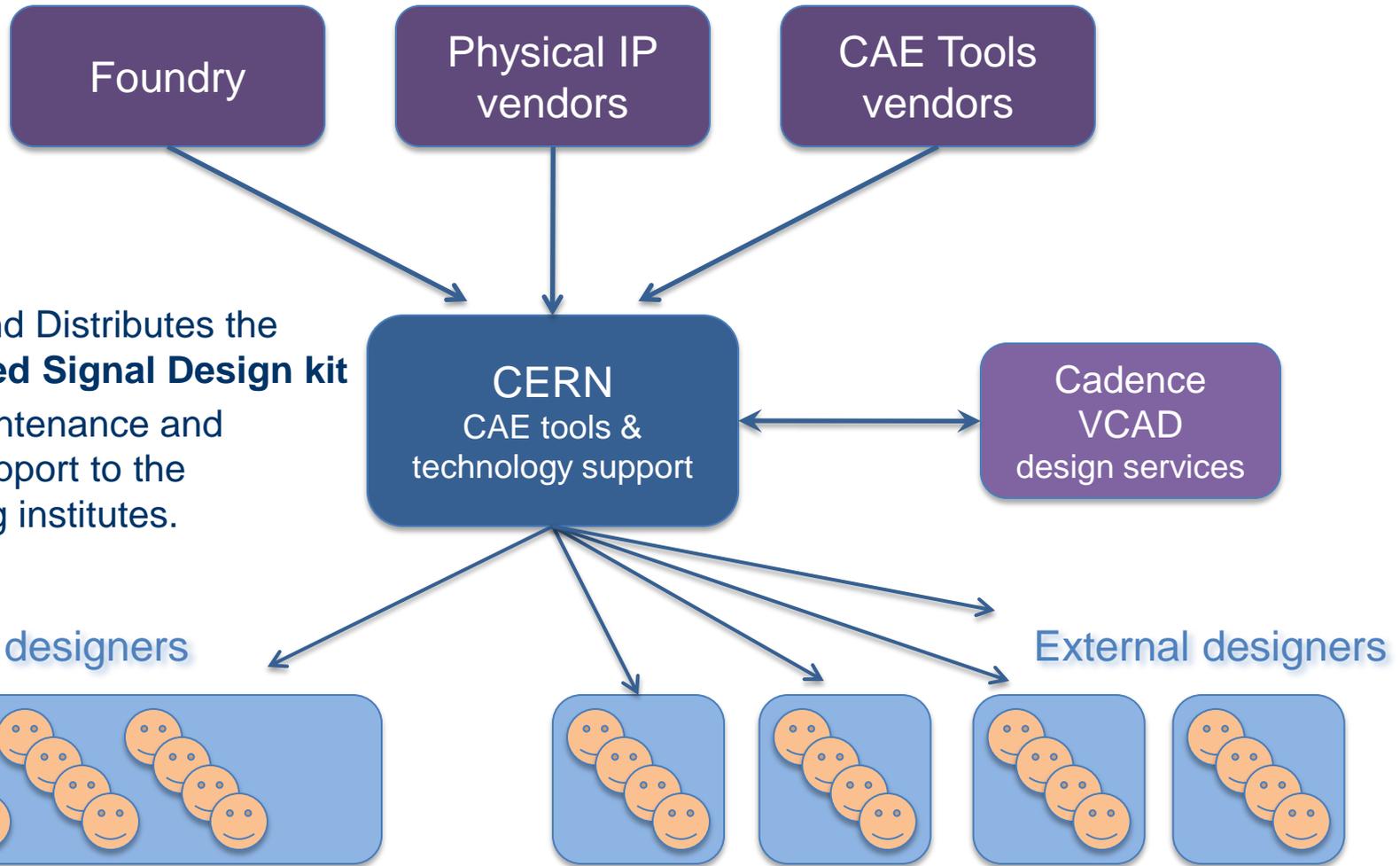
- ❑ Contract renewed for 3 years (2013-2015)
- ❑ Same pricing conditions apply with some minor changes
- ❑ Confidential Disclosure Agreement (CDA) with institutes will expire by the end of 2013
 - Renewal procedure has started
Institute signatory authorities are already contacted by e-mail
ACTION: verify that your institute has renewed the CDA with the foundry to maintain uninterrupted access to technology

■ Contract with Foundry B

- ❑ Foundry access via an intermediary silicon broker
- ❑ Contract preparation is in the final stage
- ❑ Long procedures for negotiating technology information disclosure legal terms and contractual pricing conditions for prototyping and production services
- ❑ Contract covers a period of 5 years (2013-2017)
- ❑ More information on the next presentation by Sandro Bonacini.



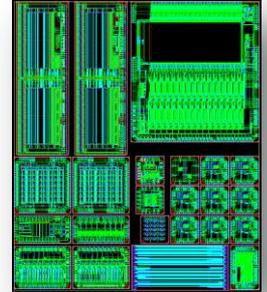
Support for Foundry A



- Compiles and Distributes the **130nm Mixed Signal Design kit**
- Provide maintenance and technical support to the collaborating institutes.

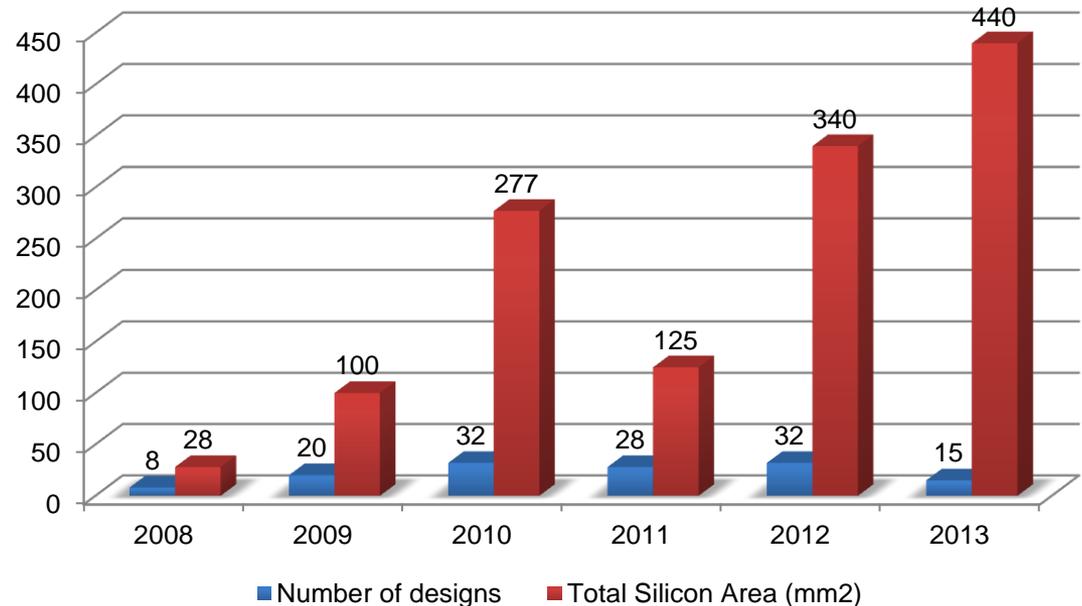
130nm MPW activity

- CERN participates on all MOSIS MPW runs (4 runs/year) and organizes ad-hoc MPWs directly with the foundry for high volume and/or area demanding designs
- Prototyping and Engineering run costs are kept the same for the last 2 years.



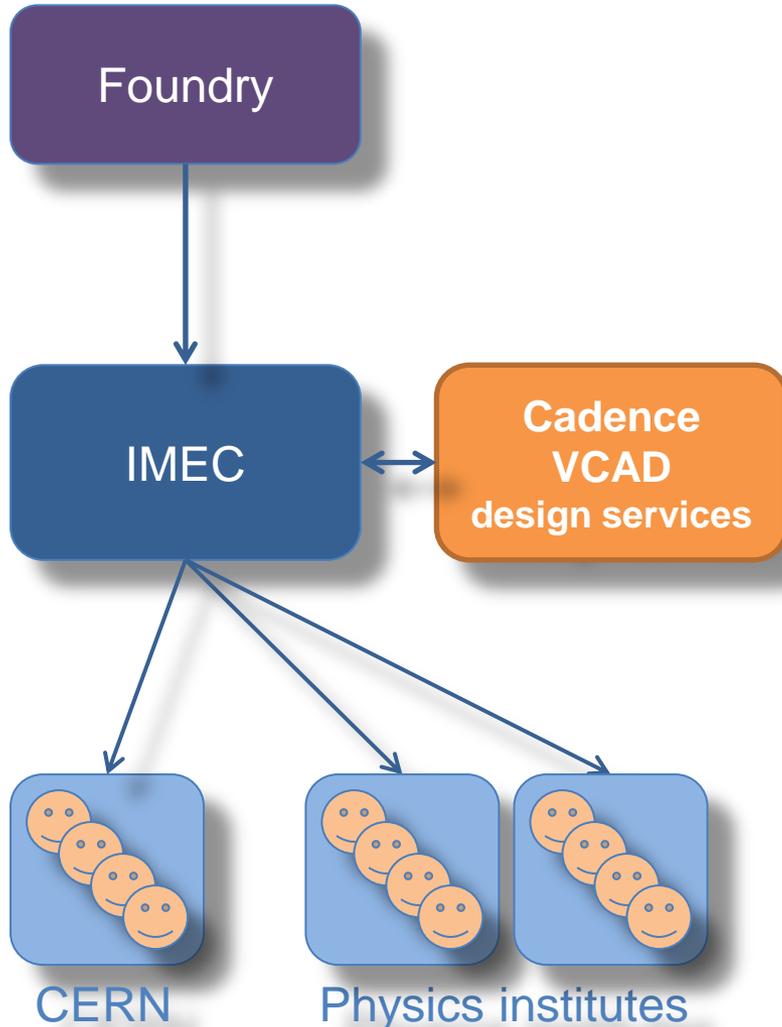
CMO8RF (130nm) Prototyping activity

- Evolution of the Prototyping activity on CMOS8RF for the last 6 years
- CMOS8RF-DM (3-2-3) is the dominant metal stack





Support for Foundry B



- Distribution of package to institutes done by IMEC
 - ❑ Sign NDA with institutes
 - ❑ Distribute the M/S design kit and workflows
 - ❑ Provide maintenance and updates in collaboration with VCAD



65nm Mixed Signal Design kit

■ Objectives

- Development of a “Design Kit” for Mixed Signal environments.
 - With integrated standard cell libraries.
 - Establish well defined Analog & Mixed Signal design workflows.
 - Implemented on modern versions of CAE Tools.
 - Physical Layout views available.
 - Suitable for analog, digital and mixed design

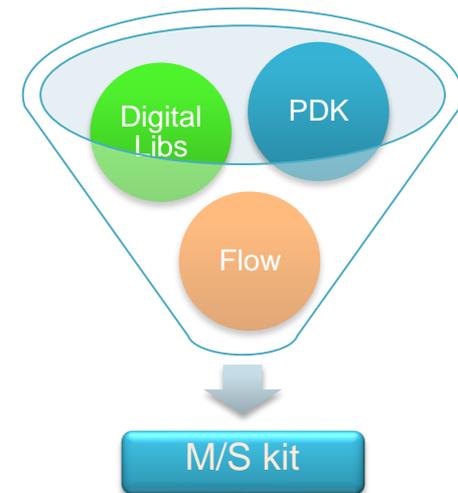
- Foundry database not made for full M/S interoperability
 - Technology library and PDK in OA (and CDB)
 - Digital libraries in CDB only
 - Must be ported to OA for full M/S flow

■ Integration work done by VCAD (Cadence)

- Many modifications in the technology file
- Validated by CERN

■ Work with VCAD started Apr. 2013

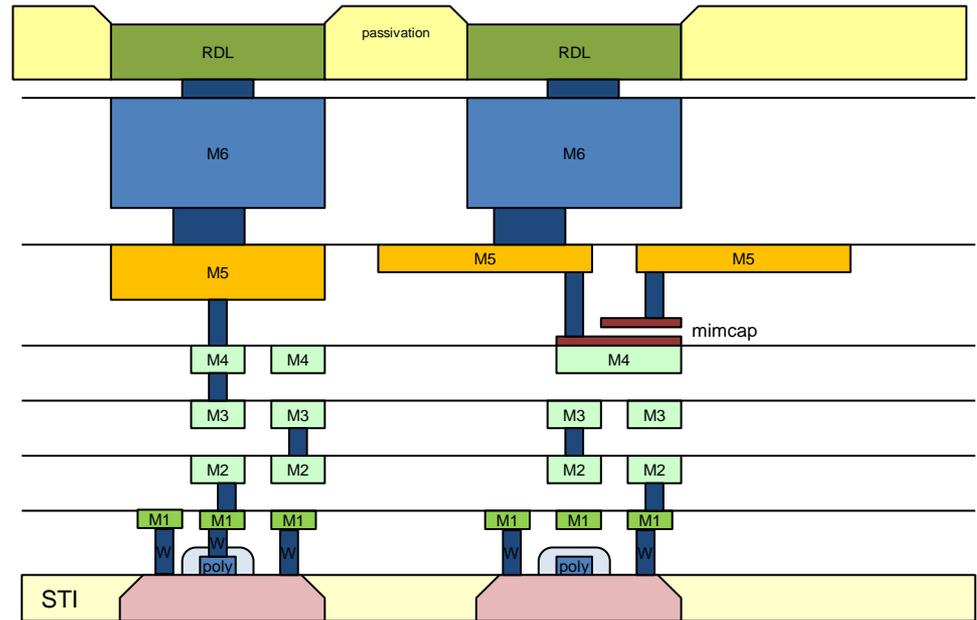
- Preliminary version delivered to CERN this month
- Final version target date: 31st October 2013





Supported metal stacks and libraries

- CERN mixed signal (M/S) kit will be supported for:
 - 2 metal stacks
 - 6+1 metals (“CERN metal stack”)
 - 4-thin, 1-thick, 1-UTM , RDL
 - 9+1 metals (compatible with IMEC mini@sic)
 - 7-thin, 1-thick, 1-UTM , RDL
 - + 220 k\$ for mask set (!)
 - 2 choices of std. cell libraries
 - 9-tracks, standard-Vt
 - tcbn65lp
 - 7-tracks, high-Vt
 - tcbn65lpbwp7thvt





Rad-hard libraries

- Standard cell & IO pad libraries from foundry suffer from radiation effects
 - NMOS leakage
 - PMOS tend to turn off + loss in transconductance

- Re-characterize standard cells libraries
 - PMOS drive loss results in speed loss with TID (above ~50Mrad)
 - Create standard cell library timing (liberty file) for radiation corner

- Develop Radiation hardened I/O pad library
 - Rated for 1.2V or 1.0V
 - Only core devices, thin gate oxide
 - Subcontract the development work for rad-hard ESD circuitry

- Access to layout views & modification allowed by foundry
 - Clause of no-redistribution except to signatories of NDA (list to be updated annually)
 - Discharge of any foundry liability for modified libraries
 - Modified library has to be given back to foundry
 - Library NOT to be used with other foundry !!!



Rad-hard IP Blocks

- Rad-hard SRAM compiler
 - Single-port / pseudo-dual-port
 - Minimum size: 128 words of 8 bit
 - Max size: 1k words of 256 bits
 - Specifications on minimum W of transistors to avoid leakage and drive loss
 - $W_{\text{PMOS}} > 500\text{nm}$, $W_{\text{NMOS}} > 200\text{nm}$
 - Design outsourced Jul. 2013
 - Delivery expected Jan. 2014

- ADC, bandgap
 - Delivery expected 2014, Q2



Open discussion

- Addressed many issues concerning access to Foundry B services for the 65nm process
 - Technical (Design kit, IP blocks and metal stack options)
 - Non technical (NDA clauses, fabrication cost etc)
 - Institutes must sign the specially prepared 3-party NDA for Foundry B access services that permits the use of the technologies in collaborations
 - Export restrictions apply as for Foundry A
 - Prototyping costs
- Foundry B 130nm process
 - Judicious choice for future projects
 - Need radiation hardness validation and MS design kit development
- CAE tools
 - Europractice distribution of CAE tools for the HEP community
 - Design database management CAE tool for teamwork.

A nighttime photograph of the Globe of Science and Innovation at CERN. The globe is illuminated from within, showing its metallic structure. The background is a dark blue night sky with stars and a bright meteor streaking across the right side.

Thank You