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A new approach to interfacing on-detector electronics

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The current off-chamber readout chain in the ATLAS experiment consists of sub-detector specific ReadOut Drivers (RODs), typically 9U VME cards, which receive data from a number of front-end links. The RODs build event fragments and forward these via point-to-point links, the Read-Out Links (ROLs) to the ReadOut System (ROS). The functionality of the RODs, not only consisting of fragment building but also of the associated error handling and for some subdetectors processing of the event data and also of support for calibration, is implemented in FPGAs and DSPs. For the Readout of new muon detectors to be installed during LS2 and for the Readout of all detectors after LS3 a new approach is foreseen, in which as much as possible functionality is moved to software. A similar system has been proposed for the LHCb experiment electronics upgrade in LS2.

In this paper we present the new approach. We foresee that first results of tests can also be presented.

Summary

A new approach to interfacing to on-detector electronics

The upgrade of the LHC planned during LS3 (˜2022) will necessitate major changes in the ATLAS trigger/DAQ system. The current first-level trigger will be augmented with a track trigger and be subdivided into two levels: an L0 trigger on the basis of calorimeter and muon detector with an accept rate of at maximum 500 kHz and an L1 trigger also making use of tracking detector data with an accept rate currently foreseen to be at maximum 200 kHz. The ATLAS detector will need to be read out at the new L1 accept rate, which currently is at maximum 100 kHz. On-detector electronics of the calorimeters and muon detectors, apart from the "small wheels", will be completely or to a large extent be replaced, while a complete new inner detector with associated on-detector electronics will be installed. All detector systems are foreseen to be read out via GBT links, either directly connected to the on-chamber electronics, or via off-detector pre-processors for the calorimeters. New muon detector "small wheels" will be installed already during LS2. The readout of the detectors (sTGCs and MicroMegas detectors) will be done with GBT links and the organisation of the off-chamber readout will be similar to the organisation foreseen for post-LS3 running. Also the

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The evolution of general purpose processors allows to implement ROD functionality now implemented in FPGAs in software, and further evolution of the technology can be expected at the time scale of LS2 and LS3. Also further evolution of network technology is to be expected, 40 Gb/s and 100 Gb/s Ethernet links for example at acceptable cost are on the horizon, allowing to concentrate the data from tens of GBT links on a single network link.

In view of this and in view of the desire to keep any special-purpose off detector electronics as simple and subdetector independent as possible a new readout architecture has been defined in which the ROD functionality is implemented as much as possible in software. The equivalent of the current ROD system is foreseen

to be implemented as a combination of dedicated electronics interfacing to the GBT links and of server nodes receiving data from the dedicated electronics via a local area network. The dedicated electronics has been given the name FELIX (Front End LInk eXchange). The task of FELIX is not only to forward event data, but also to forward L1 and possibly L0 trigger information, as received from the TTC or its successor, to the on-chamber electronics, and to provide support for the communication of the Detector Control System (DCS) via GBT links with on-chamber electronics and on-chamber sensors. The latter functionality demands continuous running of FELIX and support for this type of communication. Handling of data received via the GBT links should essentially consist of forwarding the data to the server nodes via the general purpose network based on routing tables loaded in the FELIX system. A similar system has been proposed for the LHCb experiment electronics upgrade in LS2. Protocol definitions and implementations will be useful for and be applicable to both systems.

In this paper we present the new approach as outlined in this summary. We foresee that first results of tests can also be presented.

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