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Digital Column Readout Architectures for Hybrid Pixel Detector Readout Chips

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In this paper, two digital column architectures suitable for sparse readout of data from a pixel matrix in triggerless applications are presented. Each architecture reads out a pixel matrix of 256x256 pixels with a pixel pitch of 55um.
The first architecture has been implemented in the Timepix3 chip, and this is presented together with initial measurements. Simulation results and measured data are compared.
The second architecture has been designed for Velopix, a readout chip planned for the LHCb upgrade. Unlike Timepix3, this has to be tolerant to radiation-induced single-event effects.
Results from post-layout simulations are shown with the detailed circuit architectures.

Summary

In this paper, column readout architectures focused on pixel detector readout chips with 65,536 pixels of 55 um x 55 um, suitable for continuous, sparse readout without trigger signal are presented. A sparse readout architecture reads only the pixels which contain event information, and continuous readout keeps pixels sensitive at all times with only a small readout related dead time. Operation without trigger requires reading out all hit information with no event-filtering by an external signal.

Timepix3 [1] was fabricated in 130 nm CMOS in spring 2013. It has been designed as a general purpose pixel detector readout chip targeted for many applications. The double column readout architecture in Timepix3 has been implemented using a low-power (high Vt), high-density (350 kgates/mm^2), custom-made CMOS standard cell library. The architecture has been designed by localising critical timing paths and making global communication asynchronous. This flexibility allows clocking the periphery of the chip with a different frequency (up to 80 MHz) than the pixel matrix (up to 40 MHz). One readout column consists of two pixel columns abutted together. Locally in a column, the readout logic is shared between a region of 2x4 pixels (a super-pixel). One double column delivers 2 Mhits/s from a pixel matrix to the periphery.

Each column uses a two-stage token ring arbitration with 8 token stations per super pixel and 64 stations per double column. The token is fully synchronous within a column. Data is transported from pixels to End-of-Column using a 2-phase handshake protocol over 4 handshake cycles. In Timepix3, event information is encapsulated into a 48-bit pixel packet containing a 14-bit coarse time (40 MHz), a 10-bit time-over-threshold measurement and a 4-bit fine time (640 MHz) information in addition to a 16-bit pixel address. For characterising the chip, a custom test system has been constructed based on programmable logic. Initial measurements of the efficiency of the Timepix3 architecture are presented.

Velopix is targeted specifically for the LHCb upgrade [2] and a fully synchronous design has been chosen. Local pixel logic has been implemented using high-density cells and global communication is driven by stronger cells from a commercial library. The column architecture has been designed for maximum peak rate of 8.8 Mhits/s per super pixel column. The architecture has been protected against single-event-upsets by triplicating on-pixel configuration registers, state machine registers and FIFO pointers.

Locally in a column, the readout logic is shared by a super-pixel of 4x4 pixels. A data encoding scheme has been implemented in this region to share coarse time and address information with a cluster of hits formed by the same track. Particle hits create clusters with an average size of 2.2 pixels and a reduction of over 25% of data volume can be achieved using this encoding scheme compared to reading out individual pixels. The

format has been optimised to simplify decoding at the next level of electronics where the high data rates result in complex algorithms for event-reconstruction.

For future work, the characterization of Timepix3 readout architecture will continue. Implementation of Velopix will proceed aiming for a maximum data rate of about 17 Gbit/s/chip.

References:
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[2] J Buytaert 2010 JINST 5 C12035 doi:10.1088/1748-0221/5/12/C12035

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