



Pixel front-end development

in 65 nm CMOS technology

M. Havránek, T. Hemperek, T. Kishishita, H. Krüger and N. Wermes

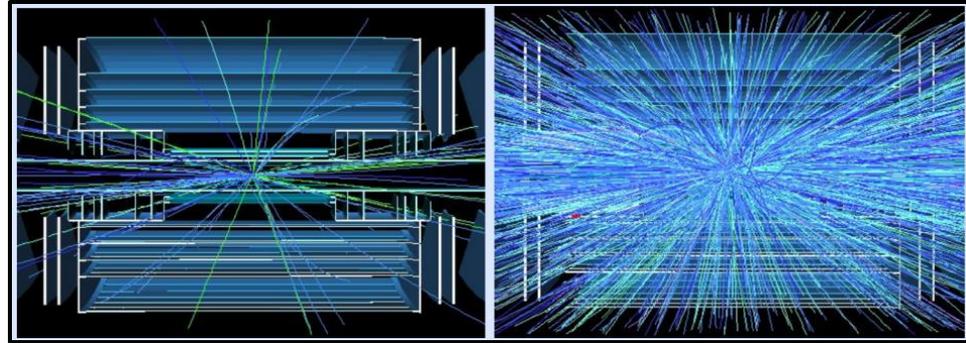
24th September 2013, TWEPP 2013, Perugia Italy

Outline

- Motivation for 65 nm
- Test chip FE-T65-1
- Measurements with FE-T65-1
- Summary

New pixel front-end chip needed

- HL-LHC in $\sim 2022 \rightarrow 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$
- Higher luminosity, higher hit rate
- Higher radiation doses
- Most critical are the innermost pixel layers



Smaller pixel size

Hybrid detector
Monolithic detector ...

3D integration (130 nm)
65 nm technology

ATLAS Pixel FE chips

<p>FE-13</p>	<p>FE-14</p>	<p>FE-?? Preliminary</p>
250 nm technology	130 nm technology	65 nm technology
pixel size $400 \times 50 \mu\text{m}^2$	pixel size $250 \times 50 \mu\text{m}^2$	pixel size $125 \times 25 \mu\text{m}^2$
3.5 mil. transistors	80 mil. transistors	~ 500 mil. transistors

65 nm

The smallest transistor in HEP !!

Specification for the new ATLAS pixel FE chip

- **Sensor thickness (planar or 3D):** 100 – 150 μm \rightarrow MIP signal $\sim 10 \text{ ke}^-$
- **Pixel size:** $\sim 150^* \times 25 \mu\text{m}^2$
- **Threshold:** $\sim 1 \text{ ke}^-$
- **Threshold dispersion:** $\sim 100 \text{ e}^-$
- **Noise:** $< 200 \text{ e}^-$ @ $C_{\text{IN}}^* = 400 \text{ fF}$, $I_{\text{LEAK}}^* = 100 \text{ nA}$
- **Power dissipation:** 3.5 mW / mm^2
- **Hit rate:** $\sim 1\text{GHz} / \text{cm}^2 \Rightarrow \sim 30 \text{ kHz} / \text{pixel}$
- **Hit loss:** $< 0.5 \%$ (rather 0.1 %)
- **Radiation tolerance:** 1 Grad, 2×10^{16} neutrons
- **Technology:** 65 nm

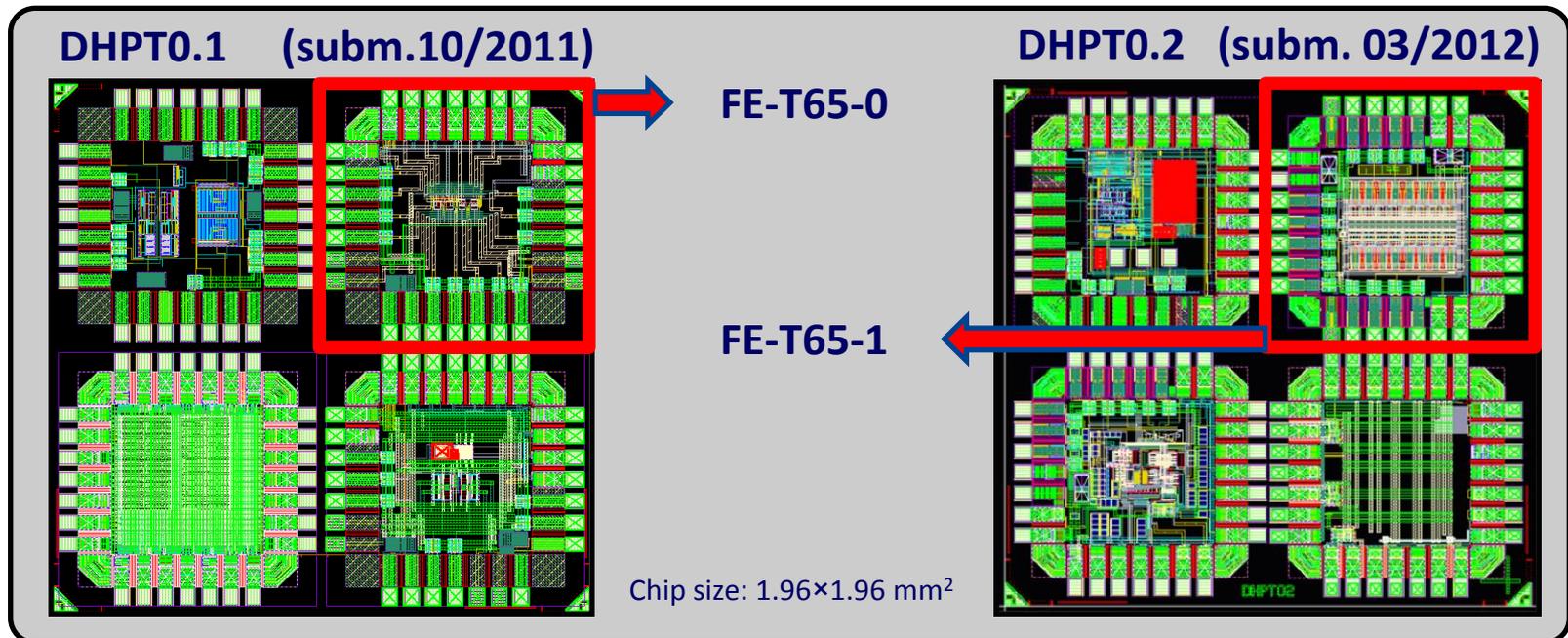
M. Garcia-Sciveres,

Future pixel chips design meeting 19th February 2013

* Parameters which are not yet clear

65 nm prototypes designed in Bonn

- Our goal: explore potential of 65 nm technology
- Design of test-chips to study analog performance of 65 nm technology
- Analog FE-prototypes:
FE-T65-0, FE-T65-1
- Other prototypes: SAR-ADC, PLL, LVDS, synthesized logic for SEU tests

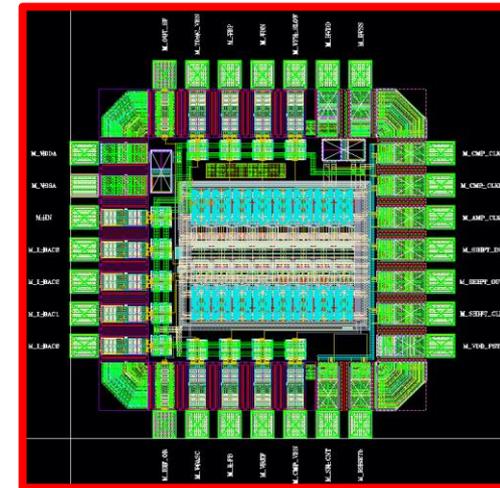


FE-T65-1

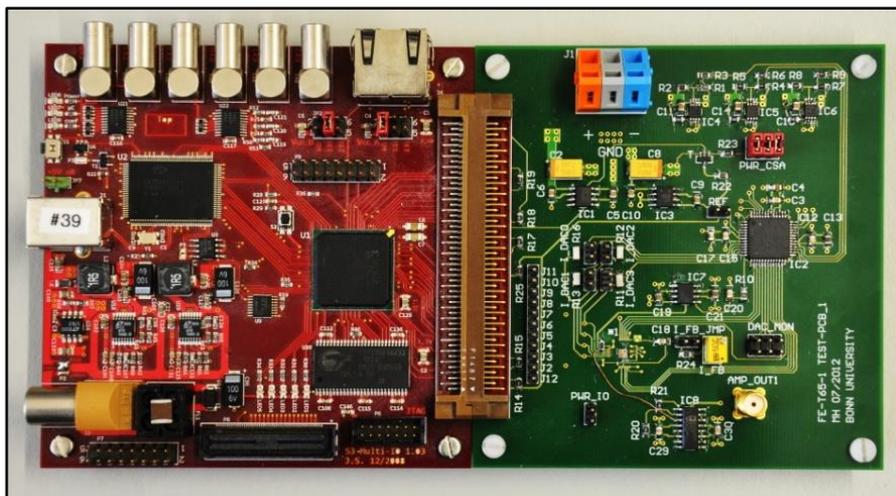
- Array of 32 pixels of four different versions:

Version	CSA	Comparator
1	Continuous reset	Continuous
2	Continuous reset	Dynamic
3	Switched reset	Continuous
4	Switched reset	Dynamic

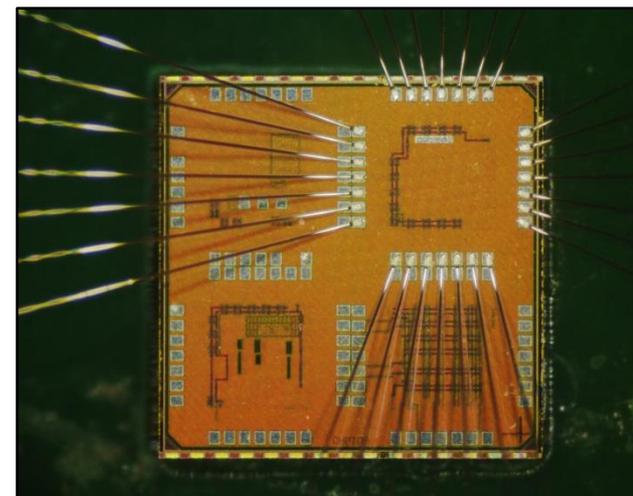
FE-T65-1 - layout



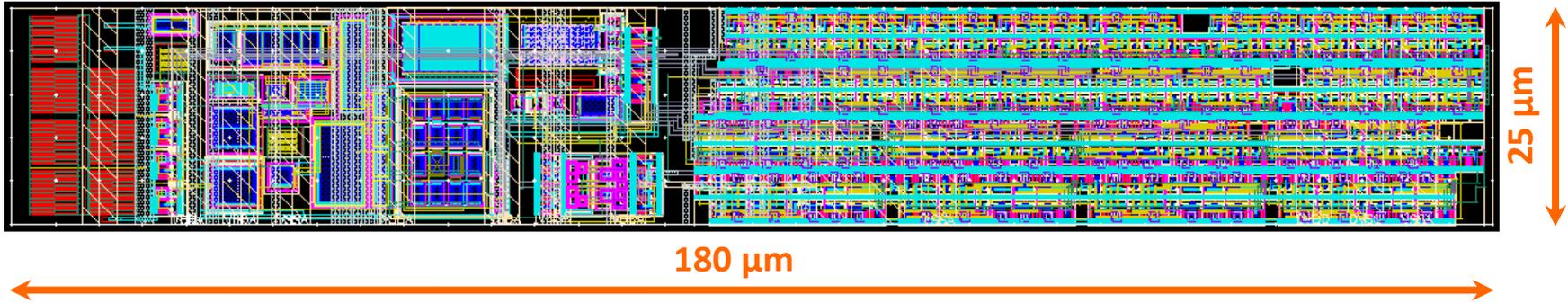
Test system



Wire-bonded FE-T65-1



FE-T65-1 – single pixel

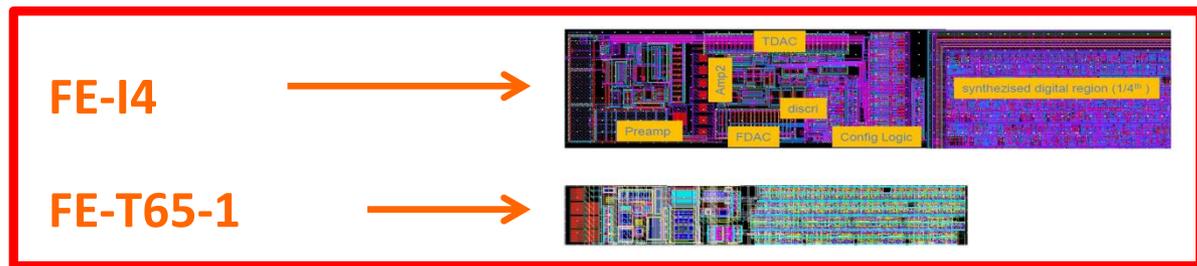


▪ Analog part:

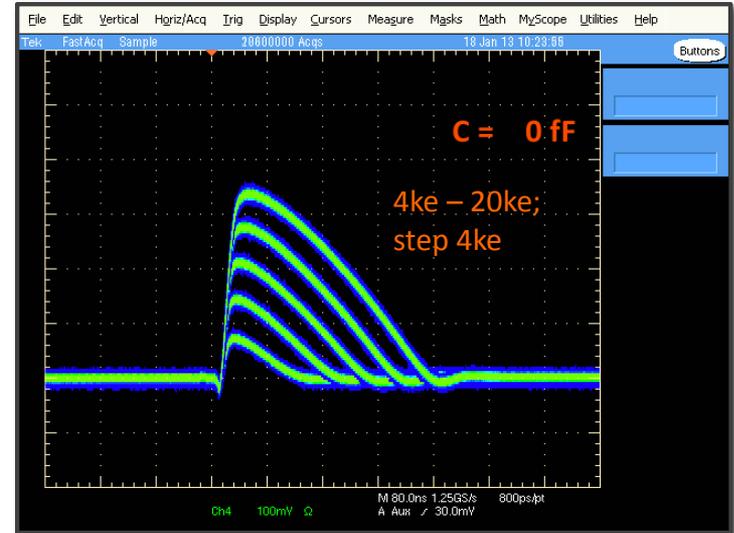
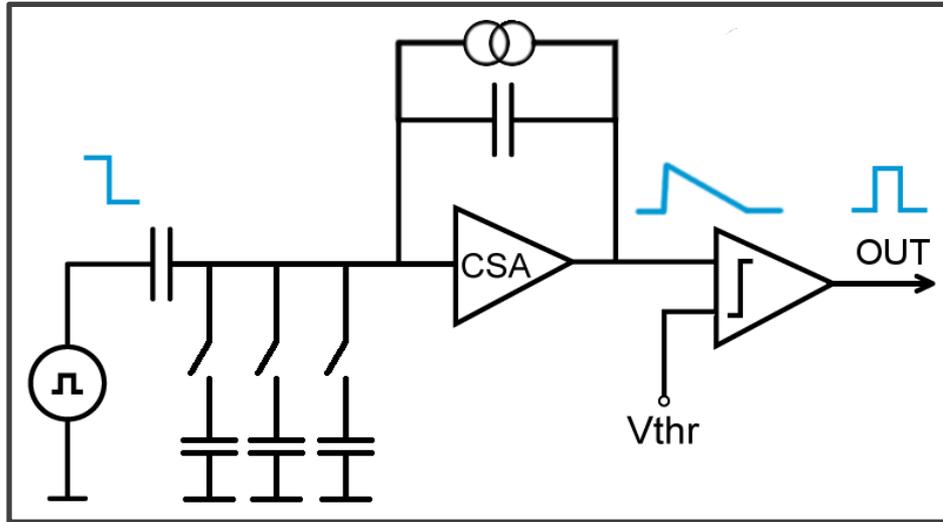
- CSA tunable input capacitance
- programmable charge injection
- FDAC – tunable feedback current
- TDAC – tunable threshold
- comparator

▪ Digital part:

- identical for every pixel
- configuration register 15-bits
- 8-bit shift register-counter
- mask-bit
- HitOr

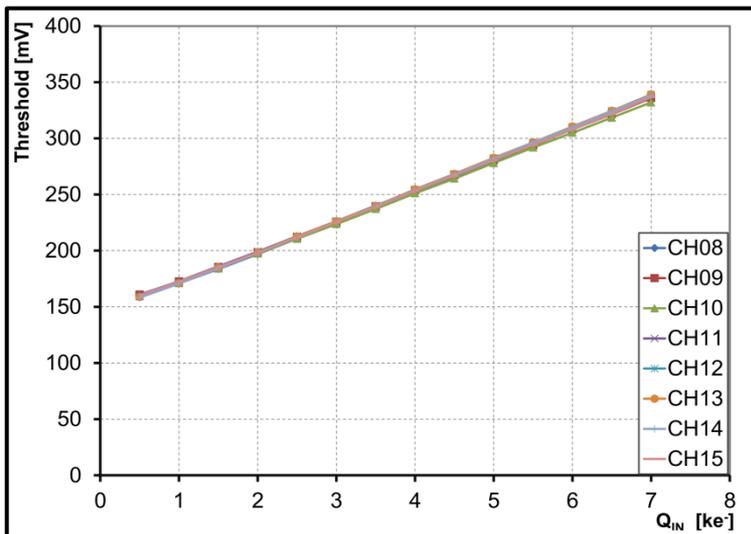


Charge sensitive amplifier with continuous reset

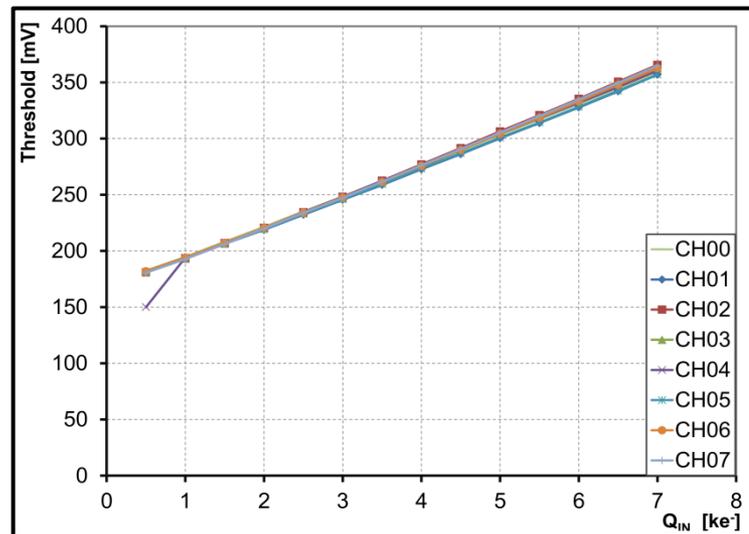


Return to baseline $\sim 240 \text{ ns}$

Version with continuous comparator

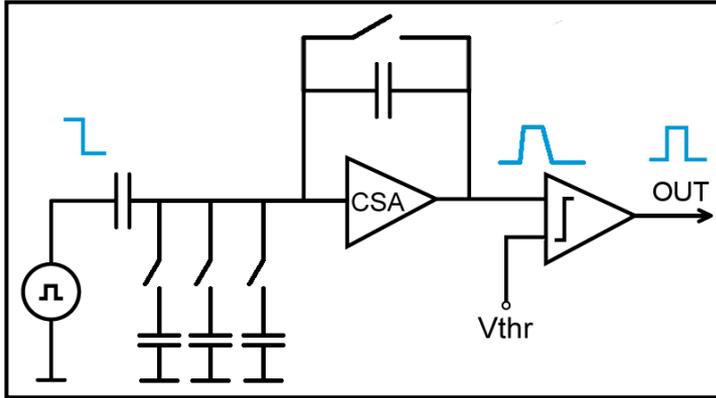


Version with dynamic comparator

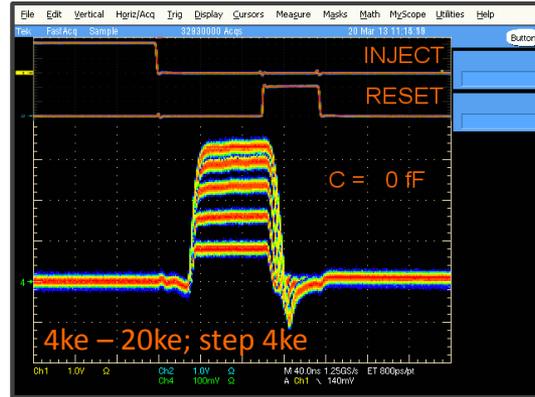


Charge sensitive amplifier with switched reset

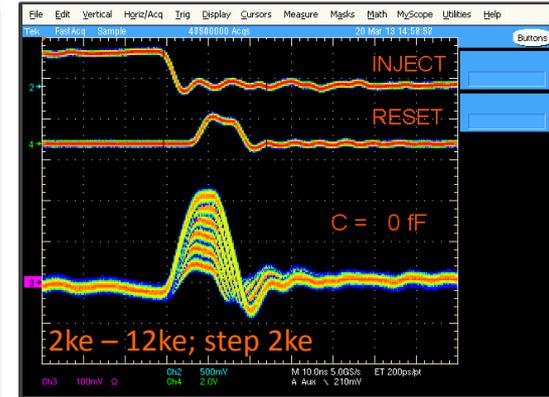
FE – with switched CSA



Slow mode (6.25 MHz)



LHC Mode (40 MHz)

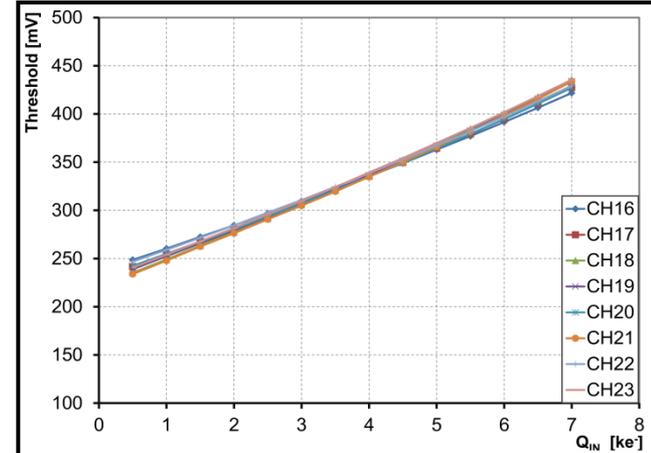
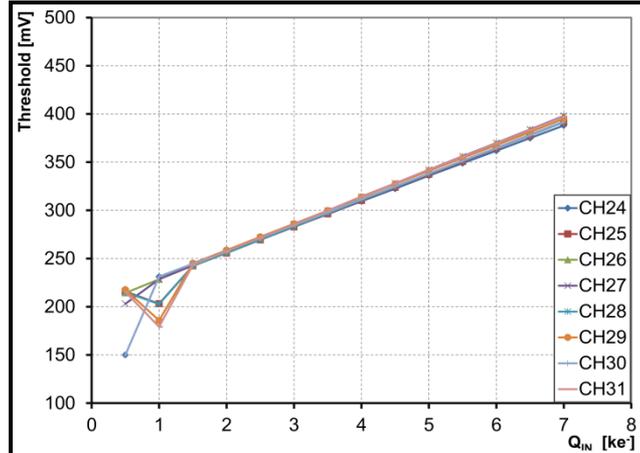


POWER (CSA only) = 11 μ W

w.r. to 6.8 μ W (cont. CSA)

Version with dynamic comparator

Version with continuous comparator



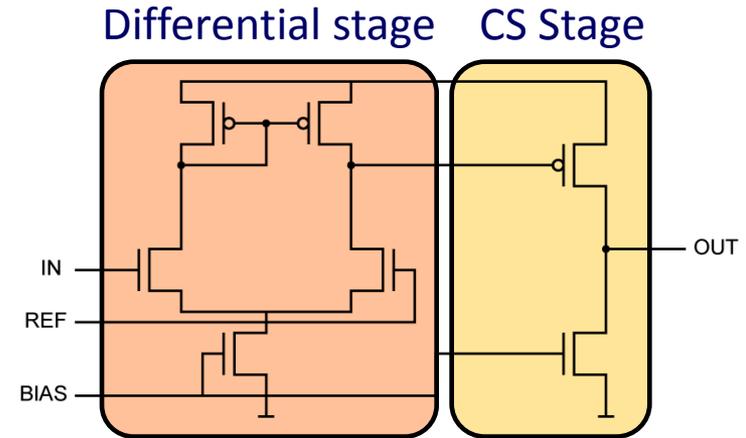
Properties of switched CSA:

- no ballistic deficit
- higher gain
- fast reset
- requires synchronous operation

Continuous vs dynamic comparator

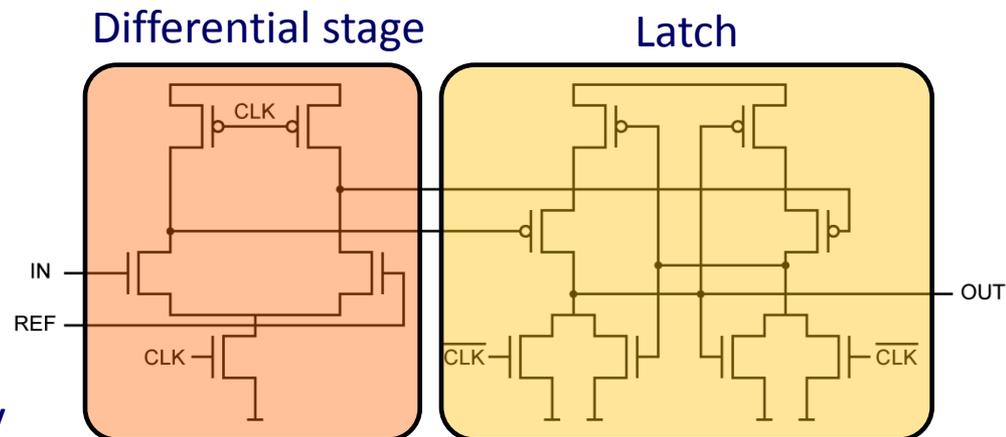
Continuous comparator

- Popular 2 stage architecture
- Asynchronous operation
- Consumes power even idle state



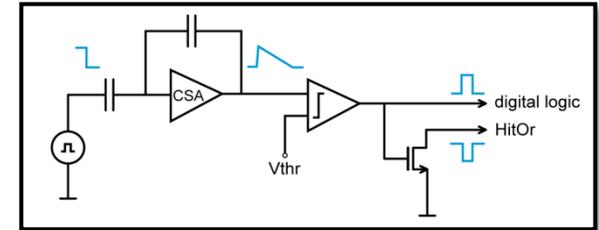
Dynamic comparator

- Based on latch in metastable state
- Does not consume power in idle state
- Active only when CLK edge comes
- Power proportional to CLK frequency

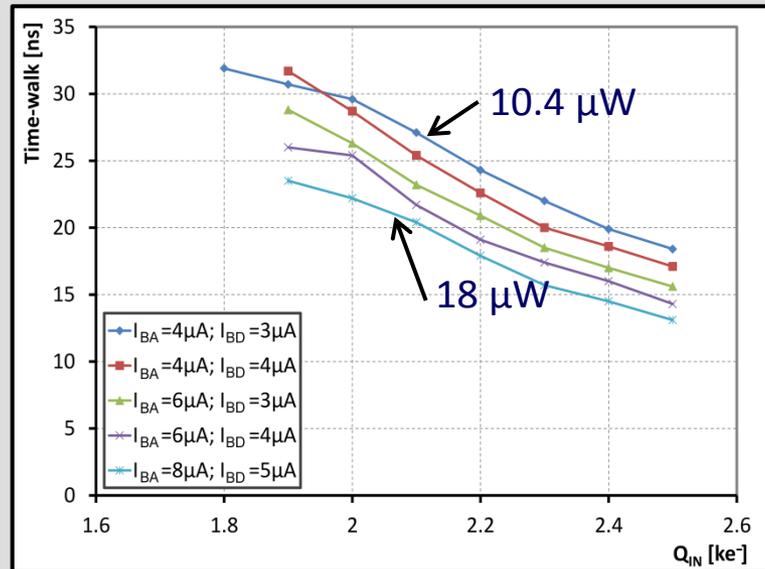
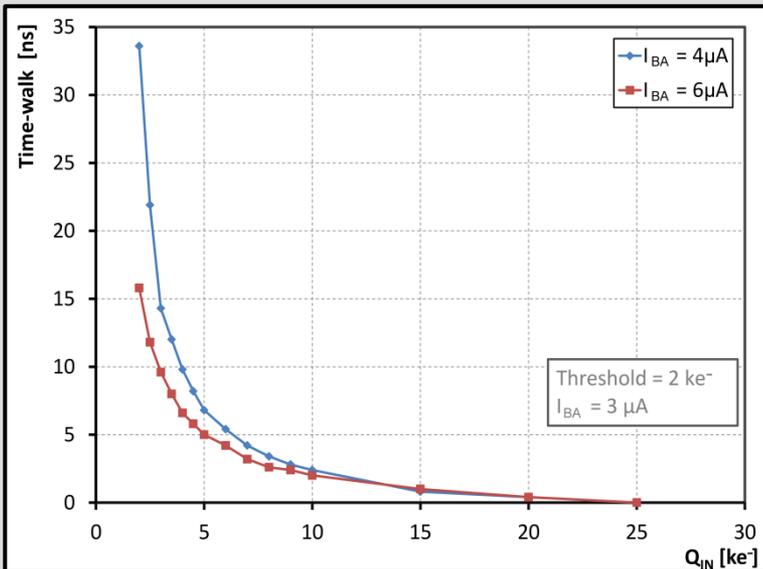


Time-walk measurement

- Time-walk: charge dependent propagation time
- The most significant delay is just around threshold
- If time-walk > 25 ns → wrong time-stamp



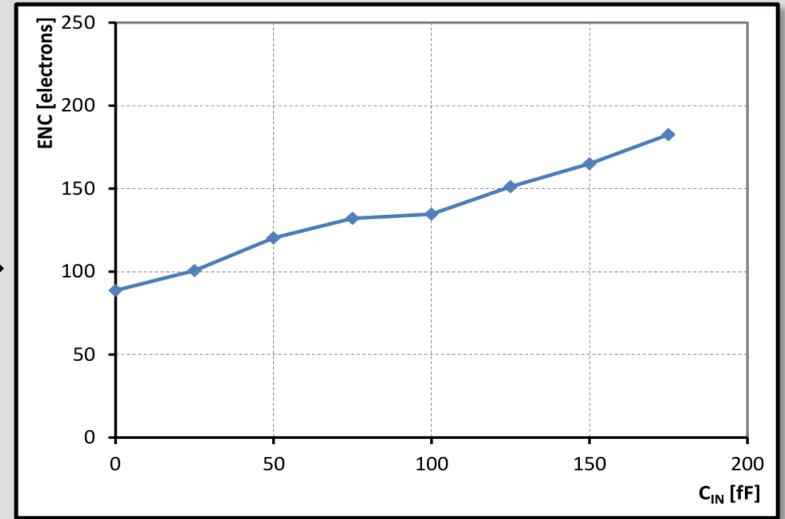
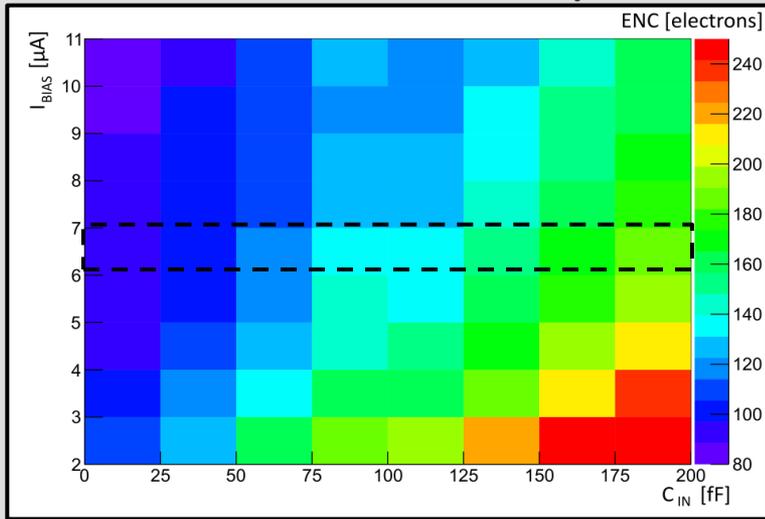
Continuous CSA + continuous comparator



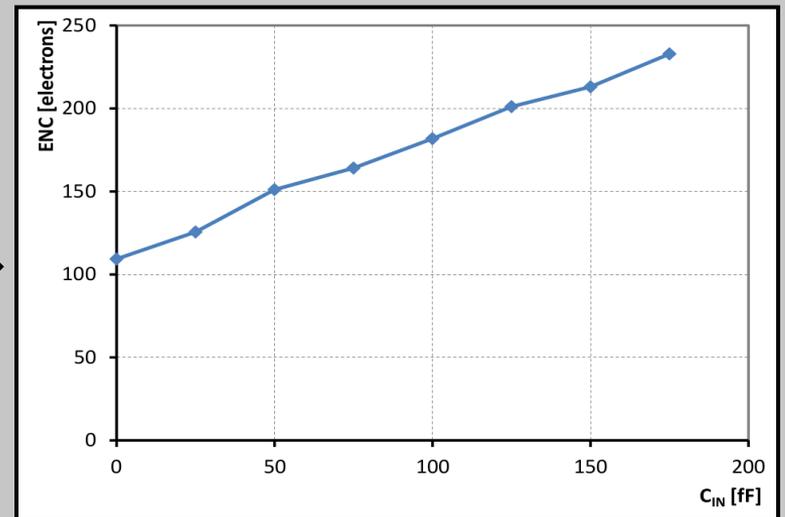
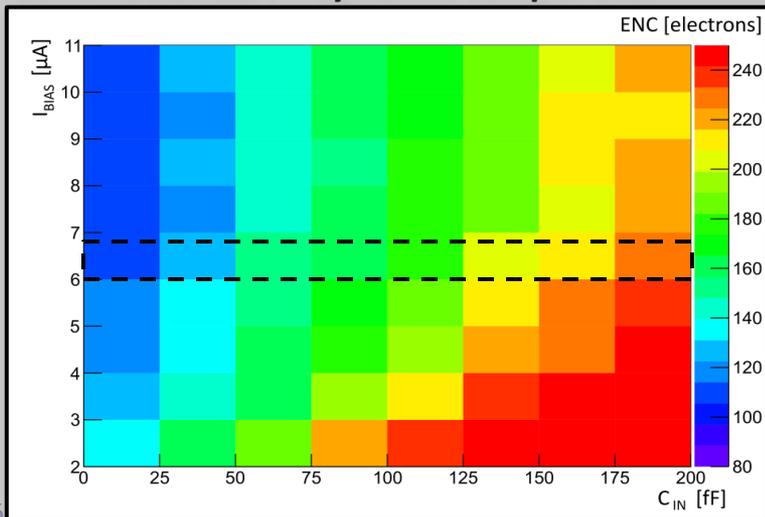
- No delayed hits observed with dynamic comparator (low power consumption of 10.6 μW /pixel is preserved)
- No delayed hits observed with switched CSA

Noise – continuous CSA

Continuous CSA + continuous comparator

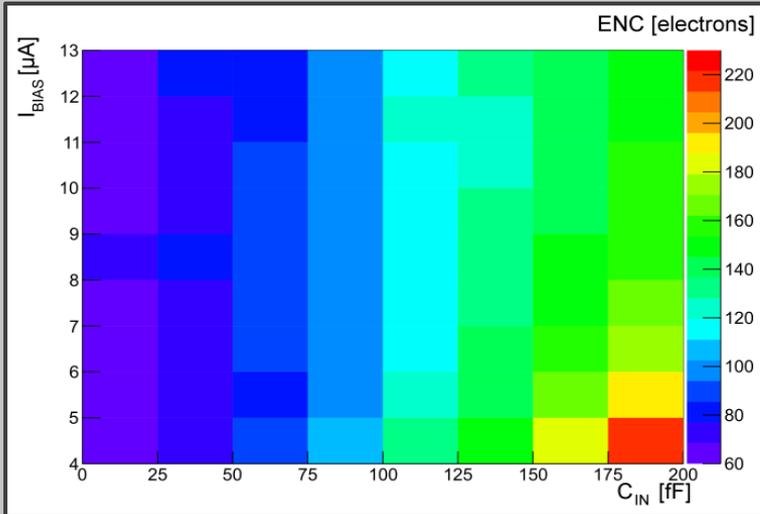


Continuous CSA + dynamic comparator

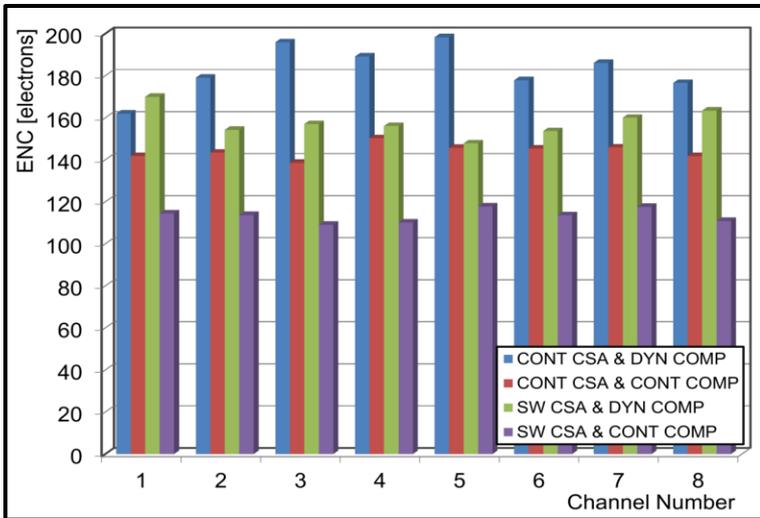
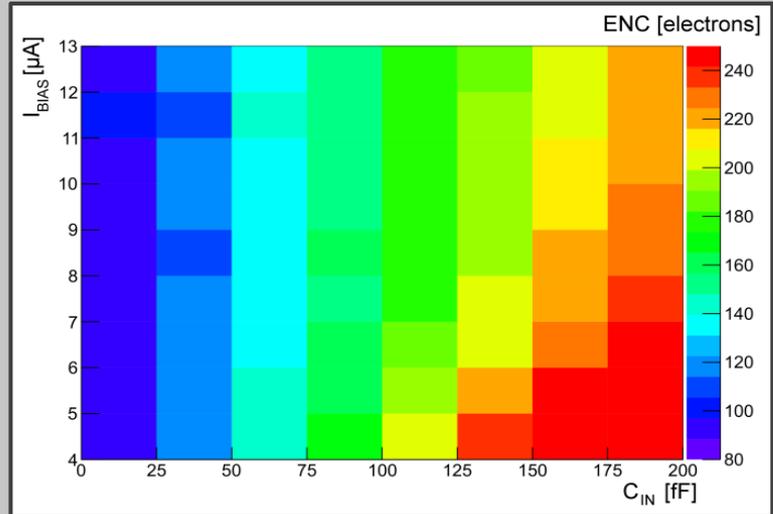


Noise – switched CSA, comparison of all versions

Switched CSA + continuous comparator



Switched CSA + dynamic comparator

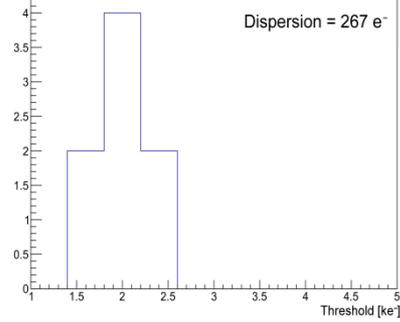
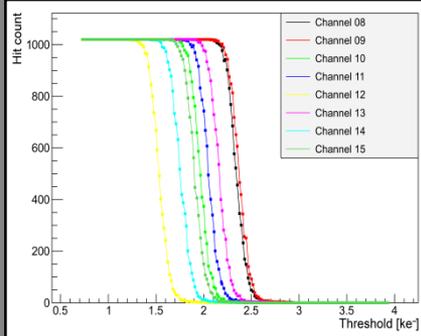


CSA	Comparator	<ENC> [e ⁻]	P [μW]
Continuous	Continuous	144	10.4
Continuous	Dynamic	183	10.6
Switched	Continuous	113	14.6
Switched	Dynamic	157	14.8

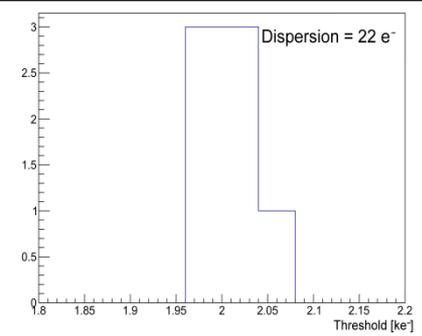
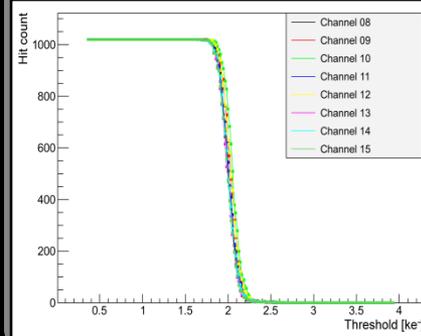
Threshold dispersion

CONTINUOUS CSA AND CONTINUOUS COMPARATOR

BEFORE TUNING

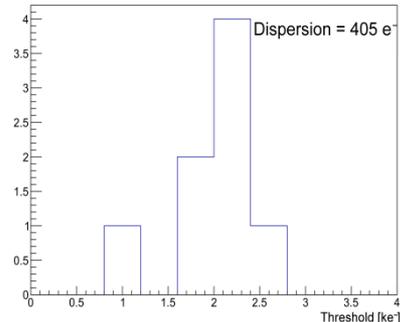
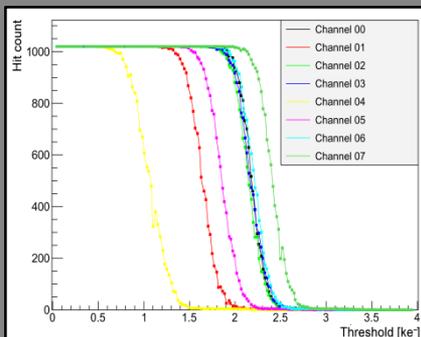


AFTER TUNING

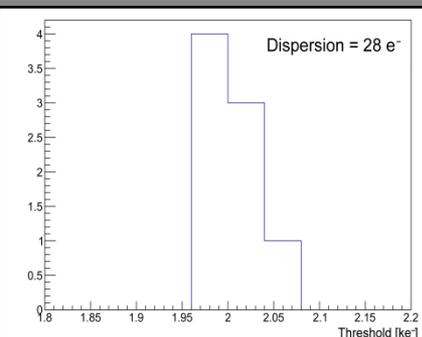
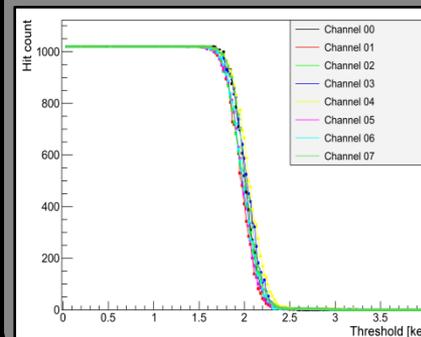


CONTINUOUS CSA AND DYNAMIC COMPARATOR

BEFORE TUNING



AFTER TUNING



FE-I4 vs FE-T65-1 (analog part)

	FE-I4	FE-T65-1
Technology	130 nm	65 nm
Pixel size	$250 \times 50 \mu\text{m}^2$	$180 \times 25 \mu\text{m}^2$
Dimensions of analog part	$156 \times 50 \mu\text{m}^2$	$59 \times 25 \mu\text{m}^2$
Charge sensitive amplifier	2 stages	1 stage
Comparator	continuous	continuous /dynamic
Analog power consumption	$12.6 + 5.4 + 3.9$ $= 21.9 \mu\text{W} / \text{pixel}$	$6.8 + 3.8 = 10.6 \mu\text{W} (18 \mu\text{W}) / \text{pixel}$
Analog power density	$1.75 \text{ mW} / \text{mm}^2$	$2.36 \text{ mW} / \text{mm}^2 (4 \text{ mW} / \text{mm}^2)$

... **$3.5 \text{ mW} / \text{mm}^2$ (including digital part)** specified the for future ATLAS pixel chip

65 nm – what we have learned:

- shrinking pixel size down to $125 \times 25 \mu\text{m}^2$ is possible
- dynamic comparator saves power but has larger threshold dispersion
- ENC is comparable with FE-I4
- power density has to be optimized

Summary

- Two test chips (FE-T65-0 and FE-T65-1) designed in 65 nm CMOS technology
- FE-T65-1 studied in terms of :
 - linearity, noise, time-walk, threshold dispersion and power density
- Analog performance is comparable with FE-I4 (130 nm technology)
- Larger prototype needs to be designed:
 - design which can be bonded to sensor
 - add full (synthesized) digital logic

=> tests with sensor, explore issues related to densely packed electronics



Thank you for your attention

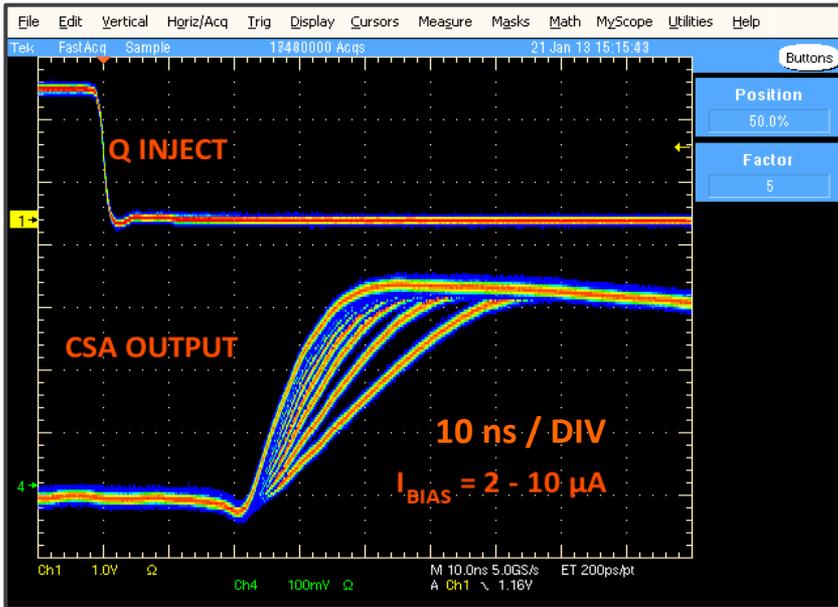


Backup slides

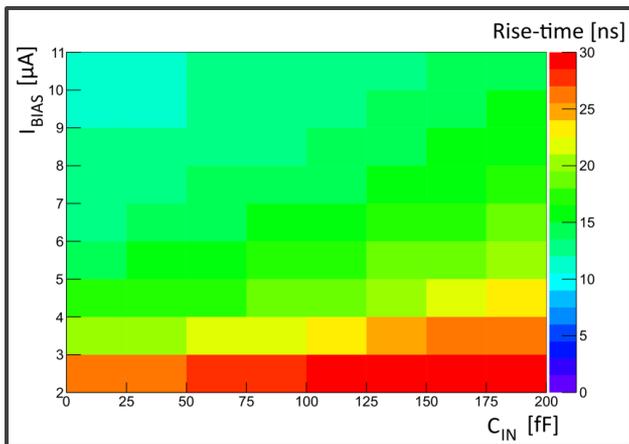
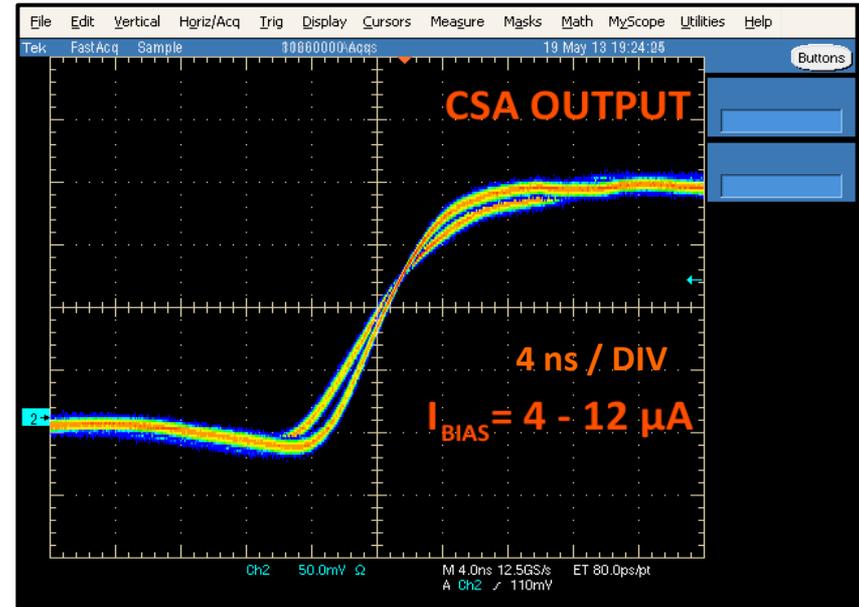
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Rise time measurement

CSA with continuous reset



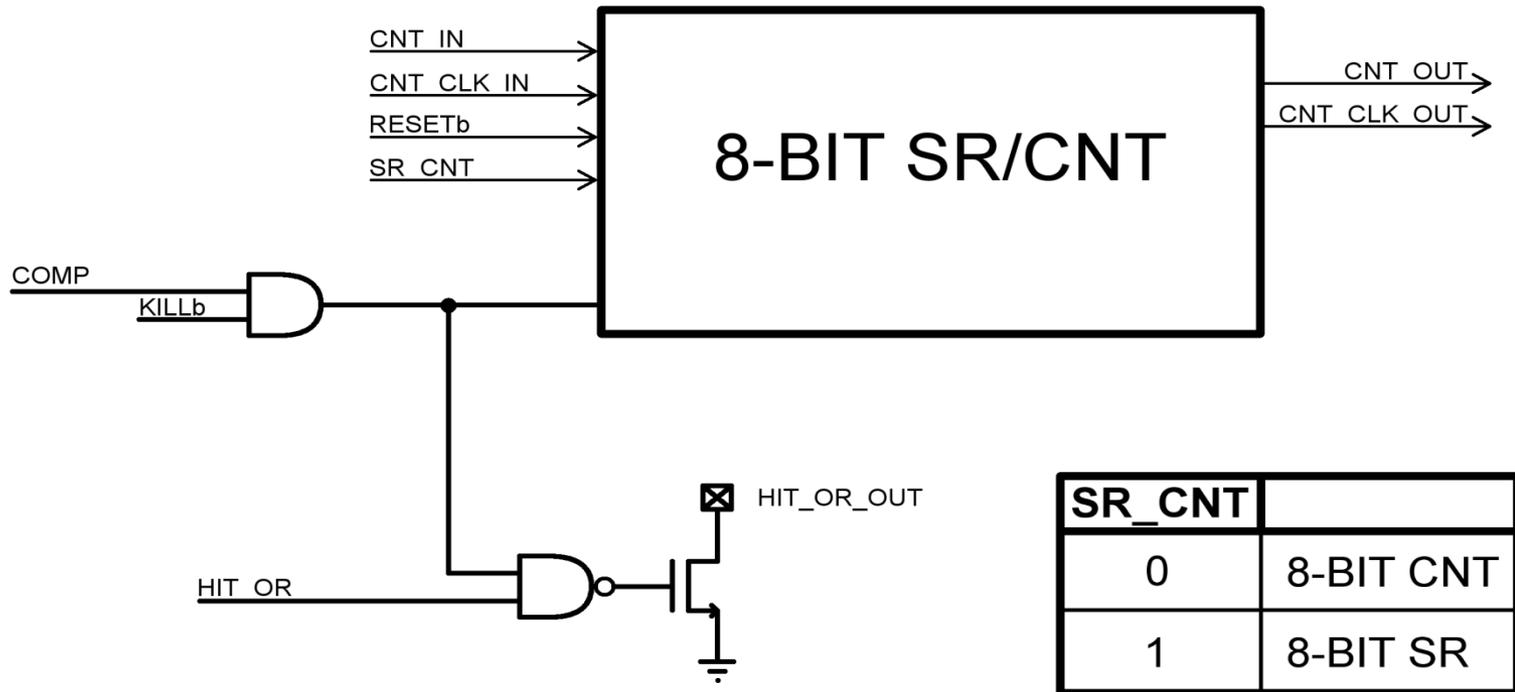
CSA with switched reset



- Rise-time depends on bias current of the CSA
- Power dependence is more significant for CSA with continuous reset

FE-T65-1 – digital part

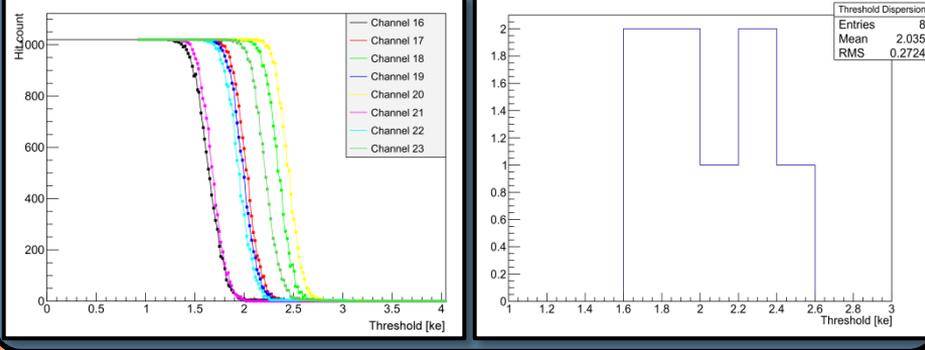
Configuration Register



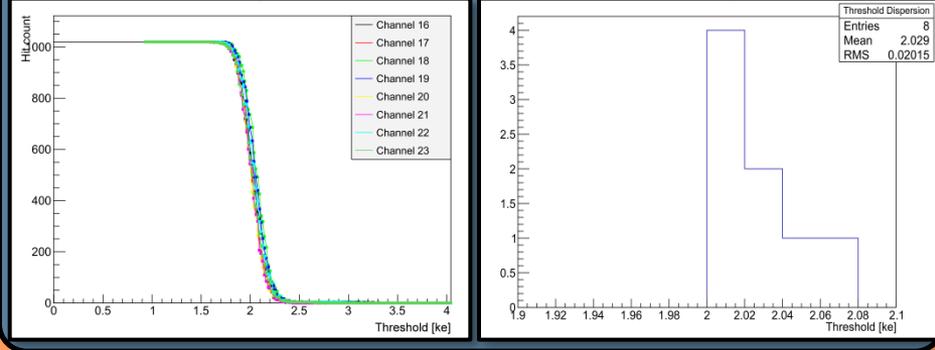
Threshold dispersion SWITCHED CSA

SWITCHED CSA & DYNAMIC COMPARATOR

BEFORE TUNING

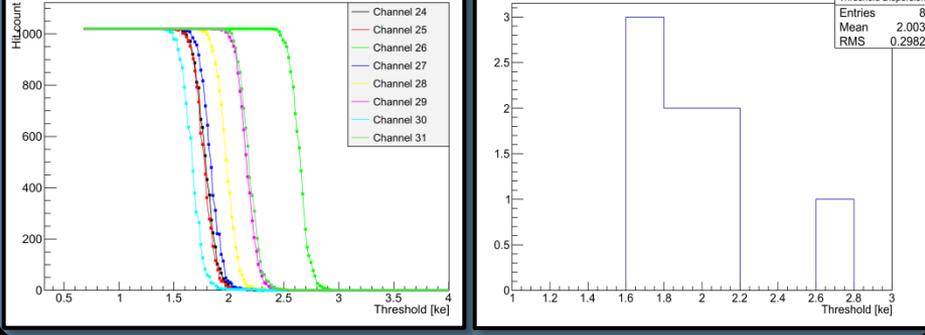


AFTER TUNING

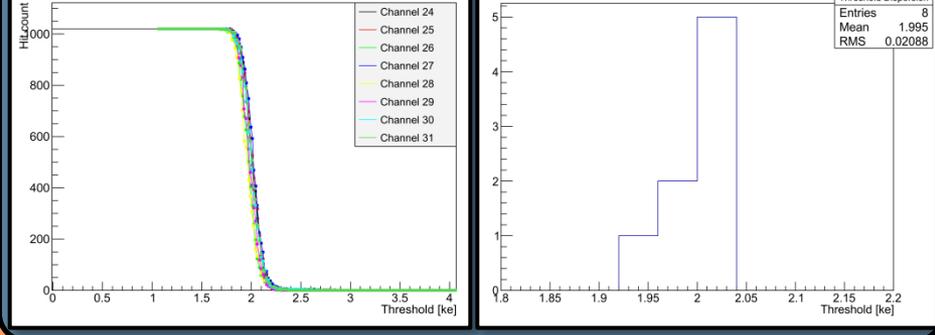


SWITCHED CSA & CONTINUOUS COMPARATOR

BEFORE TUNING

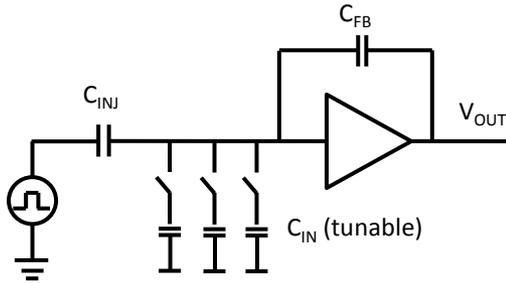
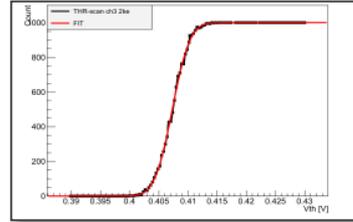


AFTER TUNING



ENC determination

$$\text{ENC} = \frac{\sigma(V_{OUT})}{\text{gain}_Q}$$



non-ideal amplifier

$$\text{gain}_Q = f(Q, C_{IN}, I_{BIAS}, I_{DIS} \dots)$$

- Finite bandwidth
- Finite gain
- Non-ideal current sources, short channel effects
- Ballistic deficit due to feedback discharge current

C_{INJ} and gain have to be measured or simulated

Ideal case

$$\text{gain}_V = \frac{\Delta V_{OUT}}{\Delta V_{IN}} = 1$$

$$\text{gain}_Q = \frac{\Delta V_{OUT}}{\Delta Q_{IN}} = \frac{1}{C}$$

Real life

$$\text{gain}_V = \frac{\Delta V_{OUT}}{\Delta V_{IN}} < 1$$

$$\text{gain}_Q = \frac{\Delta V_{OUT}}{\Delta Q_{IN}} < \frac{1}{C}$$

$$\text{gain}_Q = \frac{1}{\frac{C_{IN}}{a} + C_{FB} \left(1 - \frac{1}{a}\right)}$$

a ... open loop gain of the amplifier

a = 53 dB or 450

ENC as a function of I_{BIAS} and C_{IN}

- I_{BIAS} changes bias condition of input transistor

Higher I_{BIAS} means:

Amplifier is faster

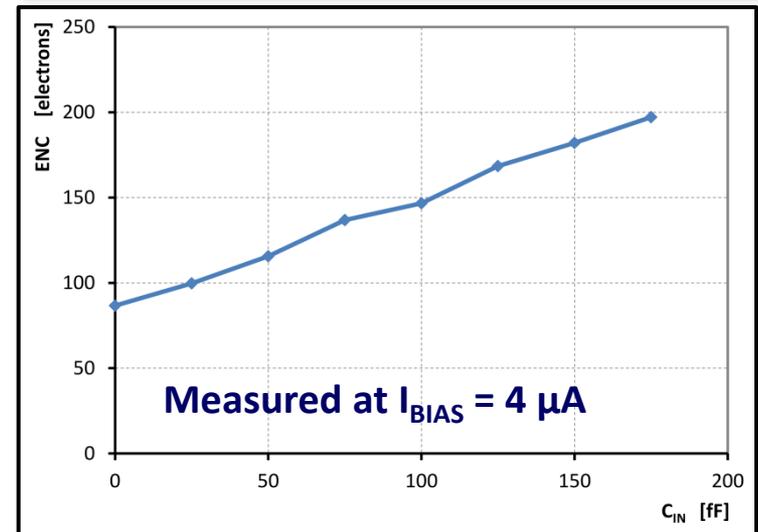
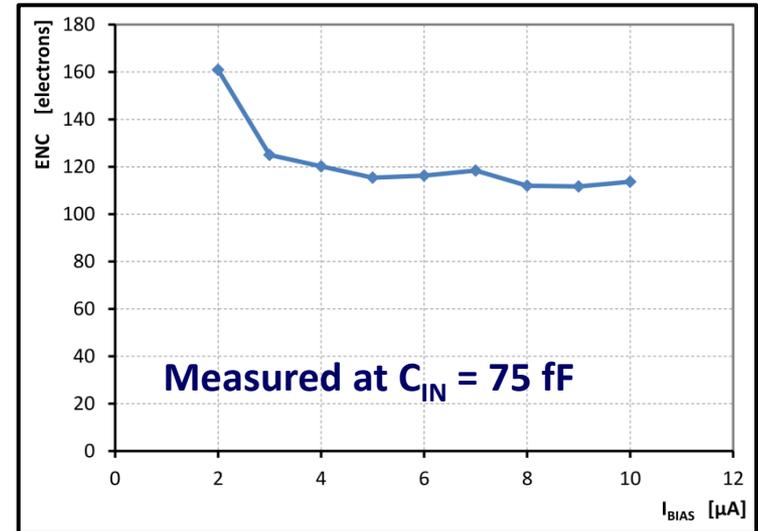
- smaller ballistic deficit
- higher gain
- smaller ENC

g_{m1} is higher

- thermal noise component smaller
- smaller ENC

- ENC scales with C_{IN}

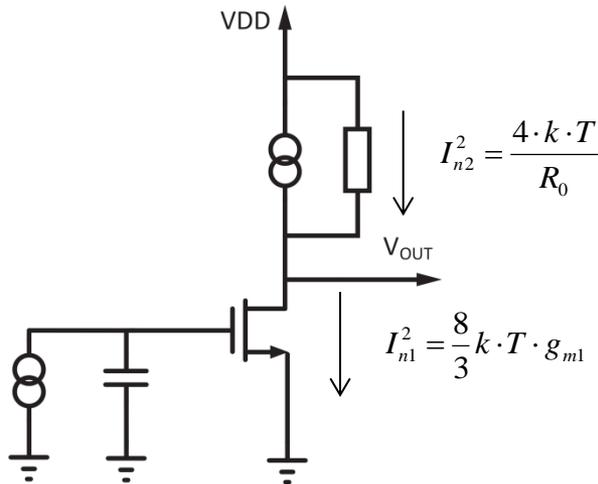
- thermal noise component scales linearly with C_{IN}
- gain of the CSA depends on C_{IN}



ENC scaling

- **ENC scaling – qualitative model:**

- most significant noise is thermal noise



$$I_{nTOTAL} = 4 \cdot k \cdot T \cdot \left(\frac{1}{R_0} + \frac{2}{3} \cdot g_{m1} \right)$$

Referring the noise source to the input:

$$ENC \approx \frac{C_D}{q} \sqrt{4 \cdot k \cdot T \left(\frac{2}{3 \cdot g_{m1}} + \frac{1}{R_0 \cdot g_{m1}^2} \right)}$$

- **ENC scales linearly with C_D**

- **ENC is inversely proportional to g_{m1}** $g_{m1} \approx \sqrt{I_{BIAS}}$

- **Other noise sources: flicker noise, shot noise**

..... more details are described in thesis of W. Tsung and M. Karagounis

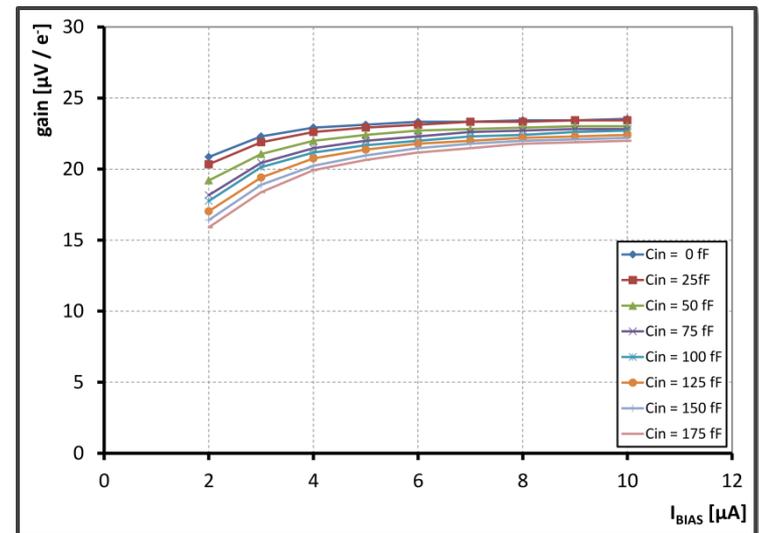
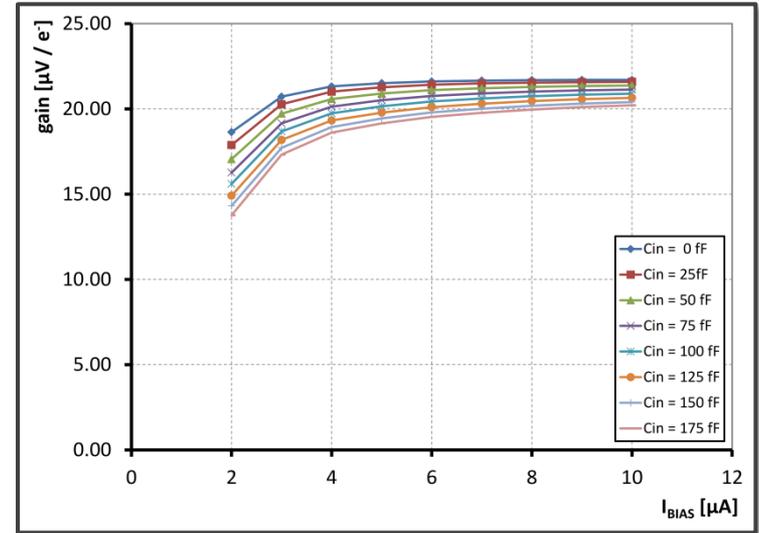
Amplifier gain determination

- 1.) using simulation data:

$$\text{gain} = f(I_{\text{BIAS}}, C_{\text{IN}}) @ Q_{\text{INJ}} = 5 \text{ ke}^-$$

- 2.) measure gain directly with FE-T65-1 chip

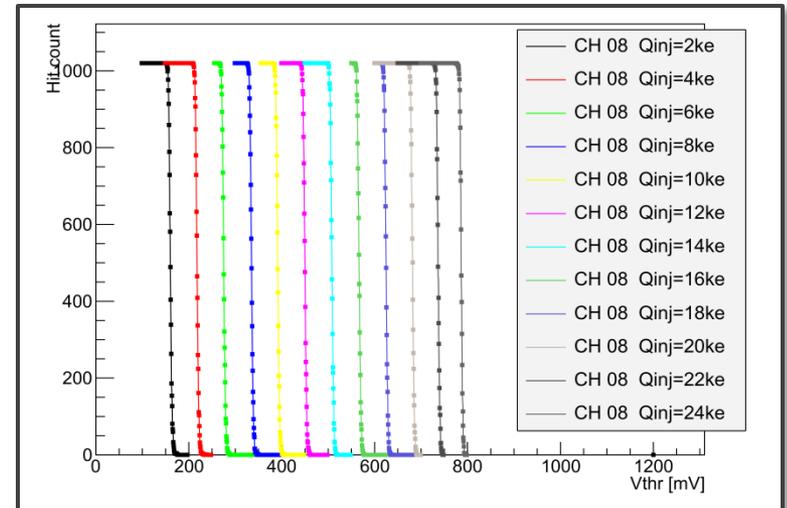
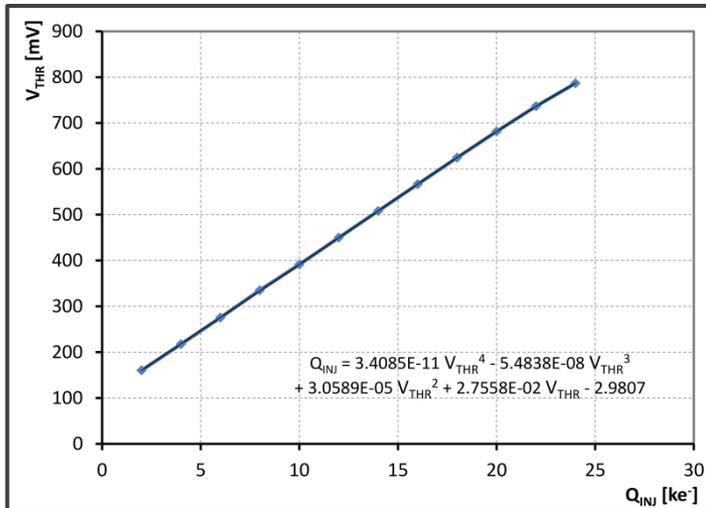
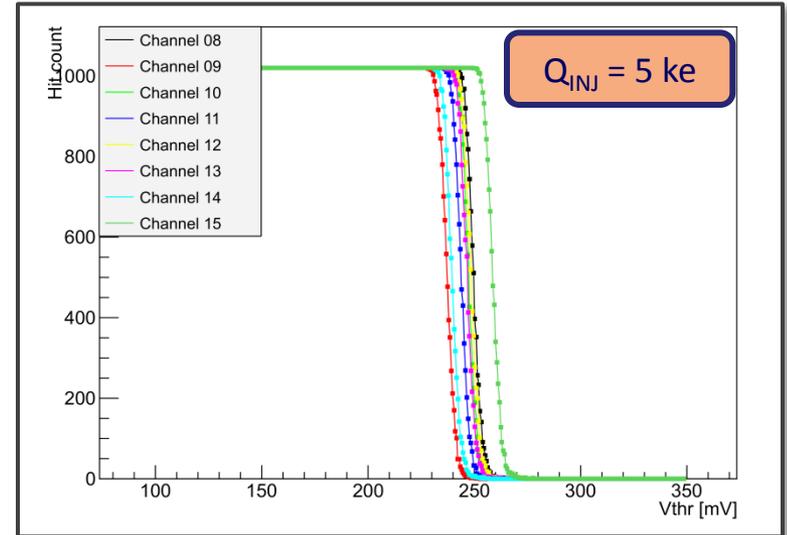
$$\text{gain} = f(I_{\text{BIAS}}, C_{\text{IN}}) @ Q_{\text{INJ}} = 5 \text{ ke}^-$$



Threshold dispersion

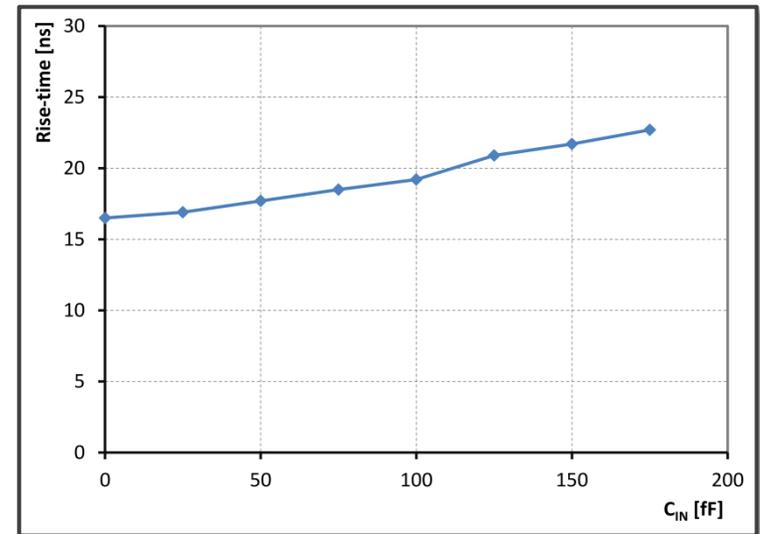
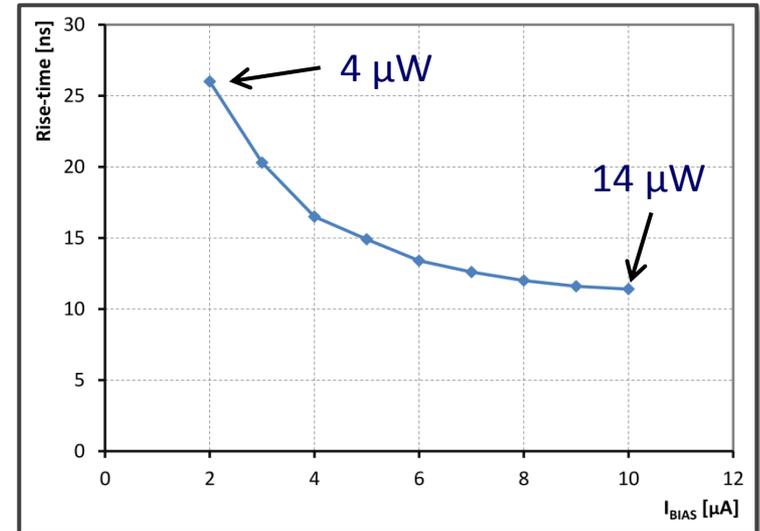
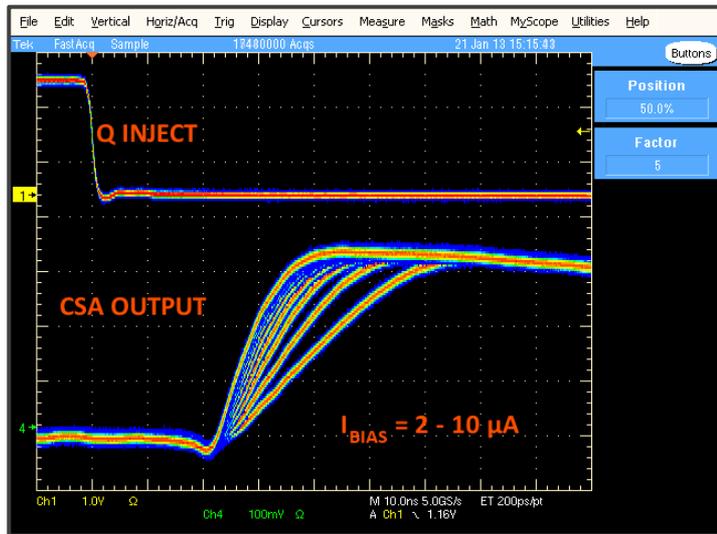
What is the threshold distribution ?

- 8 identical channels (cont. FB CSA + normal comp.)
- What is the threshold voltage for 5 ke input charge?
- > calibration has to be done !!

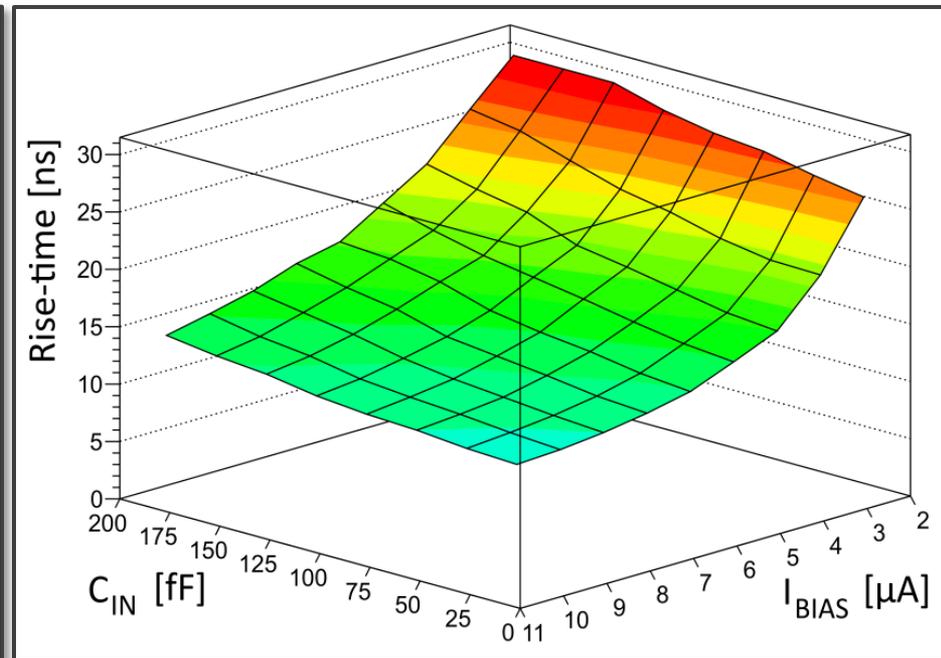
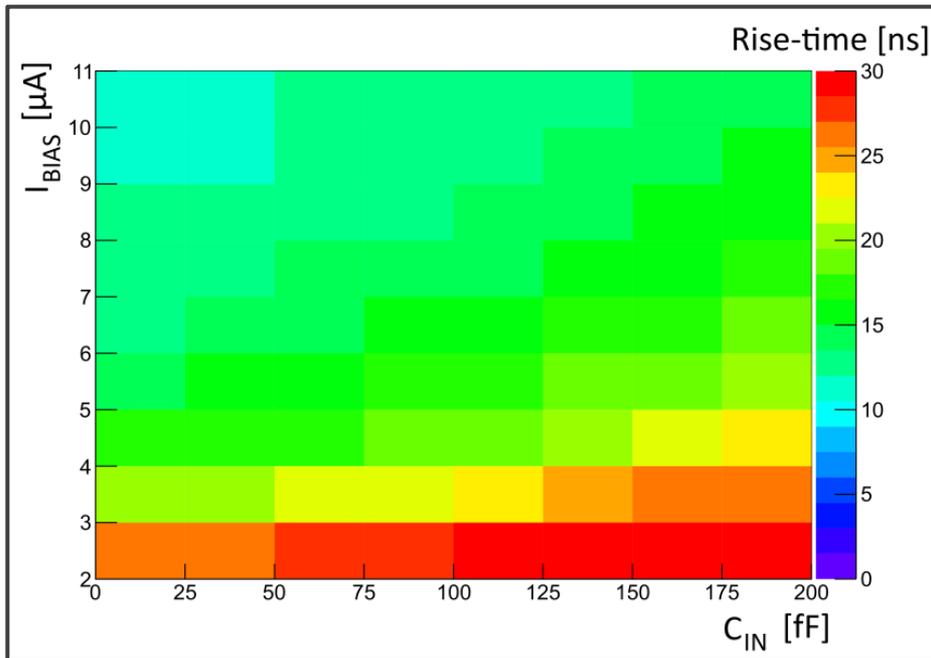


Rise-time function of I_{BIAS} and C_{IN}

- Rise-time depends on I_{BIAS} and C_{IN}
- **Higher I_{BIAS}** -> faster charging of parasitic capacitances
-> shorter rise-time
- **Higher C_{IN}** -> higher effective C_{DS} (Miller effect)
-> longer rise-time



Rise-time function of I_{BIAS} and C_{IN}

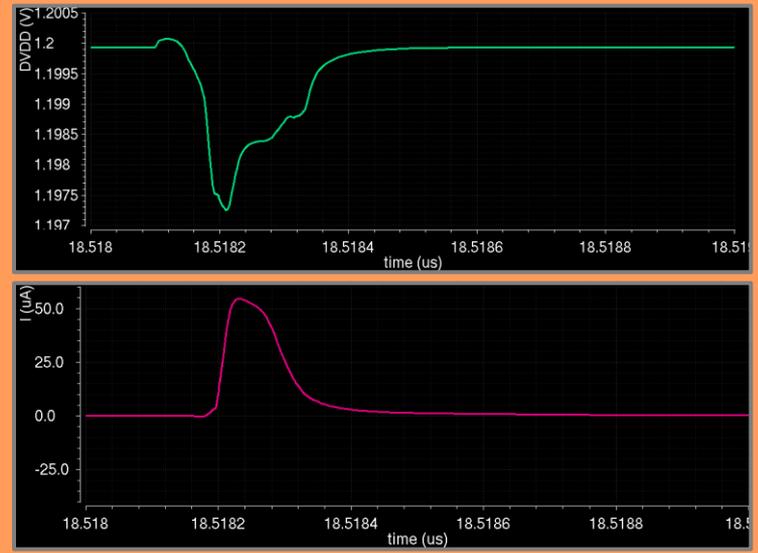


Excessive noise of dynamic comparator

Continuous comparator



Dynamic comparator



- Dynamic comparator produces spikes on the power lines and DNW
- Solution -> use decoupling MOSCAPS!!

