Pixel front-end development

in 65 nm CMOS technology

M. Havránek, T. Hemperek, T. Kishishita, H. Krüger and N. Wermes

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Outline

- Motivation for 65 nm
- Test chip FE-T65-1
- Measurements with FE-T65-1
- Summary
New pixel front-end chip needed

- HL-LHC in ~ 2022 → $10^{35}$ cm$^{-2}$ s$^{-1}$
- Higher luminosity, higher hit rate
- Higher radiation doses
- Most critical are the innermost pixel layers

Smaller pixel size

Hybrid detector
Monolithic detector . . .

3D integration (130 nm)
65 nm technology

ATLAS Pixel FE chips

<table>
<thead>
<tr>
<th>FE-13</th>
<th>FE-I4</th>
<th>FE-??</th>
</tr>
</thead>
<tbody>
<tr>
<td>250 nm technology</td>
<td>130 nm technology</td>
<td>65 nm technology</td>
</tr>
<tr>
<td>pixel size 400 × 50 µm$^2$</td>
<td>pixel size 250 × 50 µm$^2$</td>
<td>pixel size 125 × 25 µm$^2$</td>
</tr>
<tr>
<td>3.5 mil. transistors</td>
<td>80 mil. transistors</td>
<td>~ 500 mil. transistors</td>
</tr>
</tbody>
</table>

65 nm technology

The smallest transistor in HEP!!
### Specification for the new ATLAS pixel FE chip

- **Sensor thickness (planar or 3D):** 100 – 150 µm -> MIP signal ~ 10 ke⁻
- **Pixel size:** ~ 150* × 25 µm²
- **Threshold:** ~ 1 ke⁻
- **Threshold dispersion:** ~ 100 e⁻
- **Noise:** < 200 e⁻ @ C_{IN} * = 400 fF, I_{LEAK} * = 100 nA
- **Power dissipation:** 3.5 mW / mm²
- **Hit rate:** ~ 1GHz / cm² => ~ 30 kHz / pixel
- **Hit loss:** < 0.5 % (rather 0.1 %)
- **Radiation tolerance:** 1 Grad, 2×10¹⁶ neutrons
- **Technology:** 65 nm

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*M. Garcia-Sciveres,*

Future pixel chips design meeting 19ᵗʰ February 2013

*Parameters which are not yet clear*
65 nm prototypes designed in Bonn

- Our goal: explore potential of 65 nm technology
- Design of test-chips to study analog performance of 65 nm technology
- Analog FE-prototypes:
  - FE-T65-0, FE-T65-1
- Other prototypes: SAR-ADC, PLL, LVDS, synthesized logic for SEU tests

Chip size: 1.96×1.96 mm²
Array of 32 pixels of four different versions:

<table>
<thead>
<tr>
<th>Version</th>
<th>CSA</th>
<th>Comparator</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Continuous reset</td>
<td>Continuous</td>
</tr>
<tr>
<td>2</td>
<td>Continuous reset</td>
<td>Dynamic</td>
</tr>
<tr>
<td>3</td>
<td>Switched reset</td>
<td>Continuous</td>
</tr>
<tr>
<td>4</td>
<td>Switched reset</td>
<td>Dynamic</td>
</tr>
</tbody>
</table>

Test system

Wire-bonded FE-T65-1
FE-T65-1 – single pixel

- CSA tunable input capacitance
- programmable charge injection
- FDAC – tunable feedback current
- TDAC – tunable threshold
- comparator

- identical for every pixel
- configuration register 15-bits
- 8-bit shift register-counter
- mask-bit
- HitOr

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Charge sensitive amplifier with continuous reset

Version with continuous comparator

Version with dynamic comparator

Return to baseline ~ 240 ns

4ke – 20ke; step 4ke
Charge sensitive amplifier with switched reset

**Properties of switched CSA:**
- no ballistic deficit
- higher gain
- fast reset
- requires synchronous operation

**Version with continuous comparator**

**Version with dynamic comparator**

**POWER (CSA only) = 11 µW**

w.r. to 6.8 µW (cont. CSA)

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Continuous vs dynamic comparator

**Continuous comparator**
- Popular 2 stage architecture
- Asynchronous operation
- Consumes power even idle state

**Dynamic comparator**
- Based on latch in metastable state
- Does not consume power in idle state
- Active only when CLK edge comes
- Power proportional to CLK frequency
Time-walk measurement

- Time-walk: charge dependent propagation time
- The most significant delay is just around threshold
- If time-walk > 25 ns → wrong time-stamp

![Continuous CSA + continuous comparator](image)

- No delayed hits observed with dynamic comparator (low power consumption of 10.6 µW/pixel is preserved)
- No delayed hits observed with switched CSA
Noise – continuous CSA

Continuous CSA + continuous comparator

Continuous CSA + dynamic comparator
Noise – switched CSA, comparison of all versions

## Switched CSA + continuous comparator

<table>
<thead>
<tr>
<th>$I_{\text{IN}}$ [µA]</th>
<th>ENC [electrons]</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>20</td>
</tr>
<tr>
<td>8</td>
<td>40</td>
</tr>
<tr>
<td>10</td>
<td>60</td>
</tr>
<tr>
<td>12</td>
<td>80</td>
</tr>
<tr>
<td>14</td>
<td>100</td>
</tr>
<tr>
<td>16</td>
<td>120</td>
</tr>
<tr>
<td>18</td>
<td>140</td>
</tr>
<tr>
<td>20</td>
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## Switched CSA + dynamic comparator

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<td>160</td>
</tr>
</tbody>
</table>

### Table

<table>
<thead>
<tr>
<th>CSA Type</th>
<th>Comparator Type</th>
<th>$\langle \text{ENC} \rangle$ [e$^-$]</th>
<th>Power [µW]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Continuous</td>
<td>Continuous</td>
<td>144</td>
<td>10.4</td>
</tr>
<tr>
<td>Continuous</td>
<td>Dynamic</td>
<td>183</td>
<td>10.6</td>
</tr>
<tr>
<td>Switched</td>
<td>Continuous</td>
<td>113</td>
<td>14.6</td>
</tr>
<tr>
<td>Switched</td>
<td>Dynamic</td>
<td>157</td>
<td>14.8</td>
</tr>
</tbody>
</table>
Threshold dispersion

CONTINUOUS CSA AND CONTINUOUS COMPARATOR

BEFORE TUNING

CONTINUOUS CSA AND DYNAMIC COMPARATOR

BEFORE TUNING

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**FE-I4 vs FE-T65-1 (analog part)**

<table>
<thead>
<tr>
<th></th>
<th>FE-I4</th>
<th>FE-T65-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>130 nm</td>
<td>65 nm</td>
</tr>
<tr>
<td>Pixel size</td>
<td>$250 \times 50 , \mu m^2$</td>
<td>$180 \times 25 , \mu m^2$</td>
</tr>
<tr>
<td>Dimensions of analog part</td>
<td>$156 \times 50 , \mu m^2$</td>
<td>$59 \times 25 , \mu m^2$</td>
</tr>
<tr>
<td>Charge sensitive amplifier</td>
<td>2 stages</td>
<td>1 stage</td>
</tr>
<tr>
<td>Comparator</td>
<td>continuous</td>
<td>continuous /dynamic</td>
</tr>
<tr>
<td>Analog power consumption</td>
<td>$12.6 + 5.4 + 3.9 = 21.9 , \mu W / \text{pixel}$</td>
<td>$6.8 + 3.8 = 10.6 , \mu W (18 , \mu W) / \text{pixel}$</td>
</tr>
<tr>
<td>Analog power density</td>
<td>$1.75 , \text{mW} / \text{mm}^2$</td>
<td>$2.36 , \text{mW} / \text{mm}^2 (4 , \text{mW} / \text{mm}^2)$</td>
</tr>
</tbody>
</table>

...3.5 mW / mm² (including digital part) specified the
for future ATLAS pixel chip

**65 nm – what we have learned:**

- shrinking pixel size down to $125 \times 25 \, \mu m^2$ is possible
- dynamic comparator saves power but has larger threshold dispersion
- ENC is comparable with FE-I4
- power density has to be optimized
Summary

- Two test chips (FE-T65-0 and FE-T65-1) designed in 65 nm CMOS technology
- FE-T65-1 studied in terms of:
  - linearity, noise, time-walk, threshold dispersion and power density
- Analog performance is comparable with FE-I4 (130 nm technology)

- Larger prototype needs to be designed:
  - design which can be bonded to sensor
  - add full (synthesized) digital logic
  => tests with sensor, explore issues related to densely packed electronics
Thank you for your attention
Rise time measurement

CSA with continuous reset

- Rise-time depends on bias current of the CSA
- Power dependence is more significant for CSA with continuous reset
FE-T65-1 – digital part

Configuration Register

8-BIT SR/CNT

<table>
<thead>
<tr>
<th>SR_CNT</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>8-BIT CNT</td>
</tr>
<tr>
<td>1</td>
<td>8-BIT SR</td>
</tr>
</tbody>
</table>
Threshold dispersion SWITCHED CSA

SWITCHED CSA & DYNAMIC COMPARATOR

BEFORE TUNING

AFTER TUNING

SWITCHED CSA & CONTINUOUS COMPARATOR

BEFORE TUNING

AFTER TUNING
ENC determination

**Ideal case**

\[
\text{gain}_V = \frac{\Delta V_{OUT}}{\Delta V_{IN}} = 1
\]

\[
\text{gain}_Q = \frac{\Delta V_{OUT}}{\Delta Q_{IN}} = \frac{1}{C}
\]

**Real life**

\[
\text{gain}_V = \frac{\Delta V_{OUT}}{\Delta V_{IN}} < 1
\]

\[
\text{gain}_Q = \frac{\Delta V_{OUT}}{\Delta Q_{IN}} < \frac{1}{C}
\]

\[
\text{gain}_Q = \frac{1}{C_{\text{INJ}} + C_{\text{FB}} \left(1 - \frac{1}{a}\right)}
\]

- Finite bandwidth
- Finite gain
- Non-ideal current sources, short channel effects
- Ballistic deficit due to feedback discharge current

\(C_{\text{INJ}}\) and gain have to be measured or simulated

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ENC as a function of $I_{\text{BIAS}}$ and $C_{\text{IN}}$

- $I_{\text{BIAS}}$ changes bias condition of input transistor
  
  Higher $I_{\text{BIAS}}$ means:
  
  - Amplifier is faster
    - smaller ballistic deficit
    - higher gain
    - smaller ENC
  
  $g_{m1}$ is higher
  
  - thermal noise component smaller
  
  - smaller ENC

- ENC scales with $C_{\text{IN}}$
  
  - thermal noise component scales linearly with $C_{\text{IN}}$
  
  - gain of the CSA depends on $C_{\text{IN}}$

---

**Continuous CSA**

**Cont. comparator**

**Measured at $C_{\text{IN}} = 75 \text{ fF}$**

**Measured at $I_{\text{BIAS}} = 4 \mu\text{A}$**
ENC scaling

- ENC scaling – qualitative model:
  - most significant noise is thermal noise

\[ I_{nTOTAL} = 4 \cdot k \cdot T \left( \frac{1}{R_0} + \frac{2}{3} \cdot g_{m1} \right) \]

Referring the noise source to the input:

\[ \text{ENC} \approx \frac{C_D}{q} \sqrt{4 \cdot k \cdot T \left( \frac{2}{3} \cdot g_{m1} + \frac{1}{R_0 \cdot g_{m1}^2} \right)} \]

- ENC scales linearly with \( C_D \)
- ENC is inversely proportional to \( g_{m1} \)
  \[ g_{m1} \approx \sqrt{I_{BIAS}} \]

- Other noise sources: flicker noise, shot noise
  ..... more details are described in thesis of W. Tsung and M. Karagounis
Amplifier gain determination

- 1.) using simulation data:
  \[
  \text{gain} = f(I_{\text{BIAS}}, C_{\text{IN}}) \quad @ \quad Q_{\text{INJ}} = 5 \text{ ke}^{-}
  \]

- 2.) measure gain directly with FE-T65-1 chip
  \[
  \text{gain} = f(I_{\text{BIAS}}, C_{\text{IN}}) \quad @ \quad Q_{\text{INJ}} = 5 \text{ ke}^{-}
  \]
Threshold dispersion

- 8 identical channels (cont. FB CSA + normal comp.)
- What is the threshold voltage for 5 ke input charge?
  - \( Q_{\text{INJ}} = 5 \text{ ke} \)

\[
Q_{\text{INJ}} = 3.4085\times10^{-11} V_{\text{INJ}}^2 - 5.4838\times10^{-8} V_{\text{INJ}}^3 + 3.0588\times10^{-5} V_{\text{THR}}^2 + 2.7558\times10^{-2} V_{\text{THR}} - 2.9807
\]
Rise-time function of $I_{BIAS}$ and $C_{IN}$

- Rise-time depends on $I_{BIAS}$ and $C_{IN}$

- Higher $I_{BIAS}$ -> faster charging of parasitic capacitances
  -> shorter rise-time

- Higher $C_{IN}$ -> higher effective $C_{DS}$ (Miller effect)
  -> longer rise-time

Continuous CSA

![Graph showing rise-time vs. $I_{BIAS}$ and $C_{IN}$](image)
Rise-time function of $I_{\text{BIAS}}$ and $C_{\text{IN}}$
Excessive noise of dynamic comparator

- Dynamic comparator produces spikes on the power lines and DNW
- Solution -> use decoupling MOSCAPS!!