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Pixel front-end development in 65 nm CMOS technology

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Upgrade of luminosity of the LHC (HL-LHC) imposes severe constraints on detector tracking systems in terms of radiation hardness and ability to cope with high hit rates. One possible way of keeping track with increasing luminosity is usage of more advanced technologies. Ultra deep sub-micron CMOS technology allows design of complex and high speed electronics with high integration density. In addition these technologies are inherently radiation hard. We present a prototype of analog pixel front-end designed in 65 nm CMOS technology with applications oriented to upgrade of the ATLAS Pixel Detector. Aspects of ultra deep sub-micron design and performance of the analog pixel front-end circuits will be presented.

Summary

We present a prototype of a pixel analog front-end FE-T65-1 designed in 65 nm CMOS technology. The development of this integrated circuit has been motivated by a need of a new read out chip to operate ATLAS pixel detector after high luminosity LHC upgrade.
The test chip contains an array of 32 pixels with pixel size of 180×25 μm2. Four flavors of the pixel electronics have been implemented. The pixels differ by architecture of charge sensitive amplifier (constant current reset or switched reset) and comparator (continuous and dynamic comparator). Analog part of every pixel is equipped with tunable input capacitance allowing determination of noise as a function of input capacitance. Digital part is identical for every pixel and contains configuration register and hit counter.
Performance of each version of FE-T65-1 has been evaluated in terms of noise, time-walk and threshold dispersion.
Noise performance of the pixel front-end depends on the input capacitance of the charge sensitive amplifier (CSA) and also on the version of the analog circuitry. CSA with switched reset exhibits systematically lower noise (ENC = 113 e-) with respect to CSA with constant current feedback (ENC = 144 e-). This effect is attributed to the absence of ballistic deficit of the switched CSA and therefore this CSA has higher gain and lower noise. An excessive noise contribution has been found in the pixel versions with the dynamic comparator possibly due to additional switching activity in the pixel (ENC = 183 e- resp. 157 e-).
The dynamic performance of the front-end electronics greatly depends on power budget. Peaking time of the CSA as well as the comparator contributes to the time-walk. Time difference between large hit (20 ke-) and small hit (2 ke-) with threshold of 2ke- has been studied. In order to avoid delay exceeding 25 ns (one bunch crossing at the LHC) power consumption of the pixel with constant current CSA and with continuous comparator must be increased up to 18 μW per pixel. The dynamic comparator (clocked at frequency of 40 MHz) has a very small intrinsic time-walk with respect to the CSA and therefore overall power consumption to meet 25 ns criteria is 10 μW per pixel. The versions with switched CSA meet 25 ns criteria with power consumption of 15 μW.
Another important property of many pixel front-end chip is threshold dispersion. Every pixel in the test matrix have slightly different threshold. The mean value of the threshold dispersion is about 400 electrons. In order to compensate this effect, every pixel contains 5-bit DAC allowing threshold adjustment locally in every pixel. Applying threshold tuning procedure the threshold dispersion has been reduced well below 30 electrons for every pixel version.
To summarize the results achieved with FE-T65-1 the overall analog performance of this prototype is least comparable with the existing ATLAS pixel front-end chip FE-I4 designed in 130 nm technology.

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