A 20 mW, 4.8 Gbit/sec, SEU robust serializer in 65nm for read-out of data from LHC experiments

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TWEPP
Perugia 24-09-2013
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OUTLINE

- GigaBit Transceiver (GBT)
- Low Power GBT serializer specifications
- How to reduce power consumption
  - TMR Serializer
  - Code-Protected Serializer
- Test chip
  - Characterization
- Conclusions
THE GIGABIT TRANSCEIVER (GBT)

- Developed at CERN in the past years
- It provides the support to transmit bidirectionally the information required to run a HL-LHC experiment
- It has to run in an hostile radiation environment due to the higher Luminosity ($L \leq 10^{35} \text{ cm}^{-2}\text{s}^{-1}$) reachable in the LHC upgrade
- Radiation dose of several Mrad in certain point of the detector
- 18K links in the CMS (pixel + inner) tracker
- The high data rates produced in the experiments demand high bandwidth with a small power consumption and low error rates.
  - For this reason a Low Power version of the GBT is under development
- The work presented here is focusing on the design of the Serializer block of this Low Power GBT
SERIALIZER BLOCK SPECIFICATIONS

- Same transmission protocol of GBT130 Serializer
- 65nm technology
- Radiation robustness (Total Ionizing Dose = 100Mrad/10 years, Single Event Upset = 1 wrong word/day)
- Power consumption per serializer ≤ 30mW (25% of GBT130 SER power consumption)
- \( V_{dd} = 1.2 \, V \pm 10\% \) (1.5 V in GBT130)
GBT TRANSMISSION PROTOCOL

- Bitrate 4.8 Gb/s
- 120 bits for each word
- 4 bits header
- Each word is divided in 4 bit symbols
- Reed-Solomon code, it can correct up to 4 wrong symbols per word
HOW TO REDUCE POWER CONSUMPTION?

- More advanced technology and lower Vdd, but it is not enough
- Change architecture:
  - Reduce the number of clock signals
  - In the GBT130 transistors in FFs have very large channel widths in order to increase SEU robustness (in addition to other techniques). Reduce the size of the transistor
- Two solutions have been investigated:
  - TMR serializer
  - Code Protected serializer

Current GBT130 serializer block scheme
TMR SERIALIZER

- SEU robustness through triplication, TID robustness through proper transistors sizing
- Full custom design
- TSPC FFs
- Optimized counters

Load Generator 0
Ck @ 4.8 GHz
Reset

Load Generator 1
Ck @ 4.8 GHz
Reset

Load Generator 2
Ck @ 4.8 GHz
Reset

SR 0 120 bit
Load
Data input
Ck @ 4.8 GHz
Reset

SR 1 120 bit
Load
Data input
Ck @ 4.8 GHz
Reset

SR 2 120 bit
Load
Data input
Ck @ 4.8 GHz
Reset

Voted Restart

From pattern generator

120

Voter

Output

Reset

Reset

Reset

Reset

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A load pulse every 120 clock cycles (25 ns)

Regular counter logic is too slow:

- A 7 bit Linear Feedback Shift Register used as pseudorandom counter
  - Reset to initial value after 25 ns
- TSPC Flip Flops, CMOS Combinational Logic Gates
✓ Low Vth mosfets
✓ $t_{\text{Ck-}q} = 45$ ps
✓ $t_{\text{setup}} = -35$ ps
## GBT 130 FFs vs LpGBT FFs

In the shift registers

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<th>GBT 130</th>
<th>LpGBT</th>
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<td>L (each MOS)</td>
<td>120 nm</td>
<td>60 nm</td>
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<td>Total W</td>
<td>170 µm</td>
<td>6.6 µm</td>
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- 3 voted Load Generators => A SEU on the voter can flip more bits than the code can correct
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- A single shift register => data protects data
- 3 voted Load Generators => A SEU on the voter can flip more bits than the code can correct

The idea is to split the load signal in enough branches so that each SEU potentially generated can always be corrected by the Reed-Solomon code.
SEU robustness through triplication for Load signal generation, Reed–Solomon code for data. TID robustness through proper transistors sizing

- Full custom design
- TSPC FFs
- Optimized counters
12 BIT BLOCKS

The Reed-Solomon code can correct up to 4 wrong symbols.

@ Loading each blocks of 12 bits contains 3 symbols
The Reed-Solomon code can correct up to 4 wrong symbols.

@ Loading each blocks of 12 bits contains 3 symbols ...

... but while shifting it can contain 2 entire symbols and 2 partial symbols.

With this partition the code is used by protecting not only data from transmission errors but also the control logic.

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From post parasitic extraction simulations:
- Power consumption TMR SER = 30 mW
- Area = 7900 µm²
- Power consumption CP SER = 18.9 mW
- Area = 3900 µm²
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In the testchip:

- Two serializers to test
- External 4.8 GHz Clock signal
- Internally generated test pattern
- New data word loaded every 25 ns (40 MHz)
- A PC controls the FPGA (Spartan-3) to set up the configuration bits of the chip
- The Bit Error Rate Tester (BERT) generates the clock signal and analyses the output of the serializers comparing it with the expected output
## PERFORMANCE TEST RESULTS

### Table: Bit Rate vs. Vdd

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<th>“TMR SER” max bit rate</th>
<th>“Code protected SER” max bit rate</th>
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<tr>
<td>1 V</td>
<td>4.0 Gb/s</td>
<td>4.0 Gb/s</td>
</tr>
<tr>
<td>1.1 V</td>
<td>5.0 Gb/s</td>
<td>5.0 Gb/s</td>
</tr>
<tr>
<td>1.2 V</td>
<td>5.6 Gb/s</td>
<td>5.6 Gb/s</td>
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<td>6.0 Gb/s</td>
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</tr>
<tr>
<td>1.5 V</td>
<td>6.25 Gb/s</td>
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### Graph: Bit Rate vs. Vdd

Requirements

- Bit rate: 4.8 Gbit/s
- Vdd: 1.2 V ± 10%

### Notes:

It is possible that the maximum bit rate at Vdd = 1.5 V was higher than 6.25 Gb/s but this value is the maximum reachable with this testbench.

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The measured power consumptions for the two serializers are:

Vdd= 1.2 V, Clock frequency= 4.8 GHz

- TMR SER : P=30 mW
- Code protected SER: P=19 mW

These measures match the estimations based on the post RC extraction simulations.
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Vdd = 1.2 V, Clock frequency = 4.8 GHz
- TMR SER: $P = 30 \text{ mW}$
- Code protected SER: $P = 19 \text{ mW}$
These measures match the estimations based on the post RC extraction simulations.
A PC controls the FPGA (Spartan-3) to set up the configuration bits of the chip.
The GLIB V2 (based on a Virtex-6) can implement the same function of the JBERT but reads 4 different chip output at the same time while they are continuously irradiated.
4 Chips working simultaneously to collect data quickly.
A test has been performed at the Heavy Ion Facility in Louvain-La-Neuve.

An additional test has to be performed, in fact:

- A bug in the Virtex-6 Verilog/VHDL code limited the data acquisition (for each chip the GLIB can only count the number of wrong words or save the error bit configuration of the last wrong word found before the read out of the data from the PC).
- An unexpected behaviour appeared during the test. **Not recoverable words have been found even for the TMR SER and this words shown always ~60 wrong bits spread all over the their length.**

However some considerations on the results can be made.
SEU threshold of the TMR SER is located between the LET 10.2 and 20.4 MeV/mg/cm$^2$, on the other hand the threshold for the CP SER is located in values of LET < 1.1 MeV/mg/cm$^2$

GBT protocol code recoverable words rate:
TMR SER 50% (1 correctable word/2 wrong words), CP SER 81.2% (39 recoverable words/48 total wrong words). More tests are planned to understand the cause of these unexpected behaviour and the Error Rate could change

The estimated error rate in the LHC experiments environment near the interaction point:
- A TMR SER should experience 6.6E-04 errors/day and considering the FEC 3.3E-04 errors/day. (1.65 E-03 errors/day in HL-LHC)
- A CP SER should experience 1.8 errors/day and considering the FEC 0.34 errors/day. (1.7 errors/day in HL-LHC)
CONCLUSIONS

- The two serializers work satisfying the low power and bitrate requirements.
- Analysing the results the TMR SER satisfy the SEU robustness specifications and consumes ~37% more power than the Code Protected SER.
- The CP SER error rate is slightly over the requirements (1 wrong word/day).
  - If the future SEU test will show the cause of the not recoverable words and how to improve the SEU robustness of the Code-Protected SER it can be implemented in the Low Power GBT reducing the power to 1/5 of the current serializer.
- In the CP SER an unusual way to use coding to protect the correct behaviour of the control logic in addition to the data integrity is introduced.
- The Total Ionizing Dose test is being prepared.

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THANK YOU!
BACK UP SLIDES
Core NMOS, threshold voltage shift

Core PMOS, threshold voltage shift

Core NMOS, leakage current

VOTED PATH

Counter → FF → FF → Voted FF → FF → Load

- Out
- FF: Reset, Ck
- FF: Reset, Ck
- Voted FF: In0, In1, In2, Ck
- FF: Reset, Ck

To Voted FFs

Restart (reset) Ck

From other 2 counters

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