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Characterization results and first applications of KLauS - an ASIC for SiPM charge and fast discrimination readout

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KLauS is an ASIC produced in the AMS 350nm SiGe process to read out the charge signals from silicon photomultipliers.
Developed as an analog frontend for future calorimeters with high granularity as pursued by the AHCAL concept in the CALICE collaboration,
the ASIC is designed to measure the charge signal of the sensors in a large dynamic range and with a high precision.
In order to compensate bias and temperature fluctuations of each sensor individually, an 8-bit DAC to tune the
voltage at the input terminal within a range of 2V is implemented.
Using an integrated fast comparator with low jitter, the time information can be measured with sub-nanosecond resolution.
The low power consumption of the ASIC can be further decreased using power gating techniques.
Future versions of KLauS are under development and will incorporate an ADC with a resolution of up to 12 bit and blocks for digital data transmission.

Most recent characterization results for the KLauS chip are presented as well as results from a KLauS-based test setup developed for mass
characterisation of scintillator tiles used in the AHCAL test beam program.

Summary

KLauS is an analog ASIC for current mode charge read out of silicon photomultipliers.
The 12 channel test chip aims at providing a readout system of scintillating tiles with silicon photomultipliers, integrated within a calorimetry system for a future linear collider experiment.
The AHCAL concept developed within the CALICE collaboration plans to build such a system, which is using scintillating tiles, silicon photomultipliers and integrated electronics in a sandwich calorimeter.
One of the main constraints in such a system is the very low allowable power consumption of the electronics.
The special feedback scheme of the KLauS input stage offers a low power consumption, which can be decreased using power gating techniques.
Using this technique the total power consumption is decreased to 25uW per channel for the nominal ILC bunch crossing scheme.
The topology of the input stage is a current conveyor specialized for the ASICs powergating capabilities, allowing a very low input impedance for the channels,
thus most of the signal charge can be collected by the later integration stage.
This yields a high signal to noise ratio even for low gain silicon photomultipliers.

The input stage topology allows the voltage at the input terminal to be adjusted to compensate for variations in the operating voltage of the silicon photomultipliers due to sensor production or temperature fluctuations.
Each of the 12 channels of the ASIC includes an 8-bit DAC to tune the input terminal voltage within 2V at an INL smaller than 2%,
with a resolution of approximately 10mV per LSB. The terminal voltage in power pulsing mode varies less than 20mV
when comparing the ‘on’ and ‘off’ state of the chip, keeping the sensors in a stable condition at all times.

The measured current is integrated in the later integration stage and then converted
to a pulse height signal using an active shaper with adjustable time constant and no undershoot.
This makes precise charge measurements possible, even for dark count rates in the order of several MHz as commonly seen in 3x3mm² Silicon Photomultipliers.
A discrete gain switching unit allows a dynamic range of more than 200pC for large area SiPMs.
The equivalent noise charge generated by the electronics was determined to be 25000 e- at an input capacitance of 40pF,
allowing a precise estimation of the sensor gain using single photon spectra. For a Hamamatsu S11028-025 MPPC, the signal to noise ratio was measured to be larger than 8 for a single pixel signal, dominated by the MPPC intrinsic signal fluctuations as SiPM excess noise and dark count pileup contributions. The ASIC contributes about 12.5% to the total noise.
In order to develop a full readout system in a mixed mode ASIC, an ADC with a pipelined capacitor switching structure is being developed.
For normal physics mode operation, a resolution of 8 bits seems sufficient due to the large landau fluctuations in the expected signals.
For measurements of the time information and calibration of the SiPM gain a higher resolution will be used (10 bits and 12 bits, respectively).
Together with a peak sensing unit, the ADC will be capable of measuring events with a rate of 1-3 MHz. This leads to a minimum of analog memory cells
prior to the conversion stages. The submission of a mini-asic to test the ADC is planned for the end of 2013.

The CALICE collaboration is running an extensive test beam program, for which scintillator tiles have to be characterized and validated for functionality. The properties of KLauS, especially the high signal to noise ratio and the pileup compensating shaper, make the ASIC very suited to test the characteristics of the scintillating tiles. A prototype setup using the KLauS ASIC has been set up, allowing semi-automated characterisation of 12 tiles in parallel. A fully automated system is being commissioned.

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