# Monolithic Active Pixel Sensor Development for the Upgrade of the ALICE Inner Tracker System

CERN/INFN/WUHAN ALICE ITS team

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ALICE Inner Tracking System at present
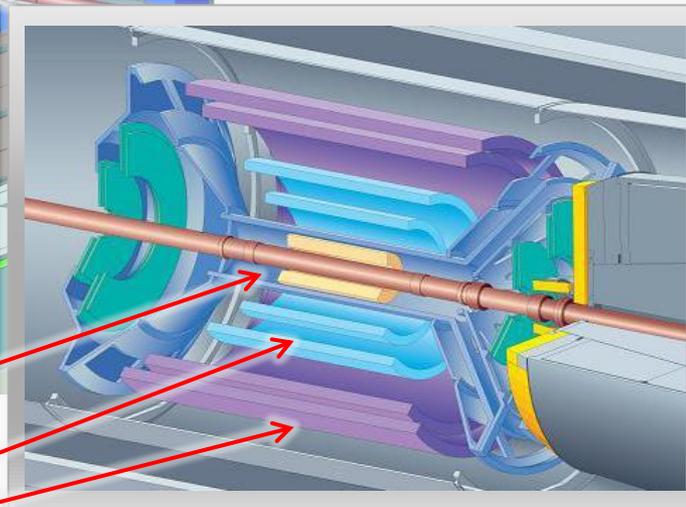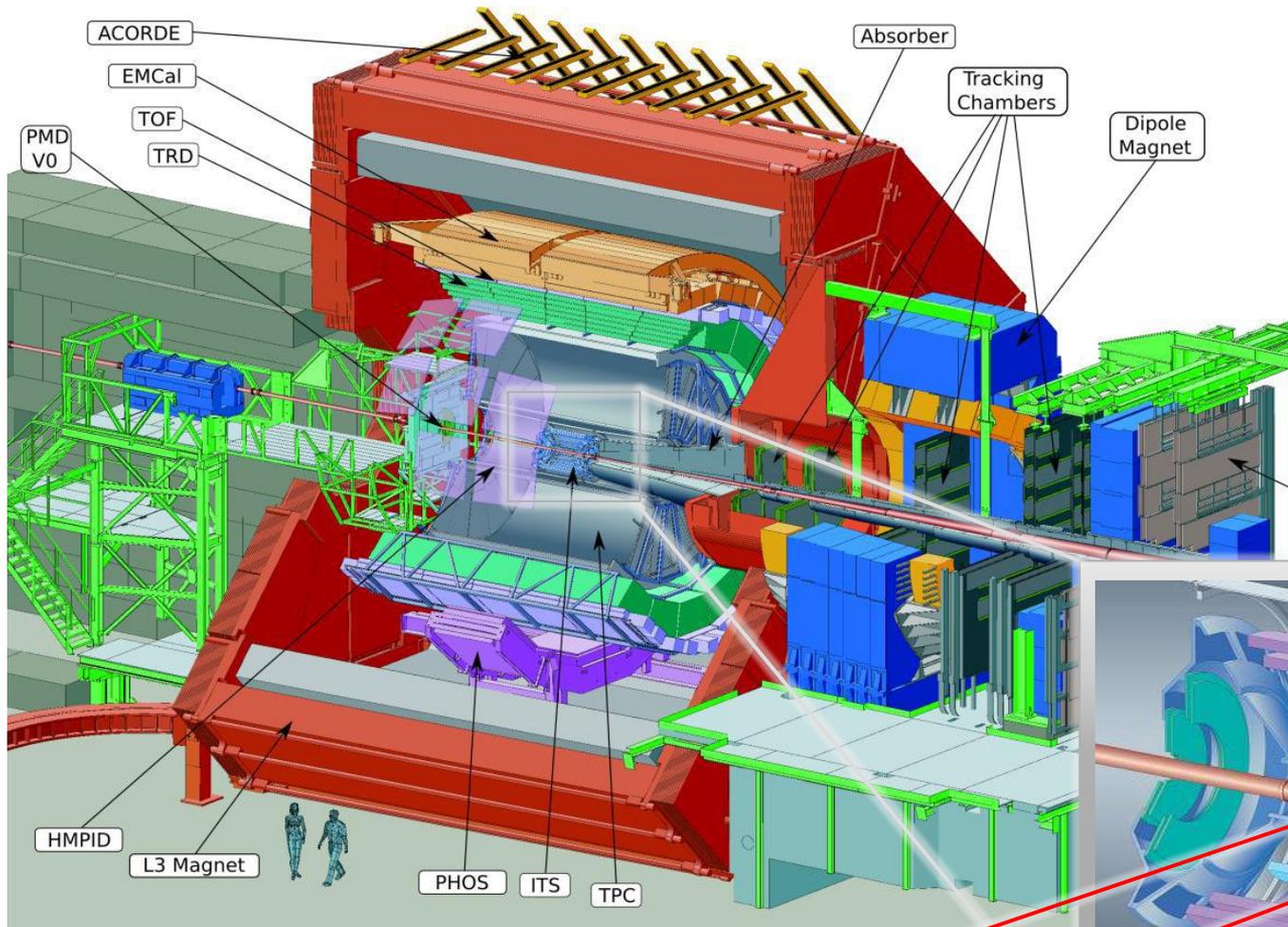
2 layers of hybrid pixels (SPD)
2 layers of silicon drift detector (SDD)
2 layers of silicon strips (SSD)

ITS upgrade

Objectives

- record collisions:
    - Pb-Pb at 50 kHz
    - pp at 1MHz

- improve impact parameter resolution by a factor 3

- improve standalone tracking efficiency and pT resolution

- fast insertion/removal for yearly maintenance

- installation 2017-2018
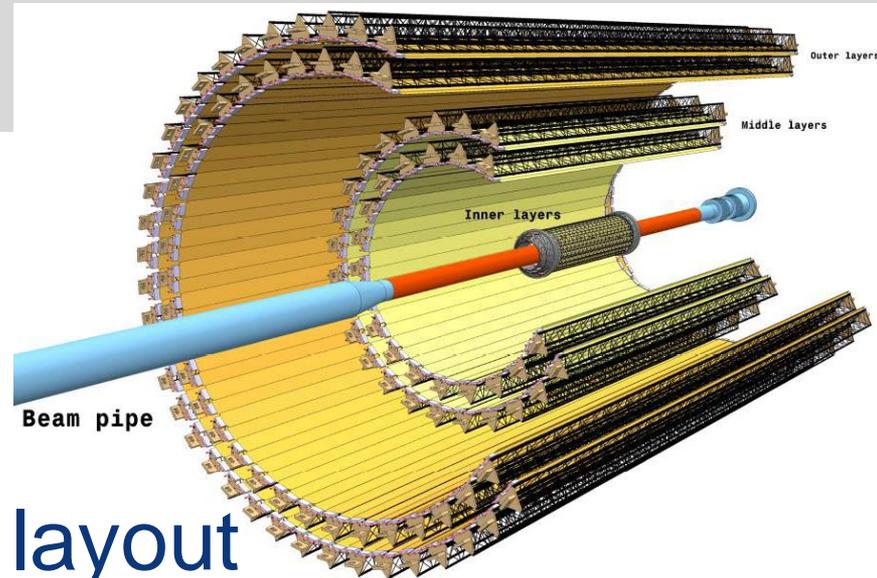
New layout

- 7 layers (3 inner, 4 middle+outer)

- reduce:

    - X/X0 per layer from 1.14 to 0.3 %

    - pixel size from 400x50 to O(30x30) μm²

    - first layer radius from 39 to 22 mm

- beam pipe outer radius: 19.8 mm

"**Upgrade of the Inner Tracking System Conceptual Design Report**"
http://cds.cern.ch/record/1475244

SPECIFICATIONS

	Inner Barrel	Outer Barrel
Silicon thickness	50 µm	
Material thickness	0.3% X_0	0.8% X_0
Chip Size	15 mm x 30 mm	
Pixel Size	$O(30 \times 30)\ \mu m^2$	$O(30 \times 30) \div O(50 \times 50)\ \mu m^2$
Integration Time	< 30 µs	
Power density	< 300 mW / cm^2	
Hit density (Pb-Pb)	~ 115 / cm^2	~ 1.5 / cm^2
Radiation Load (TID)	< 700 krad	< 10 krad
1 MeV n_{eq} fluency	1.1×10^{13} cm^{-2}	3×10^{10} cm^{-2}
Data throughputs	~1 Gbit sec^{-1} chip^{-1}	16 Mbit sec^{-1} chip^{-1}

UPPER LIMIT
lower much better !

- Nr of bits to code a hit : 35
- Fake hit : 10^{-5} /event

- Lowering integration time would significantly reduce background

- Lowering power would significantly reduce material budget

Starting point : ULTIMATE CHIP in STAR

- Developed by IPHC Strasbourg

- 0.35 µm OPTO process

- Rolling shutter and correlated double sampling

- 20.7x20.7 µm^2 pixel size

- Power consumption 130 mW/cm^2

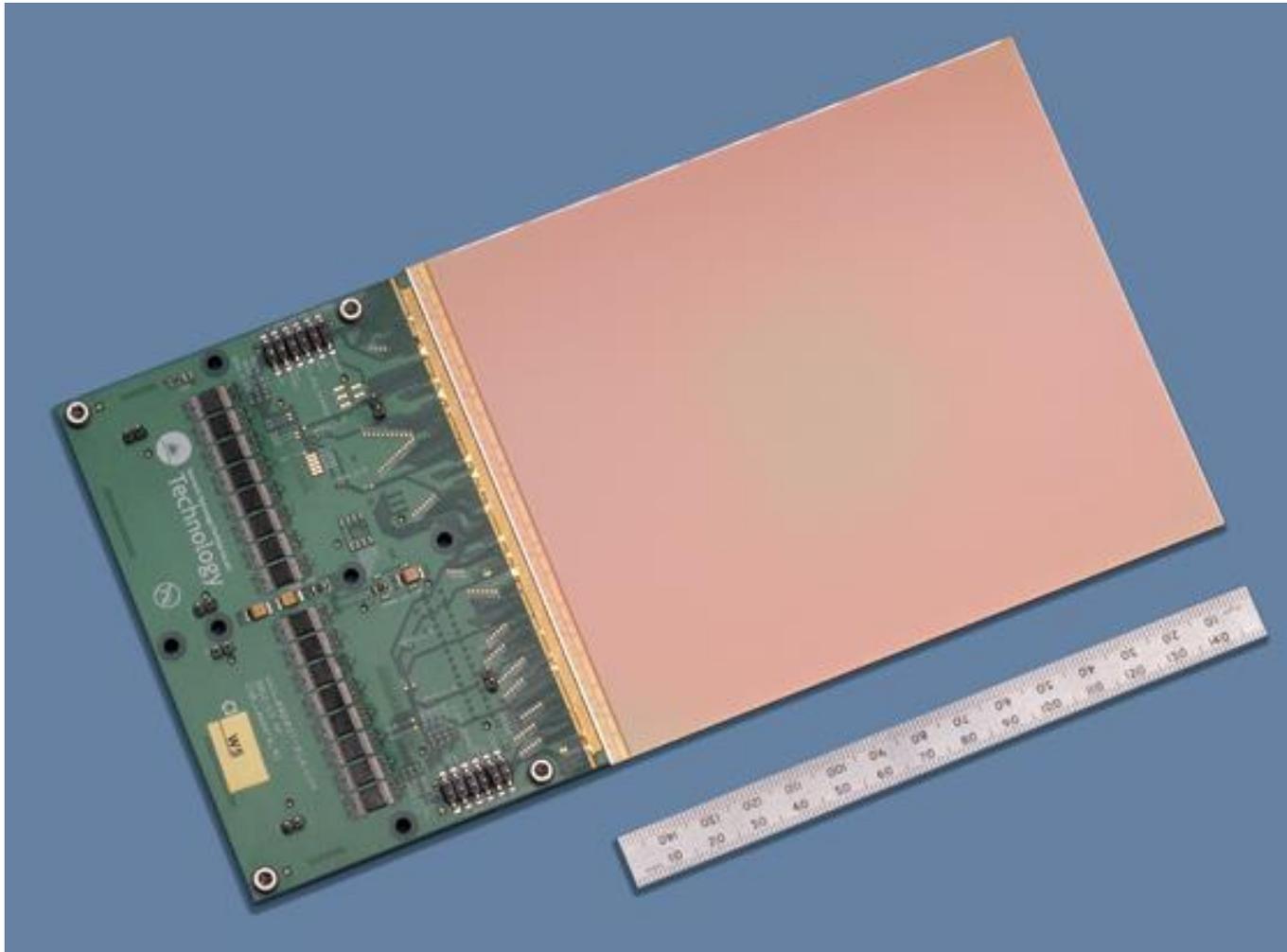Deeper submicron technology + development to meet ALICE specifications

22.71 mm

20.24 mm
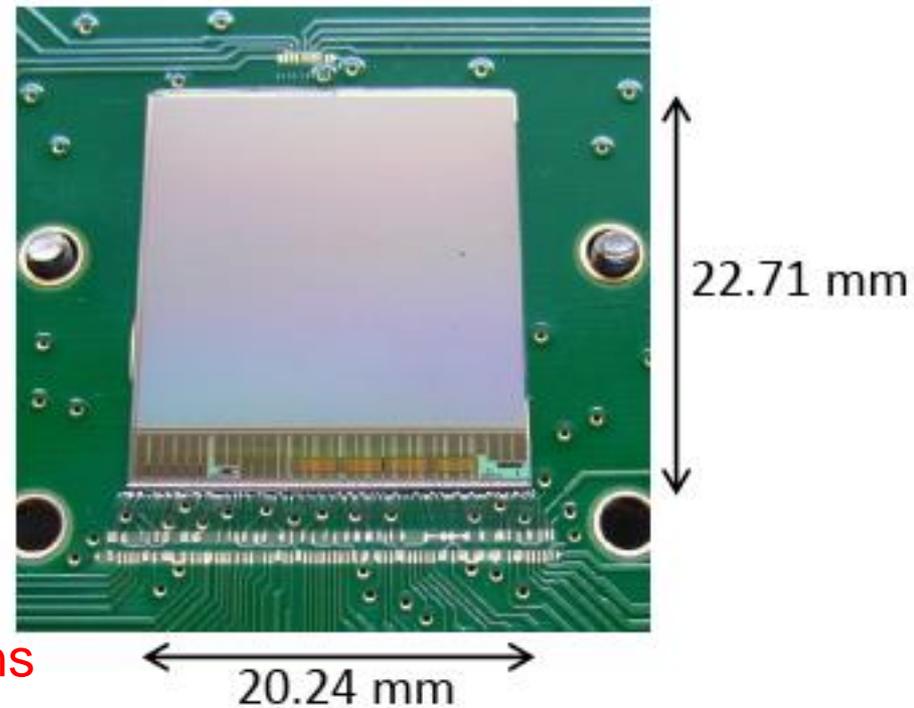
	STAR PXL	ALICE ITS (inner layers)
Readout time	190 µs	< 30 µs
TID radiation hardness	150 krad (35 °C)	700 krad (28 °C)
NIEL radiation hardness	few 10^{12} 1 MeV n_{eq} /cm^2 (35 °C)	1.1×10^{13} 1 MeV n_{eq} /cm^2

Monolithic detector in TowerJazz 180 nm CMOS

- Gate oxide < 4 nm => better transistor radiation tolerance
- 6 metal layers
- Epitaxial layer between 1 and 5 kΩcm, 15-18 µm
- Deep Pwell shields Nwell with PMOS transistors from the epitaxial layer and allows full CMOS within the pixel without efficiency loss
- Difficult to deplete epitaxial layer under Pwell far from Nwell collection electrode, but radiation tolerance sufficient (see below)
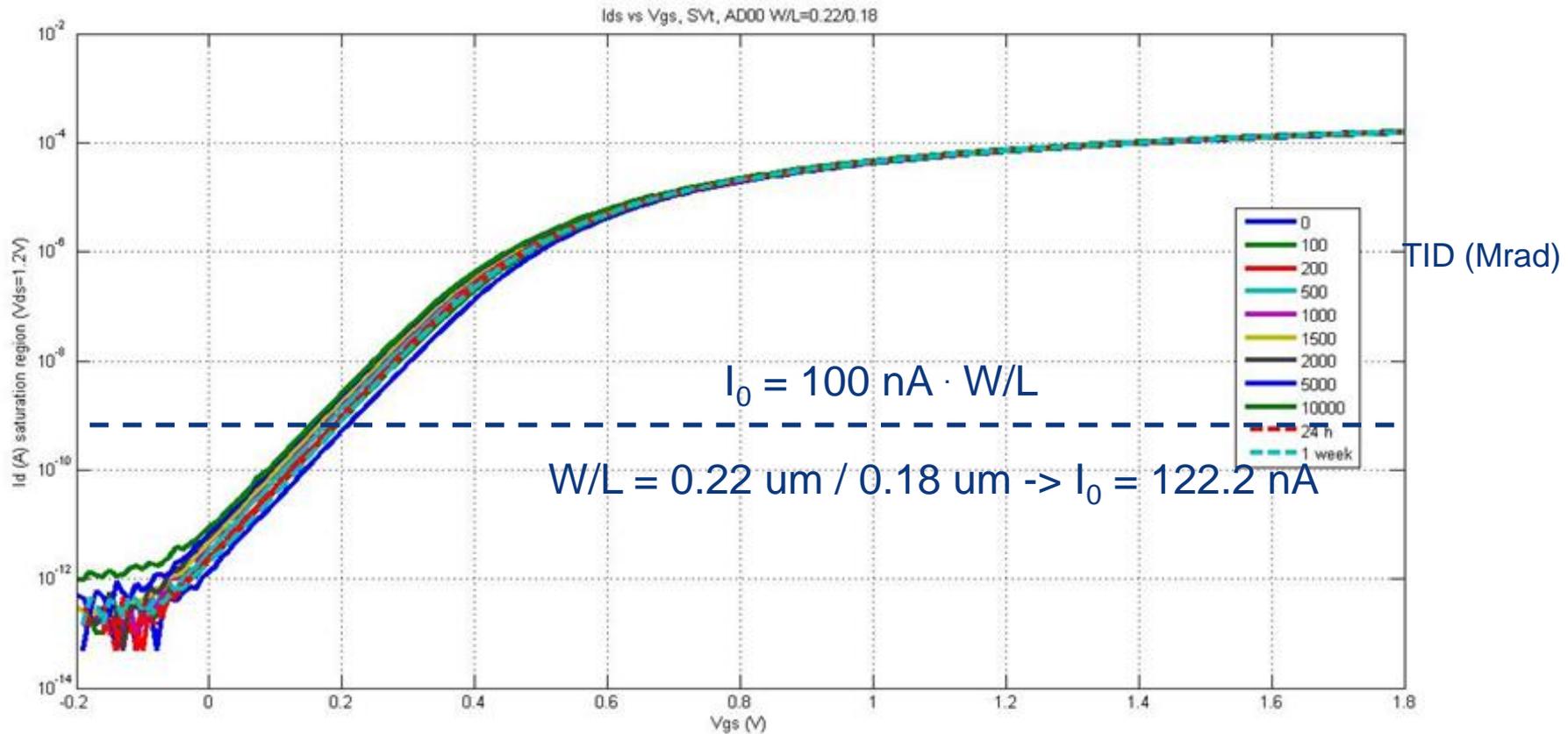- Stitching possible up to 200mm wafer scale

Courtesy: N. Guerrini, Rutherford Appleton Laboratory
V^th School on detectors and electronics for high energy physics, astrophysics, and
space and medical physics applications, Legnaro, April 2013

Radiation tolerance example: low voltage NMOS transistor

Ids vs Vgs, SVt, AD00 W/L=0.22/0.18

TID (Mrad)

Legend:
- 0
- 100
- 200
- 500
- 1000
- 1500
- 2000
- 5000
- 10000
- 24 h
- 1 week

$I_0 = 100 \text{ nA} \cdot \text{W/L}$

W/L = 0.22 um / 0.18 um -> I_0 = 122.2 nA

- Curves do not change significantly with irradiation
- Extensive testing campaign on transistors now complete and radiation tolerance in excess of ALICE needs

Developments and plan

3 Developments:

- MISTRAL & ASTRAL by IPHC Strasbourg

    Rolling shutter with discriminator at the end of the column or in the pixel

    See presentation earlier this afternoon

- CHERWELL by RAL

    Rolling shutter with strixel architecture: "end of column" circuitry integrated in pixels

- ALPIDE by CERN, INFN, CCNU(China)

   Low power front-end (20.5nA/pixel) with data-driven readout, integration time of a few µs determined by shaping time of the front end

2013 : optimize pixel structure and study different options for the readout architecture to obtain medium/large scale demonstrator

2014 : decide & finalize full scale to be ready for volume production

- CERN/INFN/WUHAN: several matrices and test structures, LVDS driver

- RAL: three matrices

- IPHC: many matrices, also significant work on zero suppression circuitry.
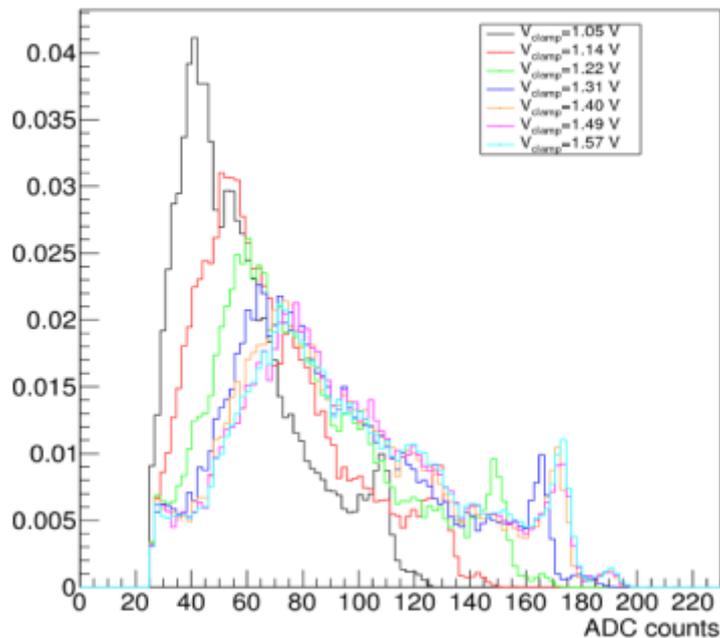
- 23.5x31 mm² total

- Several starting material

Type	epi thickness [μm]	resistivity [Ω cm]
1	12	30
2	18	> 1k
3	30	> 1k
4	40	> 1k
5	20	6.2 k
6	40	7.5 k
7	CZ	> 700

10
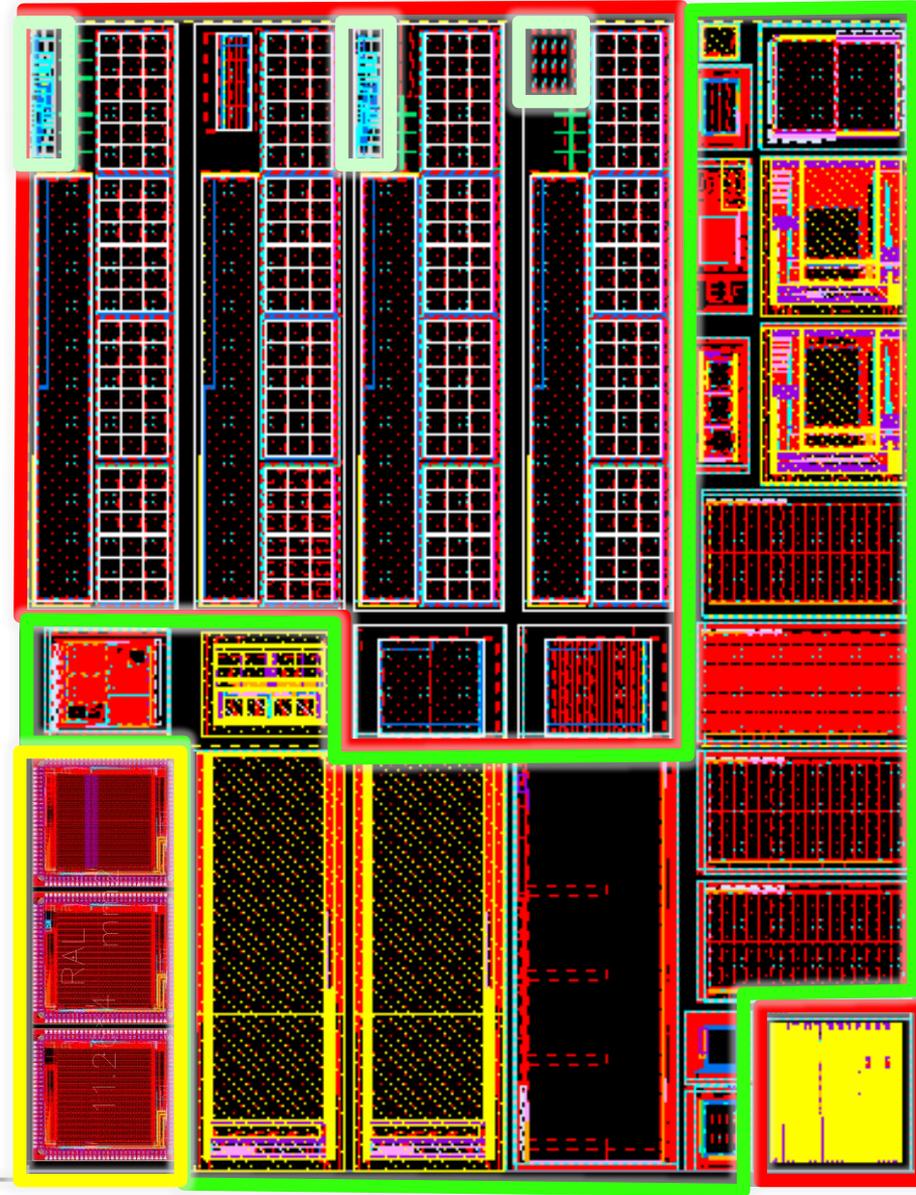
EXPLORER :
PIXEL SENSOR OPTIMIZATION and MEASUREMENTS

Starting point MIMOSA32 chips: Variation of V_{diode}

Maximum Signal

- V_{diode} up to 1.3 V:
  Shift of the spectrum towards higher ADC values

- V_{diode} larger than 1.4 V:
 No big differences observed

Cluster Signal

~1V

~1.6V
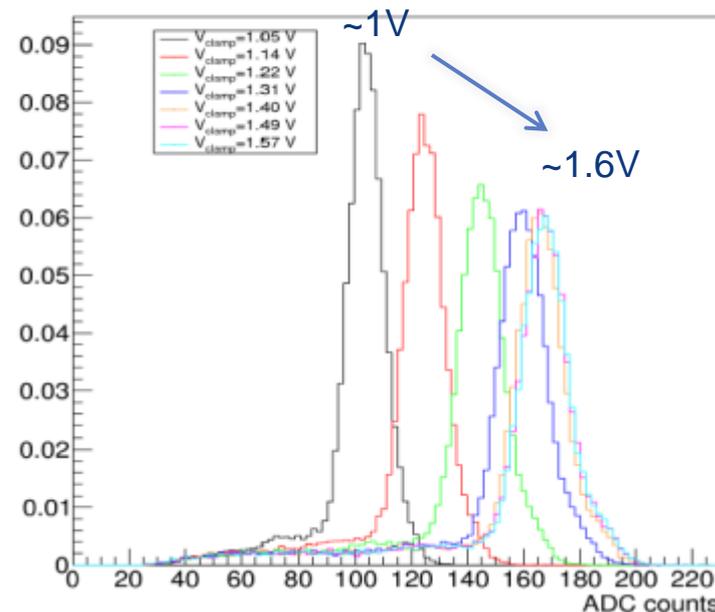
Example:
- Chip: 9B
- Structure: P00

Prototype July 2012 submission: Explorer-0

- Analog readout for pixel characterization
- Readout time decoupled from integration time
- Possibility to reverse bias the substrate
- Sequential readout with correlated double sampling
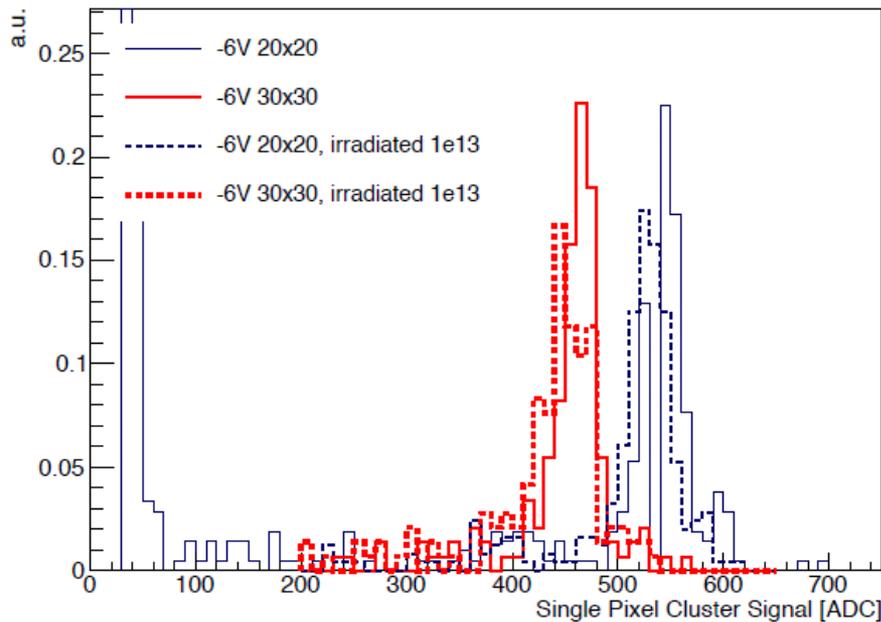- Contains two $1.8 \times 1.8 \, mm^2$ matrices of 20x20 and 30x30 micron pixels with different geometries
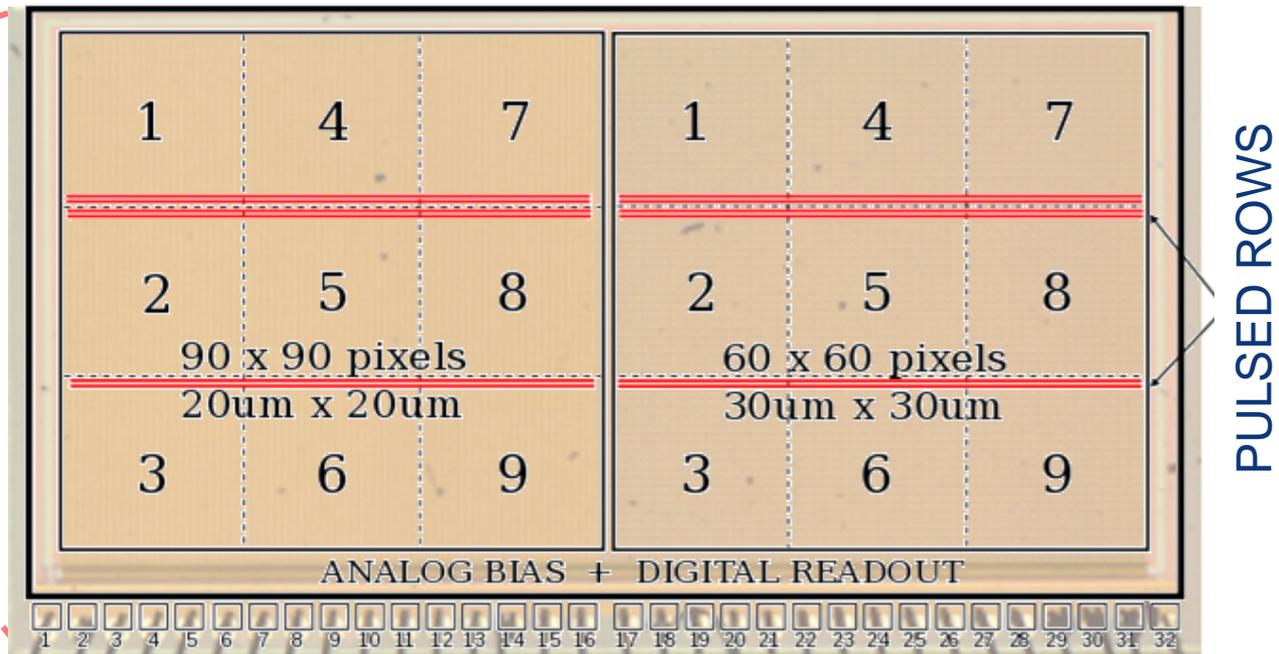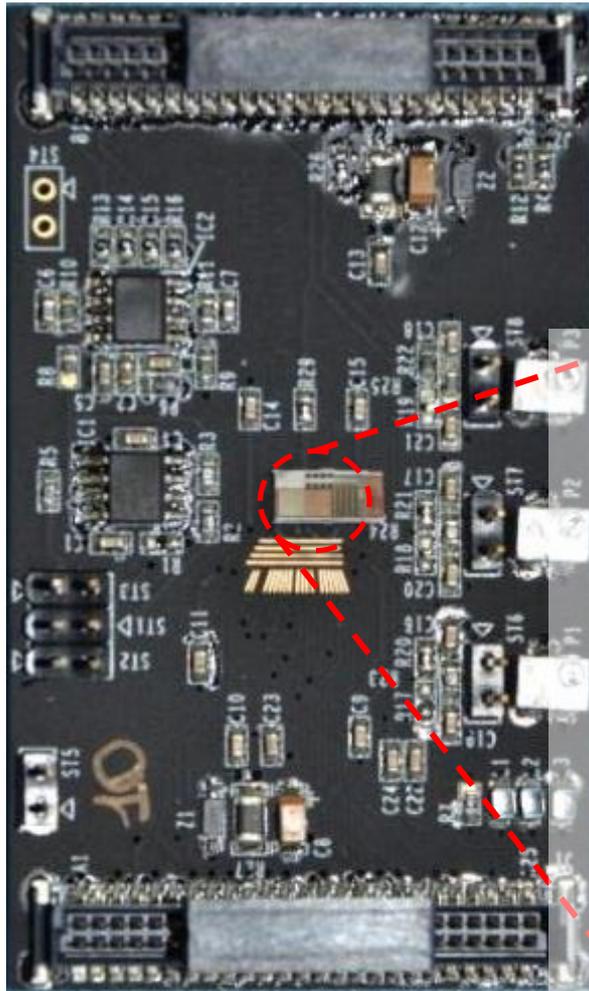
More detail on the collection electrodes

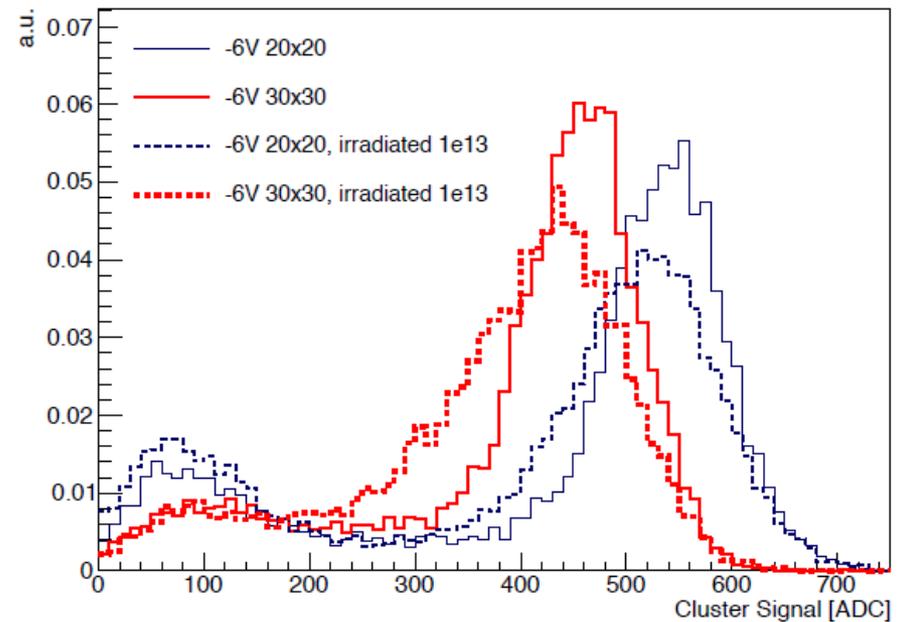| Sector	Type	Diameter [μm]	Spacing [μm]	
1		2	0	smallest diode, lower collection eff.
2		3	0	intermediate performance, S/N lower
3		4	0	larger diode, no spacing, more noise
4		3	0	performance similar to sector 2
5		3	0.6	small spacing, lower efficiency
6		3	1.04	better S/N increasing spacing
7		2	1.54	better collection eff., better S/N, TW
8		3	0	triple well
9		3	1.04	triple well

Charge collection efficiency in Explorer-0

- response to ^{55}Fe X-rays for :

  - seed (highest signal in 5x5 matrix)

  - cluster (5x5 pixels around seed)
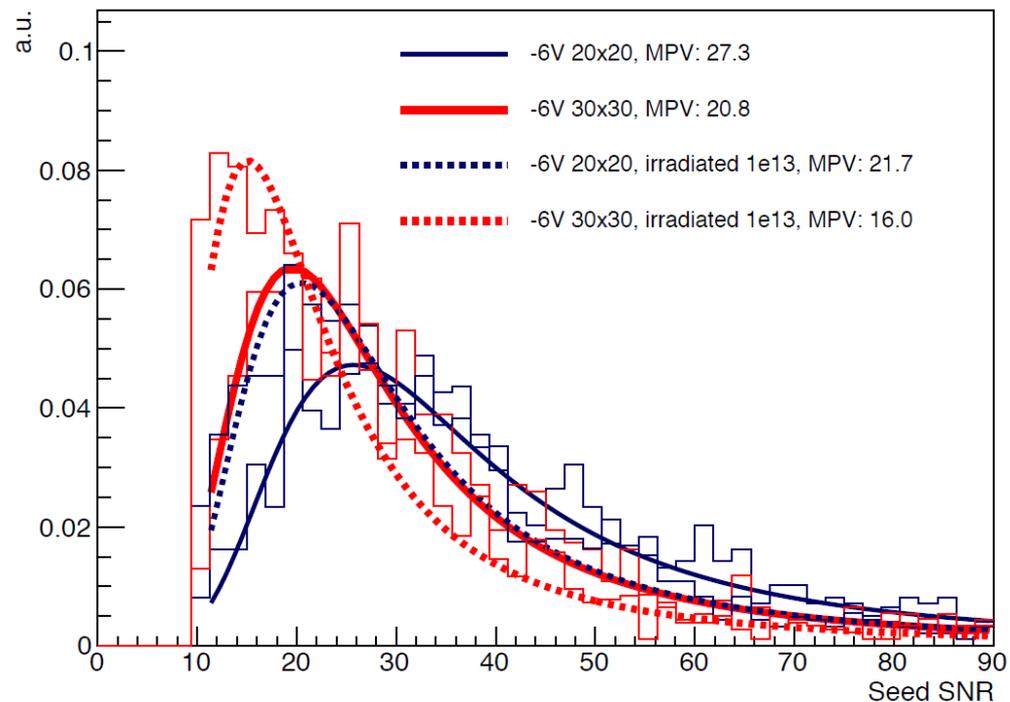
- ^{55}Fe calibration peak → charge calibration (1640 electrons in single pixel)

Seed

Cluster
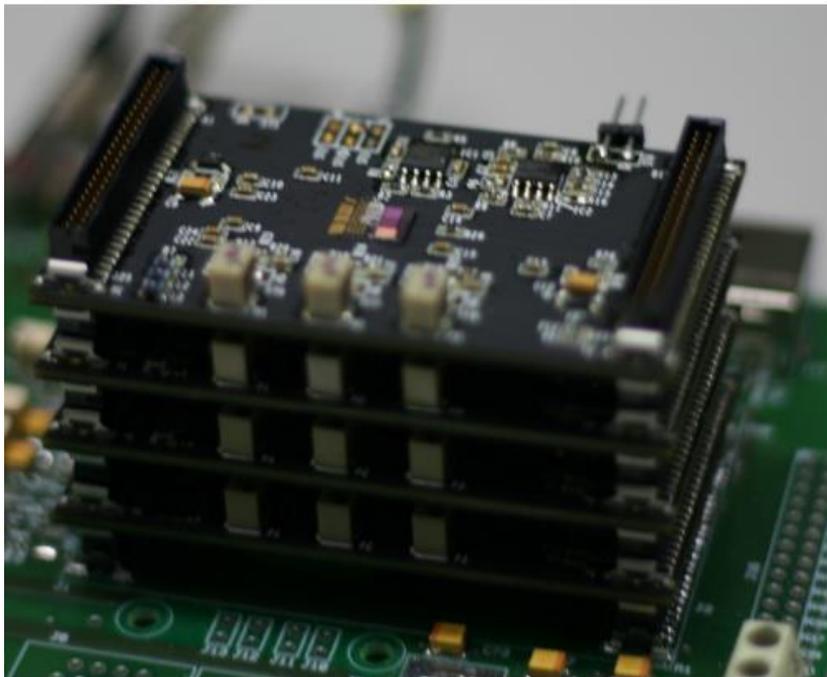
Test beam explorer-0

Legend for plot:
- —— -6V 20x20, MPV: 27.3
- —— -6V 30x30, MPV: 20.8
- ···· -6V 20x20, irradiated 1e13, MPV: 21.7
- ···· -6V 30x30, irradiated 1e13, MPV: 16.0
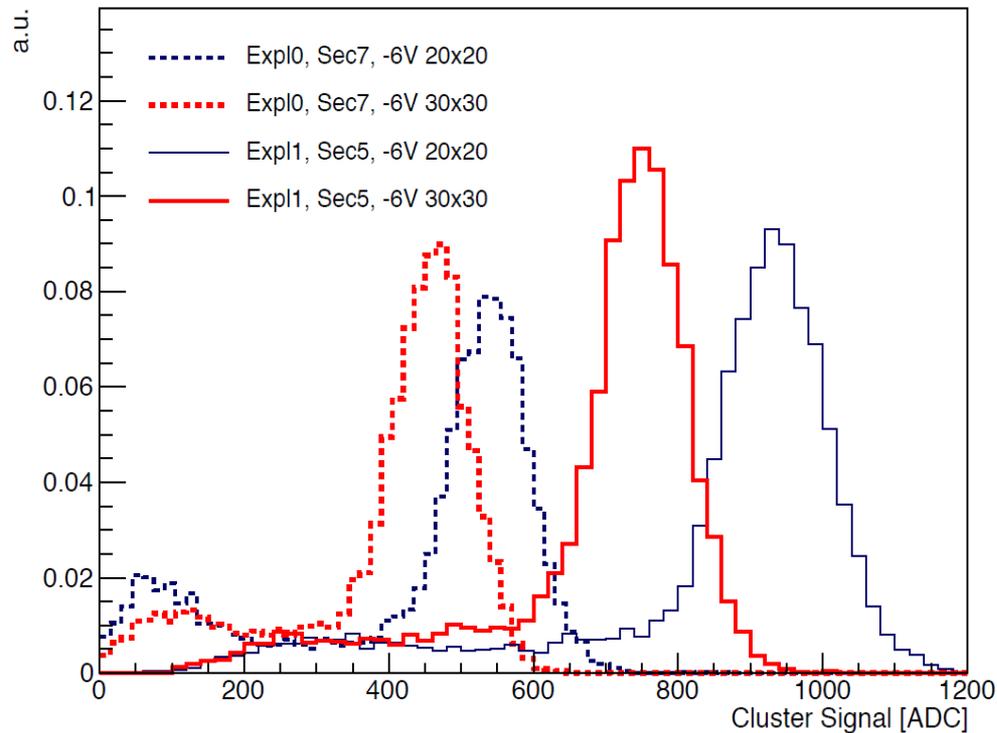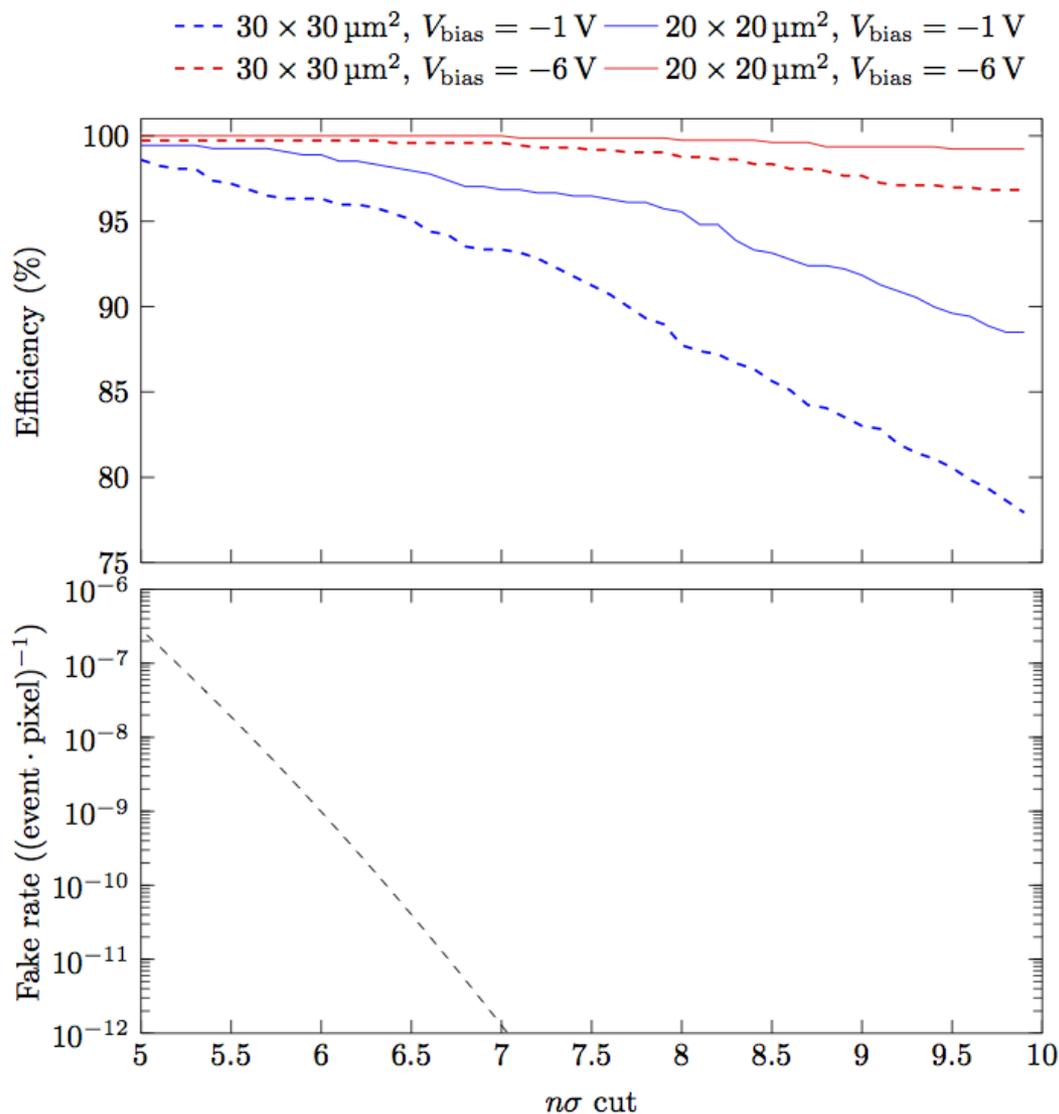
- 4 layers of explorer-0, modified setup of LePix

- 6 GeV/c pions

- Reverse substrate bias gives extra margin

- Penalized by too large input capacitance, corrected for Explorer-1.
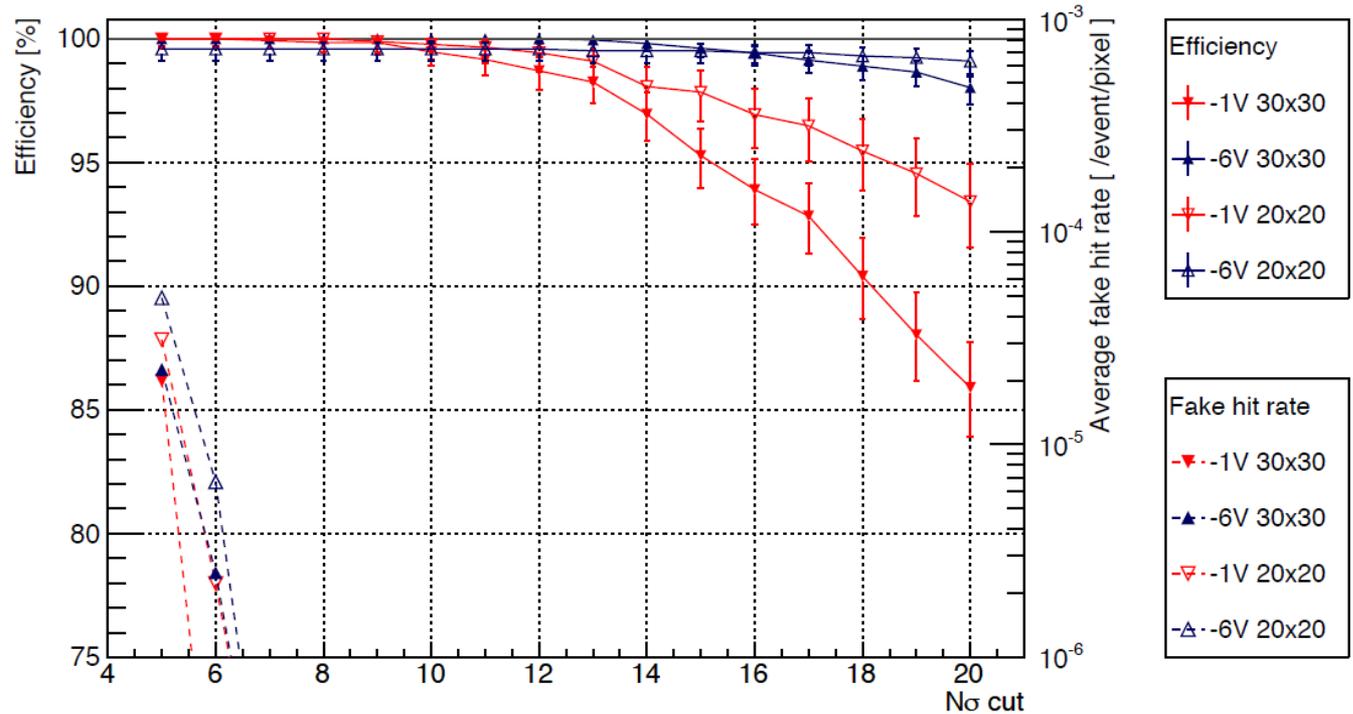
Explorer-1 vs Explorer-0

- Comparison of ^{55}Fe cluster signal for Explorer-0 and Explorer-1

- Explorer-1 shows ~ 2x signal increase, and similar noise level

- Confirms correction on input capacitance, circuit contribution reduced from ~4.6 fF to ~2 fF

- High efficiency at low fake hit rates
- Reverse substrate bias gives extra margin

Efficiency & fake hit rate (Explorer-1)

Explorer-1 results after tests with electrons at DESY, averaged on all diode geometries

- after irradiation drop of 10 - 20% in CCE, recovered with back bias
- better performance of larger diodes with larger spacing to electronics
- wider distance → wider depletion volume → lower input capacitance
- better performance of 20 x 20 µm² at low back bias voltage
- detection efficiency above 99% up to 10σ cut, also after irradiation
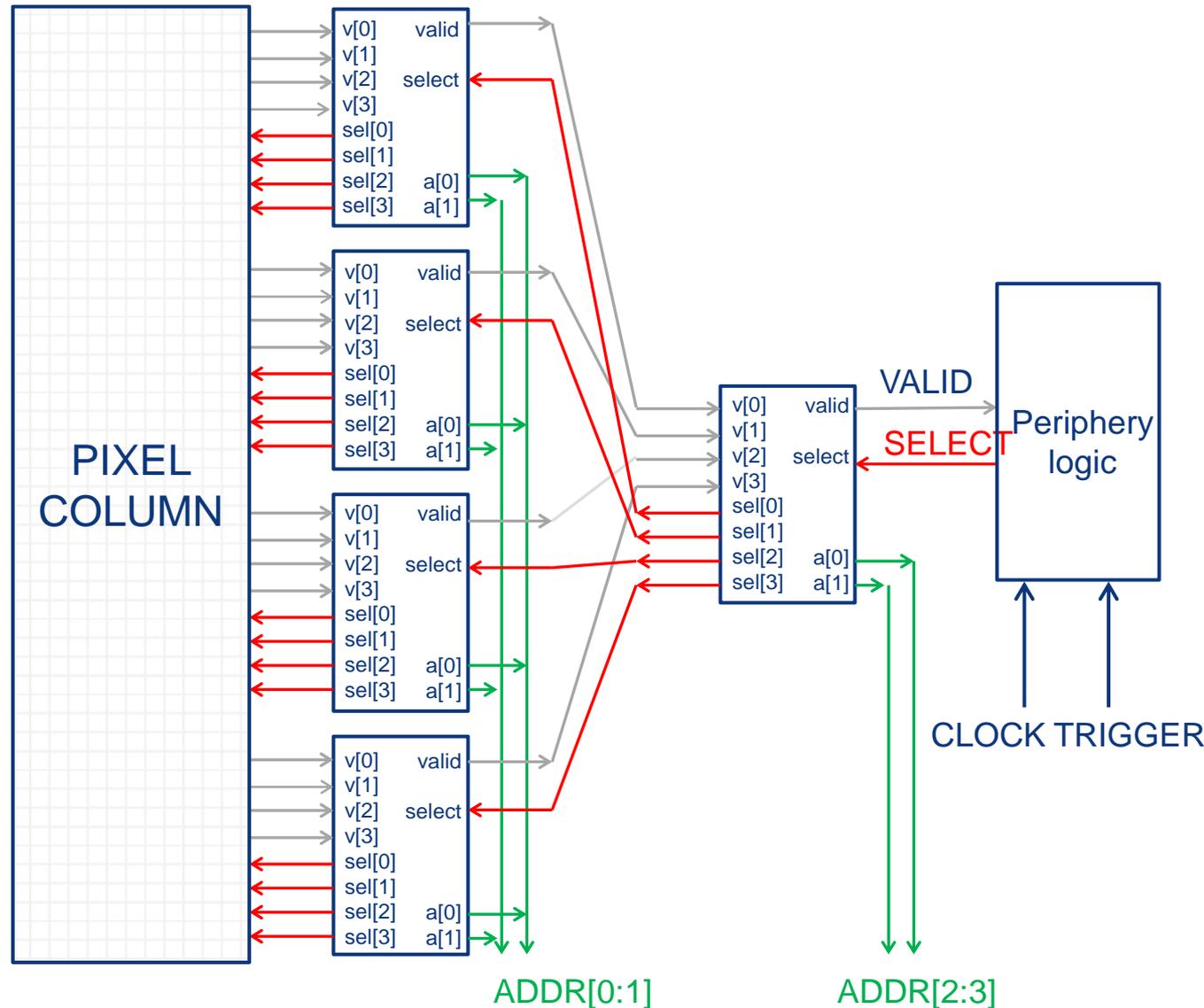
(p)ALPIDE

FRONT END AND READOUT

IN-PIXEL HIT DISCRIMINATION
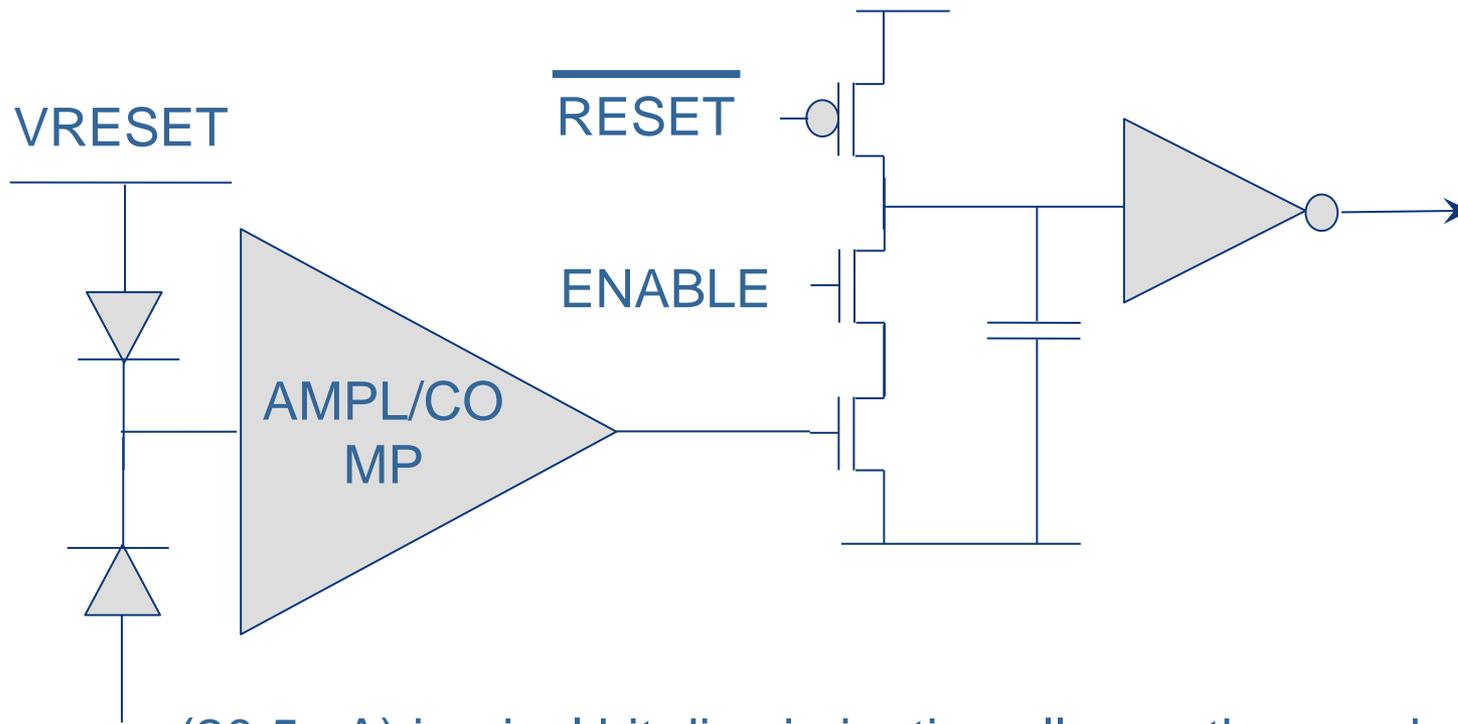
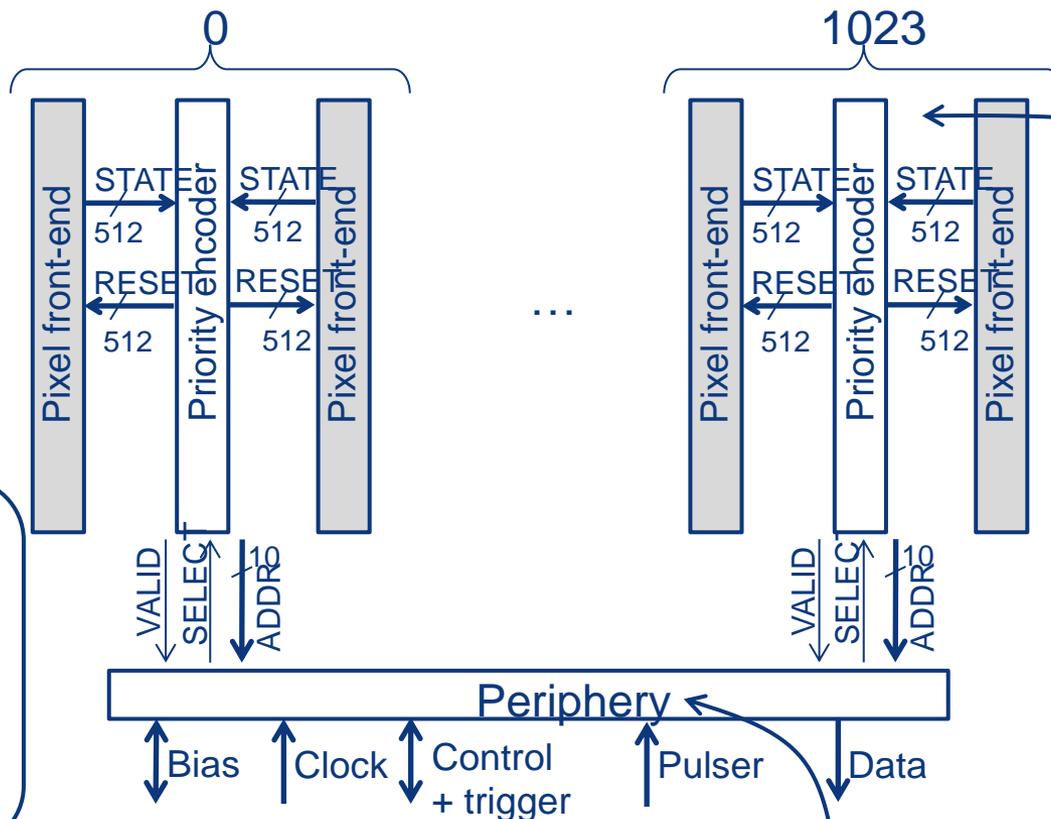- Low power (20.5 nA) in-pixel hit discrimination allows other readout architectures
- Large gain amplifier/comparator discharges ~ 80fF storage capacitor when the sensor receives a particle hit
- Storage capacitor instead of full flip-flop to save space

Priority Encoder readout

- hierarchical readout
- 4 inputs basic block repeated to create a larger encoder
- 1 pixel read per clock cycle

- forward path (address encoder) in gray
- feed-back path (pixel reset) in red

- asynchronous (combinatorial) logic
- clock only to periphery, synchronous select only to hit pixels

PIXEL COLUMN

v[0] valid
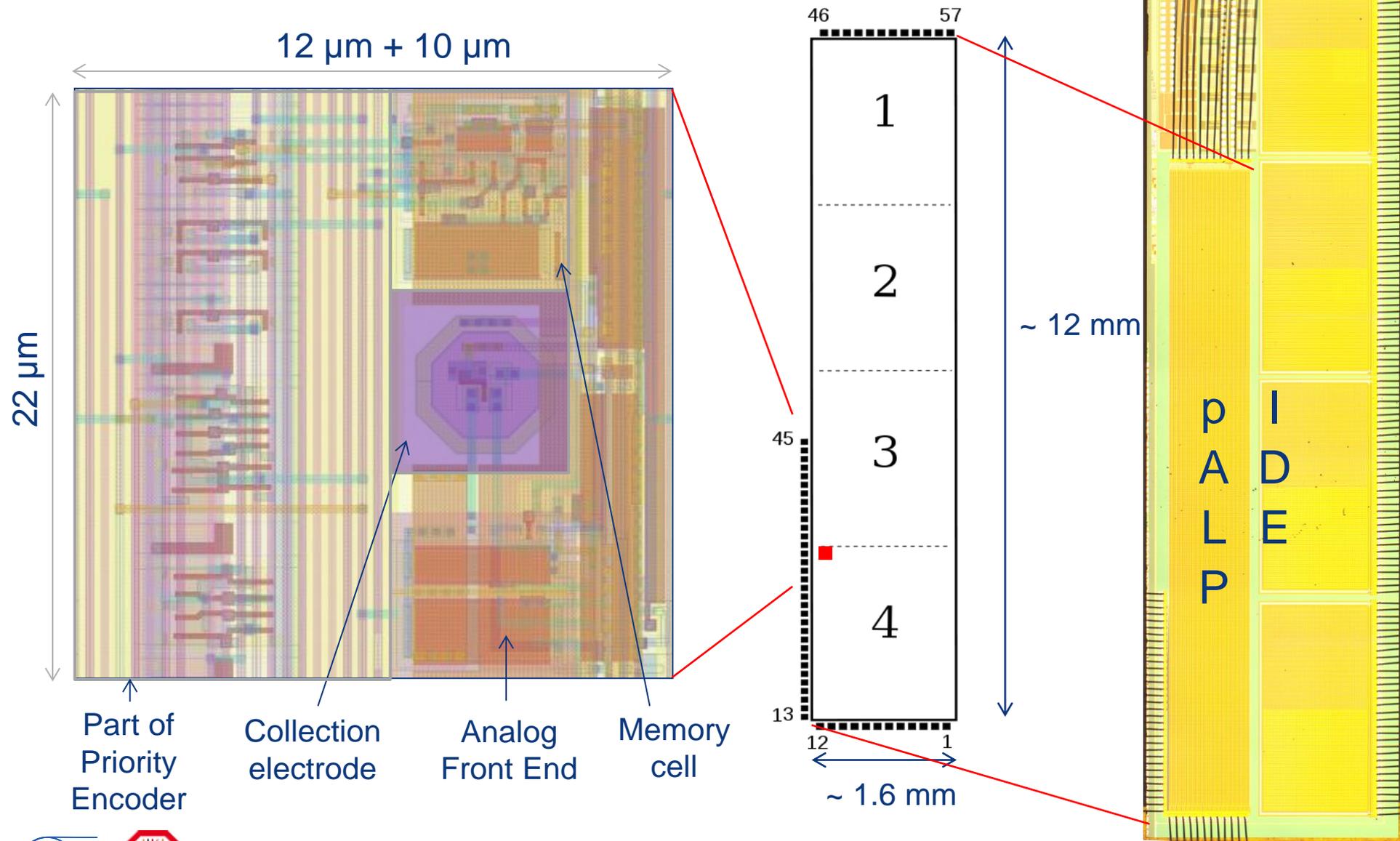v[1]
v[2] select
v[3]
sel[0]
sel[1]
sel[2] a[0]
sel[3] a[1]

VALID

SELECT

Periphery logic

CLOCK TRIGGER

ADDR[0:1]

ADDR[2:3]

ALPIDE: ALice PIxel DEtector

0

1023

- low power in-pixel discriminator
- current comparator (bias of ~20 nA)
- storage element for hit information

Pixel front-end
STATE
512
RESET
512
Priority encoder
STATE
512
RESET
512
Pixel front-end

...

Pixel front-end
STATE
512
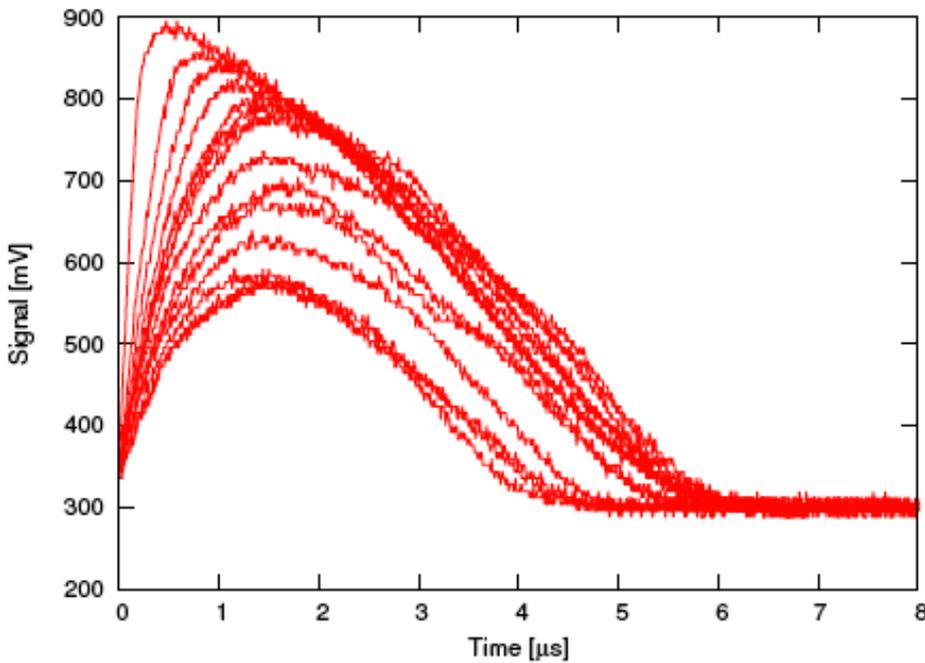RESET
512
Priority encoder
STATE
512
RESET
512
Pixel front-end

- in-matrix address encoder
- tree structure to decrease capacitive load of lines
- outputs pixel address and resets pixel storage element

VALID SELECT 10 ADDR

VALID SELECT 10 ADDR

Periphery

Bias Clock Control + trigger Pulser Data

- loss-less data compression de-randomizing circuit
- compresses cluster information in the column
- multi-event memory

Prototype ALPIDE or pALPIDE (512x64 pixels)

12 μm + 10 μm

22 μm

Part of Priority Encoder

Collection electrode

Analog Front End

Memory cell

46   57

1

2

3

4

45

13

12   1
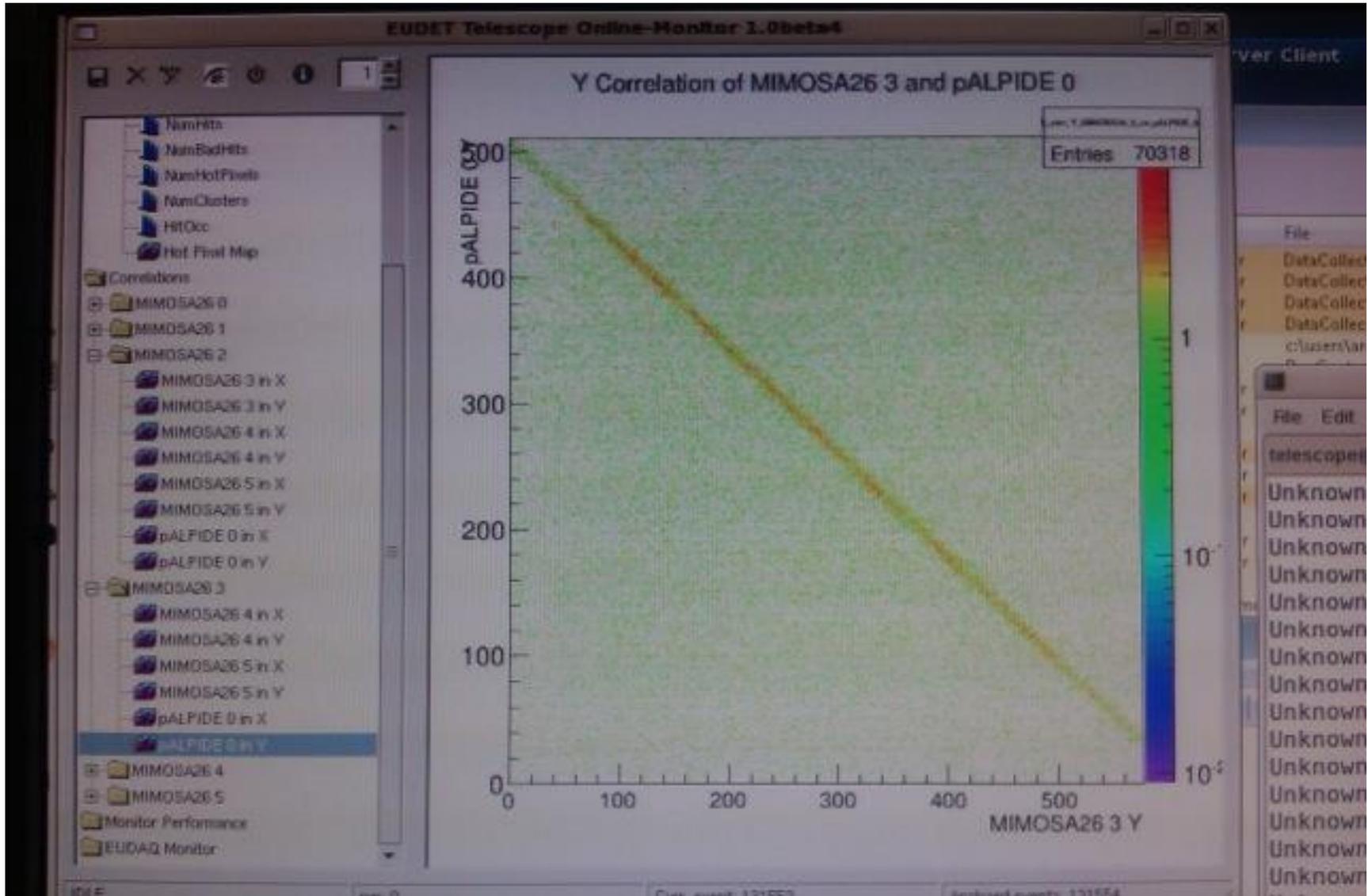
~ 12 mm

~ 1.6 mm

p A L P

I D E

pALPIDE first results

Analog output of one pixel under ^{55}Fe

- Minimum detectable charge <130 e-
- At nominal bias (20.5 nA/pixel) and threshold setting:
  - Threshold spread 17 e-
  - Noise ~ 7 e-

Threshold

$\mu = 242.1\ e^-$
$\sigma = 16.7\ e^-$

Noise

$\mu = 7.24\ e^-$
$\sigma = 0.87\ e^-$
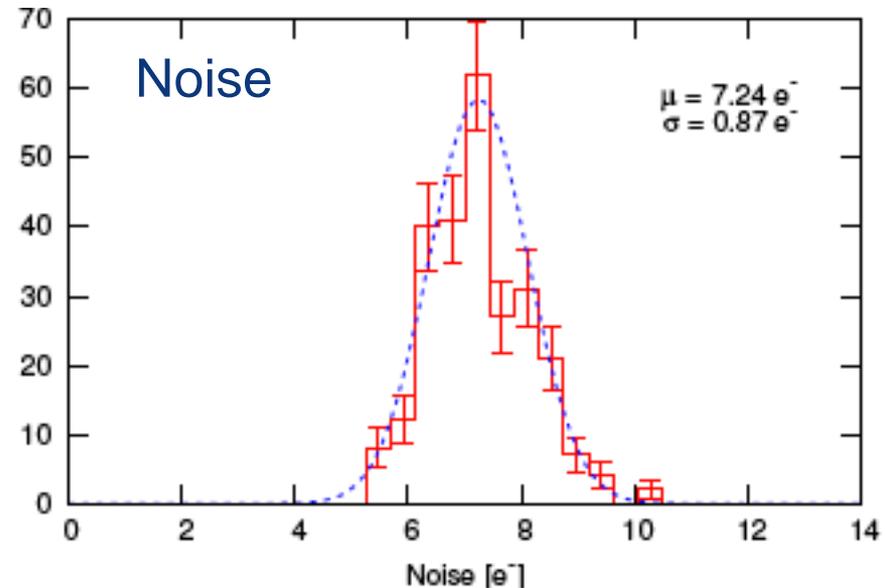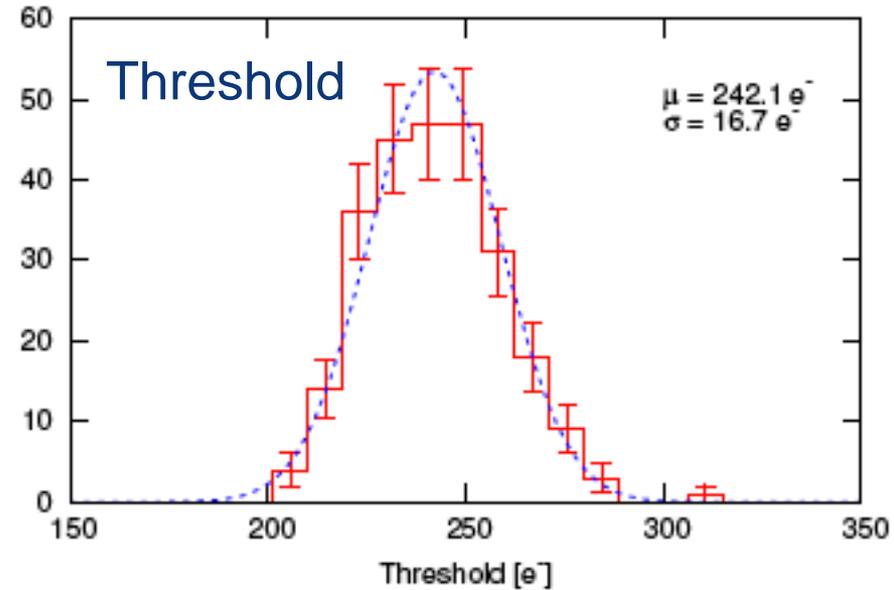
Beam test at DESY … now

CONCLUSIONS

- Pixel sensor
    - 100mV distributed over a few pixels
    - Could we get to digital signal by further optimization?
- Analog front end design: 40nW*250 000 pixels = 10 mW/cm^2

    Promising results, but more work and checking needed.
- Digital: looking at solution around 10mW/cm^2
- Off-chip data transmission ~ 30-50mW/chip or <10mW/cm^2

Trying to approach strip level power consumption per unit area and stay below 50mW/cm^2

- Radiation tolerance sufficient for Alice
- Significant work in progress in design and in test

THANK YOU !