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Monolithic Active Pixel Sensor Development for the Upgrade of the ALICE Inner Tracking System

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ALICE plans an upgrade of its Inner Tracking System for 2018. The development of a monolithic active pixel sensor for this upgrade is described. The TowerJazz 180 nm CMOS imaging Sensor process has been chosen as it is possible to use full CMOS in the pixel due to the offering of a deep pwell and also to use different starting materials.

Several prototypes have already been designed, submitted for fabrication and some of them tested with X-ray sources and particles in a beam. Radiation tolerance up to the ALICE requirements has also been verified.

Summary

For the upgrade of the Inner Tracking System [1] of ALICE at CERN a monolithic active pixel sensor is under development. R&D will be pursued during 2013-2014, with a full conceptual demonstration towards the end of 2013 and a production-ready prototype towards the end of 2014. The TowerJazz 180 nm CMOS imaging Sensor process [2] has been chosen as it is possible to use full CMOS in the pixel due to the offering of a deep pwell and also different starting materials.

A pixel size of about 20x20 μm2 is targeted. To limit material budget power consumption should not exceed 300 mW/cm2, but a reduction below 100 mW/cm2 would really be beneficial. Power is consumed in the sensor chip in the analog and digital circuitry, and also to transmit the data off-chip.

Analog power consumption is determined by the collected charge over capacitance (Q/C) ratio, requiring pixel sensor optimization. An early prototype implemented on an 18 μm thick >1 kΩcm epitaxial layer showed that changing the reset voltage of the detecting diode over a ˜1 V range drastically affects this Q/C ratio. A new prototype allowing reverse substrate bias, similar to earlier ones in another technology [3], was submitted and measured: reverse substrate bias reduces input capacitance and average cluster size, and increases efficiency for a certain charge threshold. Analysis showed that further sensor optimization could be done, both through design but also using different starting materials. An improved test chip has been submitted in an engineering run early April with a split on starting material. A prototype with a ˜40nW in-pixel binary front-end circuit was also included.

Digital power consumption depends on the on-chip architecture and also on cluster size. Apart from the traditional rolling shutter, architectures based on a low-power in-pixel binary front-end like the one mentioned before are investigated to minimize the digital power consumption. In a first architecture, a priority encoder circuit provides the address of the first hit pixel in a sector, and subsequently resets it, so that during the next clock cycle the address of the next hit pixel is made available. This continues until all hits in the sector have been read out. Power is minimized as power is consumed only if hits are present. Another architecture [4] tries to reduce power by reducing the number of signals to be treated. One example yields good reconstruction results for the outer layers and reduces the data from N2 pixels to 4N signals. Prototype circuits for both architectures were also included in the April engineering run.

If the aforementioned low-power front end in combination with one of the above architectures is successful, data transmission may very well be the dominant power contributor: about 2Gbit/s is required for a 1.5x3 cm2 pixel sensor.

Measurements with X-ray sources and particles in a beam will be presented. Radiation tolerance up to the modest ALICE requirements (Total Ionizing Dose < 700 kRad, Non-Ionizing Energy Loss < 1013 neq/cm2) has also been verified.

References
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