Radiation-Hardened-By-Design Clocking Circuits in 0.13 µm CMOS Technology

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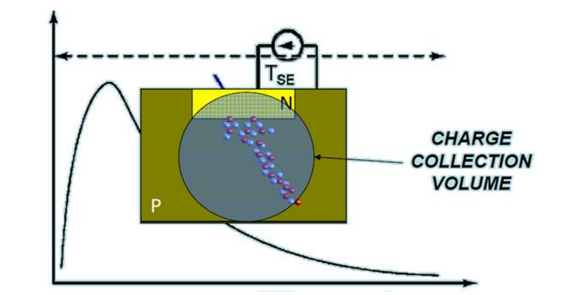
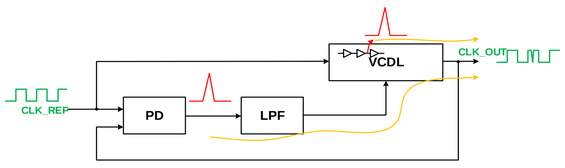
Motivation



(a)



(b)

Fig.1 (a) Single Event Effects (SEE) [Raoul Velazco] (b) SEE on the timing circuit (DLL)

- A result of the interaction between the radiation and the electronic device is SEE
- The incident particle generates a dense track of electron hole pairs and cause a transient current pulse
- In the timing circuits (such as DLL), SEE will cause a state flip to the digital logic and the delay units in the VCDL
- A radiation strike can cause the DLL to lose lock, which results in the loss of synchronization and incorrect data transmission

Circuit Solution

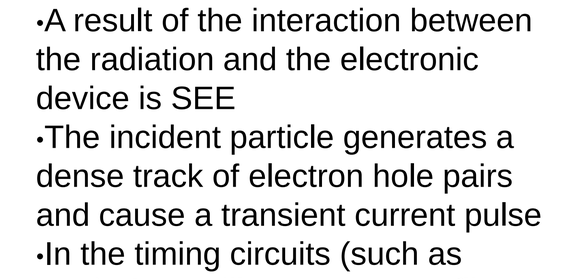


Fig.2 12.5 MHz~500 MHz Radiation-Hardened-By-Design Phased-Locked Loop

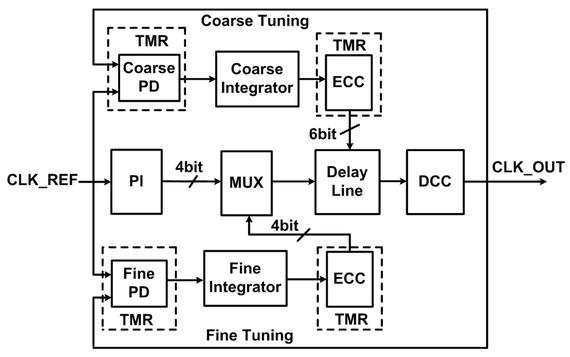
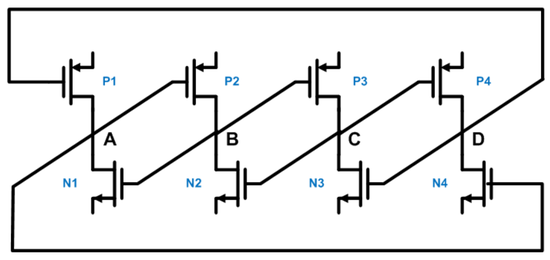
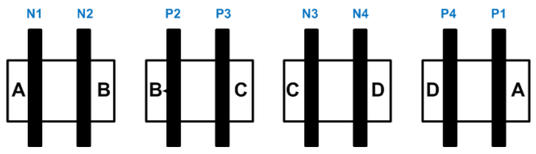


Fig.3 267MHz Radiation-Hardened Delayed-Locked Loop

- Single-event-hardened phase-locked loop (PLL) for structured-ASIC and digital delay-locked loop (DLL) for DDR2 memory interface applications
- The PLL covers a frequency range from 12.5 MHz to 500 MHz with an RMS jitter of 4.7 pS
- The radiation-hardened design techniques in the PLL include dual interlock cell flip-flop application, cross-coupled VCOs and charge compensation circuit in the loop filter
- The DLL operates at 267 MHz and has a phase resolution of 60 pS
- All digital architecture of the DLL makes digital radiation-hardened techniques possible.
- The two circuits are hardened against SEEs for charge injection of 250 fC and consume 17 mW and 22 mW of power, respectively

Radiation-Hardened PLL





Physically Separate 8 Sensitive Transistor Pair

Condition I	[A B C D]=[1 0 1 0]			
Sensitive Pair	N1:N3	P2:P4	P2:N3	P4:N1
Condition II	[A B C D]=[0 1 0 1]			
Sensitive Pair	P1:P3	N2:N4	P1:N2	P3:N4

Fig.4 DICE latch and its layout principle

- Dual interlock cell flip-flop is used in designing the phase frequency detector, frequency divider, lock detector, and all other sequential logic blocks to eliminate single event upset
- Layouts of the Dice cells are optimized by separating the sensitive transistor pairs physically

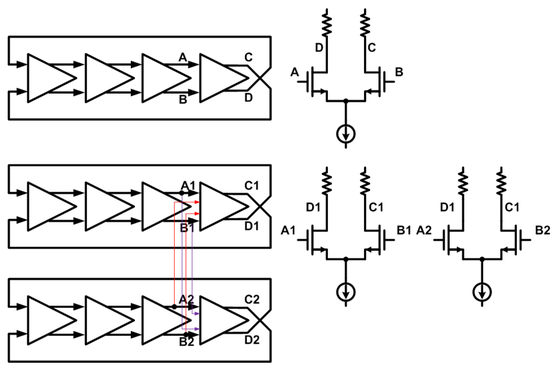


Fig.5 Split Ring VCO

- The voltage-controlled oscillator is designed with two VCOs being cross-coupled to achieve quick recovery by compensating each other during SET

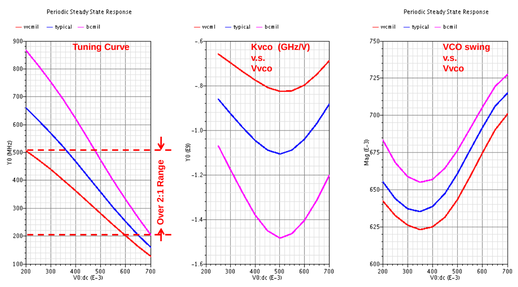


Fig.6 VCO tuning ranges, conversion gain and output amplitude

- The VCO is designed to cover a octave tuning range from 250 MHz to 500 MHz
- Phase noise of the VCO at 1 MHz offset frequency is from -98.9 dBc/Hz to -105 dBc/Hz

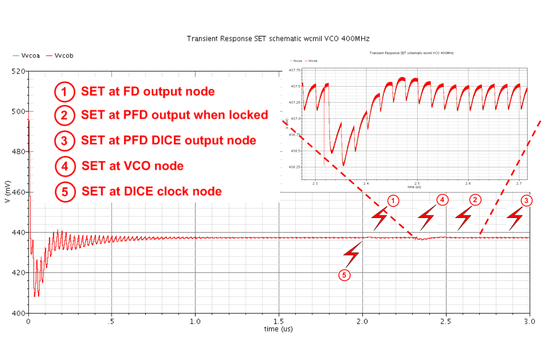


Fig.7 VCO control voltage under single event transient effect (PLL is locked)

- Single event upset is modeled as a 2 mA current pulse with a width of 100 ps
- The current pulses are applied to different nodes in the PLL. The VCO control voltage is observed

PLL V_{ctr} Compensation Solution

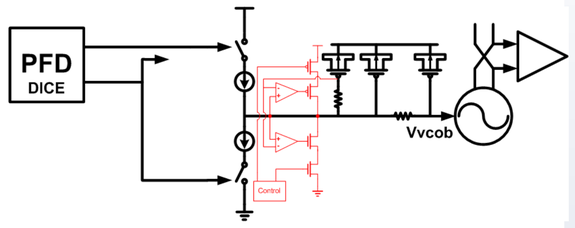


Fig.8 Compensation Solution for SET at the PLL CP output

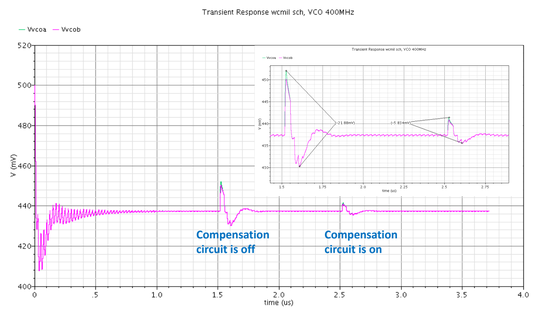


Fig.9 Compensation Result

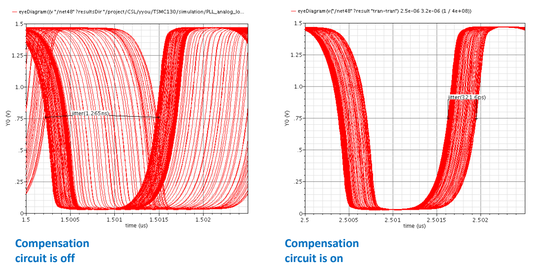


Fig.10 Output clock jitter comparison for PLL w/wo V_{ctrl} compensation circuit

Radiation-Hardened DLL

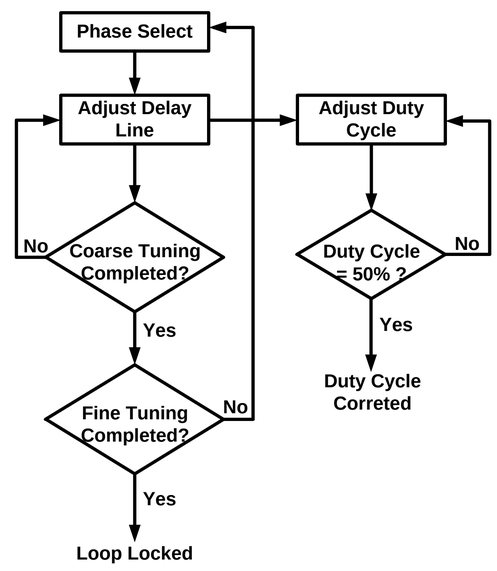


Fig.11 DLL operation procedure

- The DLL operation includes a coarse tuning and a find tuning process
- Duty cycle correction is needed for the DDR application

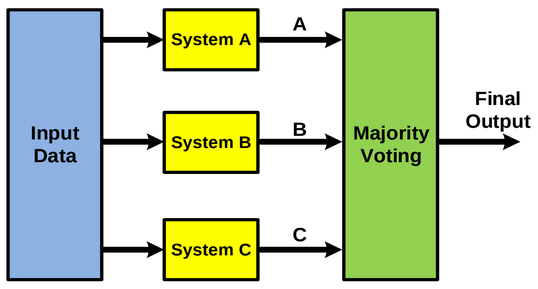


Fig.12 Radiation hardened-triple modular redundancy (TMR)

- Three devices will do the same task and a block selects the most “popular” output
- Coarse/Fine PDs and coding logics in this design are protected by TMR

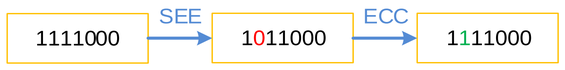


Fig.13 Error correction coding for accumulators

- Loop filter (accumulator) outputs are thermometer coded and protected by Error Correction Coding
- Bubble correction

DLL Duty Cycle Correction Circuit

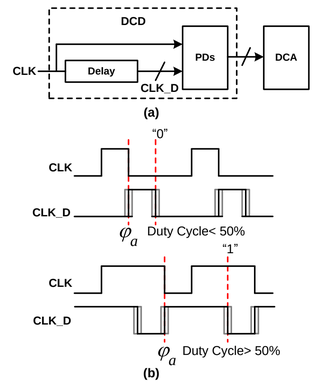


Fig.14 (a) Duty cycle detection circuit (b) Duty cycle detection principle

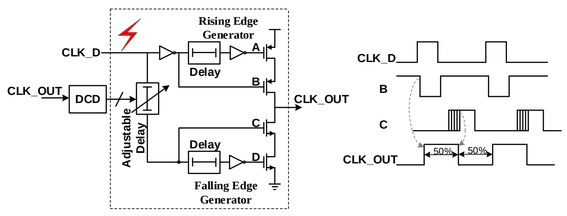


Fig.15 Radiation-hardened duty cycle corrector

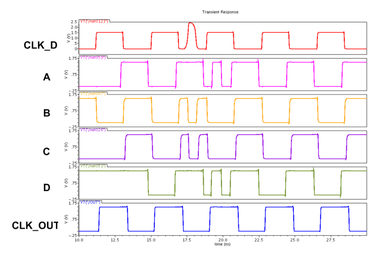
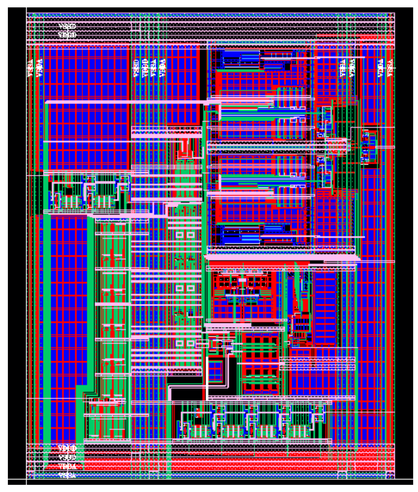


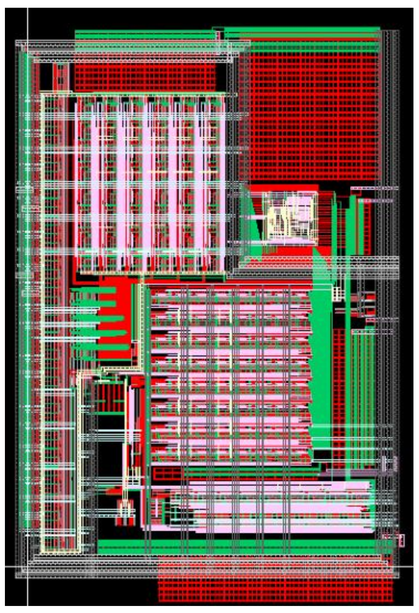
Fig.16 Duty cycle corrector signal waveforms under SEE

Layout and Summary



Technology	130nm CMOS
Architecture	Type II Analog RPLL
Core Area	0.66mmx0.83mm
Supply Voltage	1.5V±10%
Power Consumption	~17mW
Frequency Range	12.5MHz~500MHz
Output RMS RJ	4.7pS (Maximum)
SEE Solution	DICE-latch, Split RVCO, 3-order LPF, V_{ctrol} compensation

Fig.17 PLL layout and performance summary



Application	DDR2 Memory De-skew
Technology	130 nm CMOS
Core Area	0.85 mmx1.2 mm
Supply Voltage	1.5V±10%
Power Consumption	22mW
Input Reference	267MHz
Duty Cycle Distortion	+/-2% reference cycle (74.9 ps)

Fig.18 DLL layout and performance summary

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