Radiation-Hardened-By-Design Clocking Circuits in 0.13 µm CMOS Technology

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Motivation

- A result of the interaction between the radiation and the electronic device is SEE.
- The incident particle generates a dense track of electron hole pairs and cause a transient current pulse.
- In the timing circuits (such as DLL), SEE will cause a state flip to the digital logic and the delay units in the VCDL.
- A radiation strike can cause the DLL to lose lock, which results in the loss of synchronization and incorrect data transmission.

Circuit Solution

- Single-event-hardened phase-locked loop (PLL) for structured-ASIC and digital delay-locked loop (DLL) for DDR2 memory interface applications.
- The PLL covers a frequency range from 12.5 MHz to 500 MHz with an RMS jitter of 6.7 pS.
- The radiation-hardened design techniques in the PLL include dual interlock cell flip-flop application, cross-coupled VCOs and charge compensation circuit in the loop filter.
- The DLL operates at 267 MHz and has a phase resolution of 60 pS.
- All digital architecture of the DLL makes digital radiation-hardened techniques possible.
- The two circuits are hardened against SEEs for charge injection of 250 fC and consume 17 mW and 22 mW of power, respectively.

Radiation-Hardened PLL

- The voltage-controlled oscillator is designed with two VCOs being cross-coupled to achieve quick recovery by compensating each other during SET.
- The PLL covers a frequency range from 130 MHz to 500 MHz.
- Phase noise of the VCO at 1 MHz offset frequency is from -88.9 dBc/Hz to -105 dBc/Hz.

DLL Duty Cycle Correction Circuit

- The DLL operation includes a coarse tuning and a find tuning process.
- Duty cycle correction is needed for the DDR application.
- Three devices will do the same task and a block selects the most “popular” output.
- Coarse/Fine PDs and coding logic in this design are protected by TMR.

Layout and Summary

- Loop filter (accumulator) outputs are thermometer coded and protected by Error Correction Coding.
- Bubble correction.

Fig.1 (a) Single Event Effects (SEE) (Royal Velcro) by SEE on the timing circuit (DLL)
Fig.1 (b) SEE on the timing circuit (DLL) Layout and performance summary
Fig.2 12.5 MHz~500 MHz Radiation
Fig.3 267MHz Radiation
Fig.4 DICE latch and its layout principle
Fig.5 Split Ring VCO
Fig.6 VCO tuning ranges, conversion gain and output amplitude
Fig.7 VCO control voltage under single event transient effect (PLL is locked)
Fig.8 Compensation Solution
Fig.9 Compensation Result
Fig.10 Output clock jitter comparison for PLL w/ VCO
Fig.11 DLL operation procedure
Fig.12 Radiation hardened triple modular redundancy (TMR)
Fig.13 Error correction coding for accumulators
Fig.14 Duty cycle detector in circuit (b) Duty cycle detection principle
Fig.15 Radiation hardened duty cycle detector
Fig.16 Duty cycle correction signal waveform of SEE
Fig.17 DLL layout and performance summary
Fig.18 DLL layout and performance summary