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Radiation-Hardened-By-Design Clocking Circuits in 0.13µm CMOS Technology

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We present single-event-hardened phase-locked loop for structured-ASIC and digital delay-locked loop for DDR2 memory interface applications. The PLL covers a frequency range from 12.5 MHz to 500 MHz with an RMS jitter of 4.7 pS. The DLL operates at 267 MHz and has a phase resolution of 60 pS. Designed in 0.13 µm CMOS technology, the PLL and the DLL are hardened against SEEs for charge injection of 250 fC. The PLL and the DLL consumes 17mW and 22mW of power under 1.5V power supply, respectively.

Summary

In this paper, we present single-event-hardened phase-locked loop for structured ASIC and digital delay-locked loop for DDR2 memory interface applications. The PLL and the DLL are designed in a 0.13-µm standard CMOS digital technology and are hardened against SEEs for charge injection of 250 fC

All of the blocks in the PLL are designed by using RHBD techniques to reduce single-event effects. Dual interlock cell flip-flop is used in designing the phase frequency detector, frequency divider, lock detector, and all other sequential logic blocks to eliminate single event upset and to minimize effect of single event transient on the PLL performance. The voltage-controlled oscillator is designed with two VCOs being cross-coupled to achieve quick recovery by compensating each other during SET. For the most vulnerable node of the PLL, the output of charge pump, a proposed charge compensation circuit is developed to compensate the SEE-induced charge in order to minimize the SEE impact on the PLL output jitter. In addition, a third-order loop filter is used to further purify the VCO control voltage. The entire PLL only uses normal transistors. It covers a frequency range from 12.5 MHz to 500 MHz with an RMS random jitter of 4.7pS. The PLL consumes 17mW of power under 1.5V power supply and occupies an area of 0.55mm2.

The DLL is designed using a dual-loop structure which includes a coarse tuning loop and a fine tuning loop. In the DLL operation, the coarse tuning loop is first launched and is used to adjust a multiplexer-based digital controlled delay line (DCDL) until the phase difference between the output clock and the reference clock is within one multiplexer delay. The phase detection is protected by TMR. The multiplexer-based DCDL allows thermometer coding with error correction to protect the loop digital integrator from SEEs. The ECC logic itself, on the other hand, is protected by TMR. After the coarse tuning process, the fine tuning loop takes over the locking operation. It adjusts a phase interpolator to reduce the phase difference. The phase interpolator achieves a phase resolution of 60 ps. The phase detector and the digital integrator in the fine tuning loop operate in a similar manner as those in the coarse tuning loop and are also protected by ECC and TMR. In addition, a duty cycle corrector (DCC) is designed in the DLL to satisfy the DDR memory interface requirement. The DCC can self-counteract the SEEs by properly setting the delay components inside the duty-cycle adjustor circuit. The DLL operates at 267 MHz with a 1.5 V supply and consumes 22 mW of power. The DLL completes the locking process within 100 ps and achieves a phase resolution of 60 ps.

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