Messages from our friends

a few slides about xTCA projects of colleagues that did not manage to come to Perugia

RCE status update
(DOE Detector R&D program on H/P DAQ Systems)

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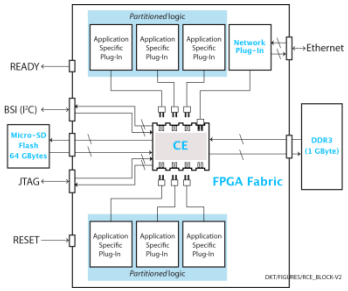
Used for the ATLAS CSC read-out after LS1

The (US) baseline for the ATLAS NSW RODs, the DAQ system for the LSST camera as well LBNE and HPS

LSST - Large Synaptic Survey Telescope. Optical telescope with the largest digital camera ever built (> 6 Gigapixels)
LBNE - Underground, long baseline Neutrino experiment using Fermilab beams located in Homestake mine in South Dakota (USA)
HPS - Heavy Photon Search. Discovery experiment at Jefferson Laboratory looking for anomalous (non-standard model) photons.

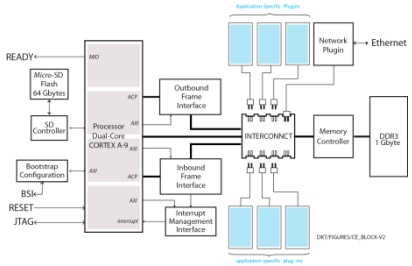
Architecture Overview

CE



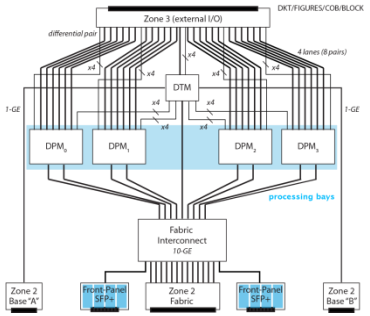
Heart of →

RCE



Use on →

COB

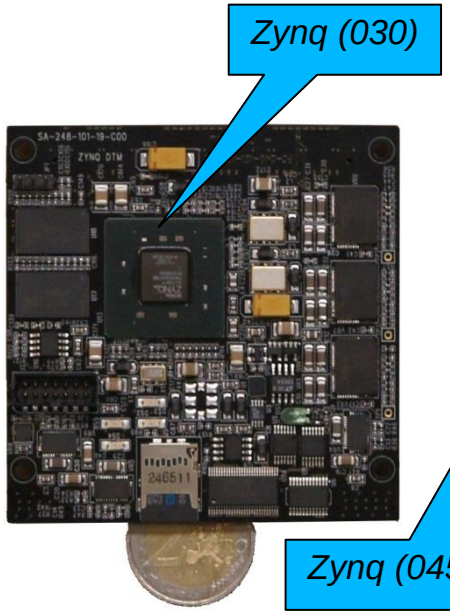


- ARM (dual-core) A-9 @ 900 MHz
- Bootstrap configuration
  - External I2C interface
  - Communicates with IPMC
- Socket Interface for plugins
  - Transfer data in units of *frames*
- Software (bundled with CE):
  - Linux: Based on 3 series kernel
  - RTEMs: RT kernel
- TCP/IP stack
- Plugin socket library

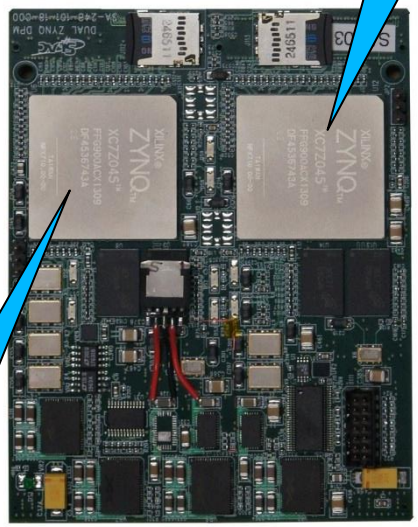
- *Based on SOC technology: Xilinx Zynq*
- *Three principal components:*
  - *Programmable FPGA Fabric*
    - *Both soft & hard silicon (resources)*
    - *Equivalent in size to (large) Kintex 7-series*
    - *900 DSP tiles (> 200 TeraMACS/Sec)*
    - *12 SerDes support up to 12.5 Gbits/s*
- *Programmable Cluster-Element (CE)*
    - *Includes MicroSD (up to 64 Gbytes)*
    - *1 Gbyte of RAM (DDR3)*
    - *10-GE Ethernet interface (as a plugin)*
    - *Plug & socket model "glues" plugins to CE*
- *User plugins*

- *Designed to satisfy ATLAS Phase-1 needs and facilitate Phase-2 R & D*
- *ROD replacement for CSC (Phase-0)*
- *(US) baseline for NSW MM-RODs (Phase-1)*
- *Option for AFP Silicon & timing readout (Phase-0/1)*
- *ATCA compliant Front (carrier) board*
- *Full Mesh board (10-GE) on fabric interface*
- *Node board on base interface*
- *Fully IPM compliant*
- *A cluster of up to 17 RCE's*
  - *4 Data Processing Modules (DPM)*
  - *Contains 1 to 4 RCEs*
- *1 Data Transport Module (DTM)*
  - *Contains 1 RCE*
  - *Manages switch & application specific timing*

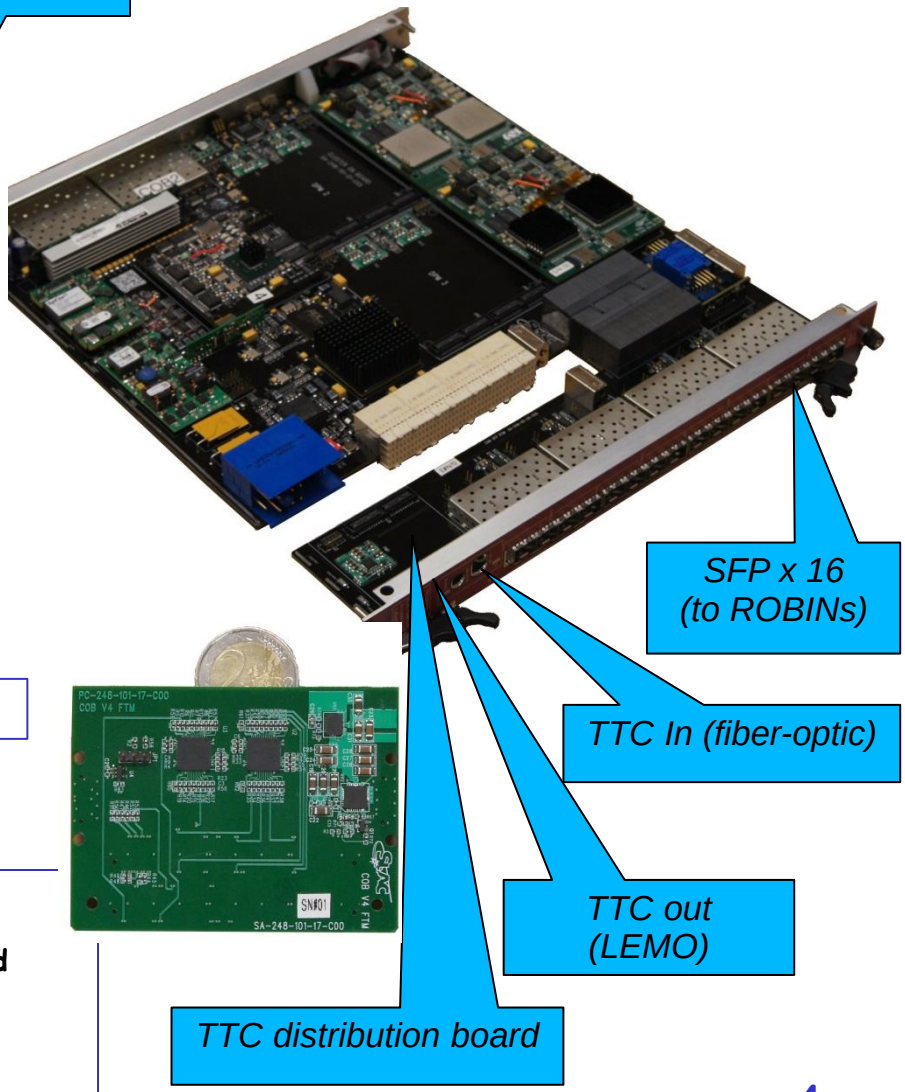
COB + RTM + TTC mezzanine



- DTM (G3)



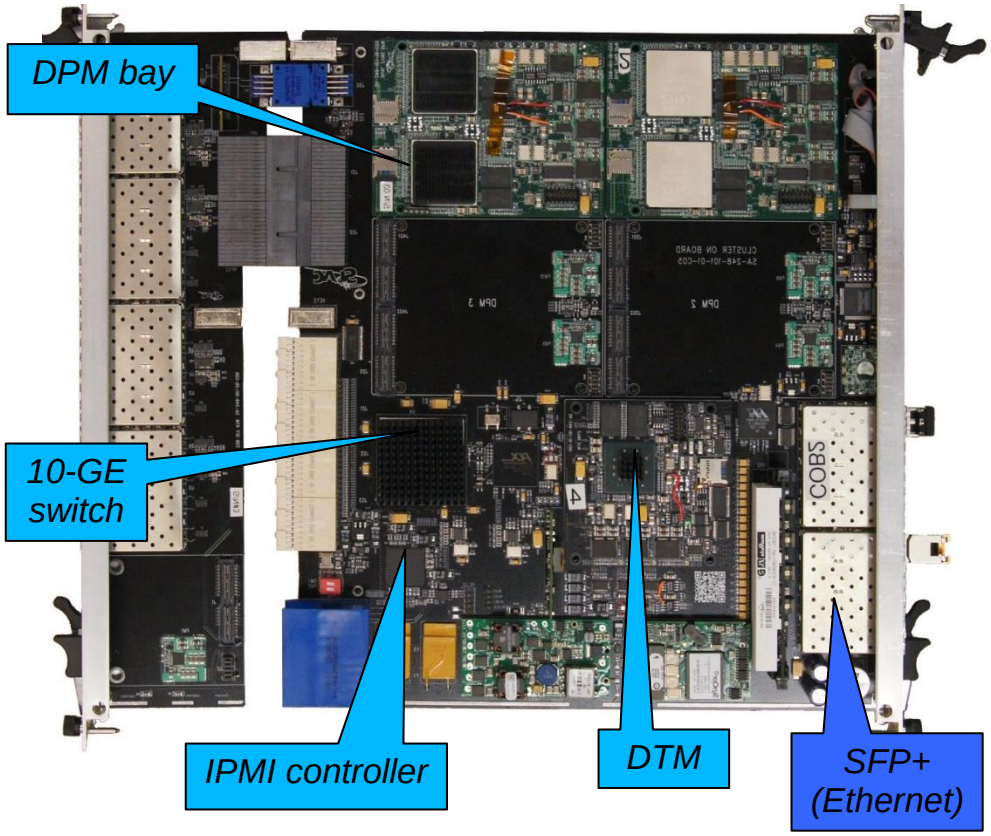
- (dual element) DPM (G3)



- TTC distribution board Status:
  - Prototype functional & signal integrity verified
  - Production schematic complete & in layout
- Firmware status:
  - BPM encoder/decoder functional & operating

COB Status (NRC ATCA-Front-Board)

- *Prototypes (RTMs and COBs) done*
- *Production was scheduled for April 2014, but it will probably be closer to beginning of summer*
- *Proof-Of-Principal of OpenHPI (and thus the shelf manager) interfacing to the ATLAS controls has been demonstrated*
    - *still a lot of on-going work necessary in this area*
- *Begun testing of TTC interface*
- *SCA controller design prototyped and waiting for COB hardware to integrate with.*
- *The most important concern: base program completion (the COB and RCE).*
    - *Focus has shifted from hardware to firmware and software*



Production prototype

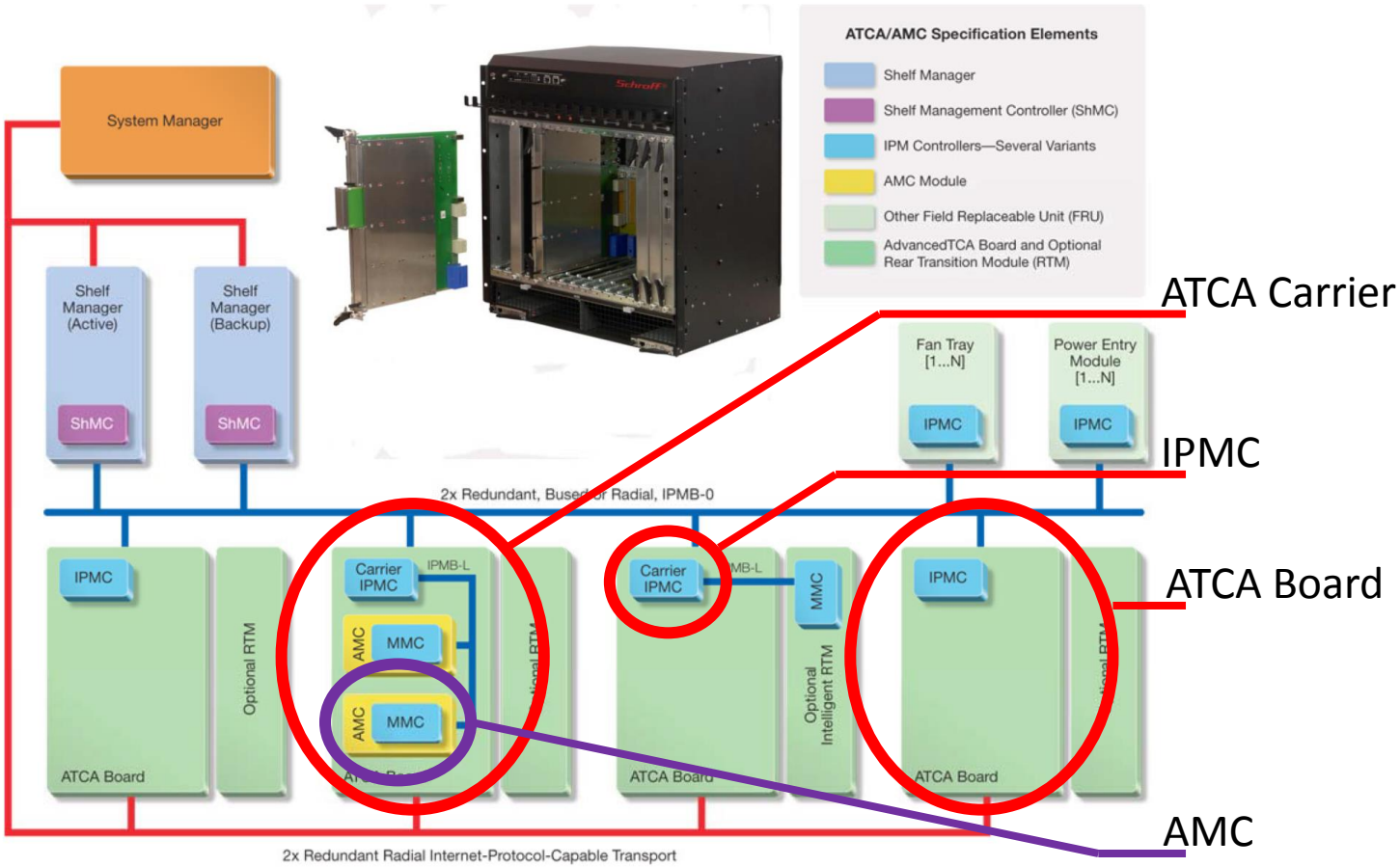
- ***From prototype to Production board***
    - ***Timing distribution (TTC) moved from COB to RTM***
    - ***SFP+ (external Ethernet) moved from RTM to COB***
    - ***Denser connector in P3 (enables move from 48 to 96 lanes)***

SCA - Switched Capacitor Analog (Memory). The sensors for the CSC detector electronics.

LAr ATCA developments

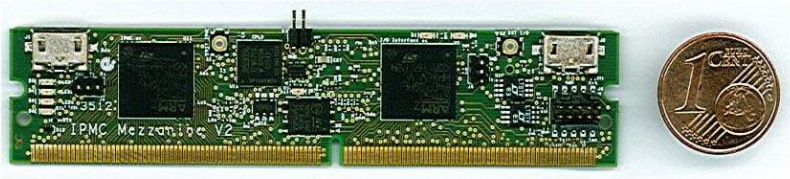
Annecy, Arizona, Brookhaven, Dresden, Stonybrook

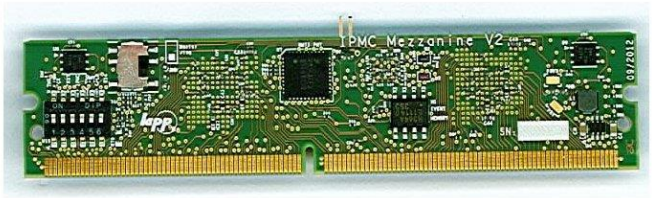
ATLAS Liquid Argon Calorimeter Phase I Upgrade (2018):
Readout of LAr Fine Granularity trigger towers for L1Calo Trigger



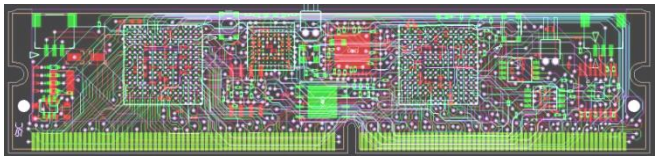
Contact: Guy.Perrot@lapp.in2p3.fr

IPMC Mezzanine V2- V2.1 & Test Board



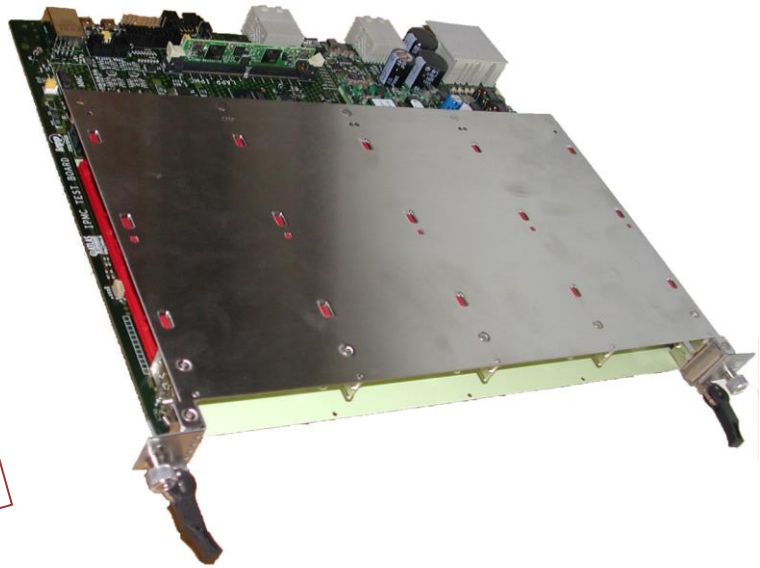


V2.0



V2.1

Will also be used by LHCb



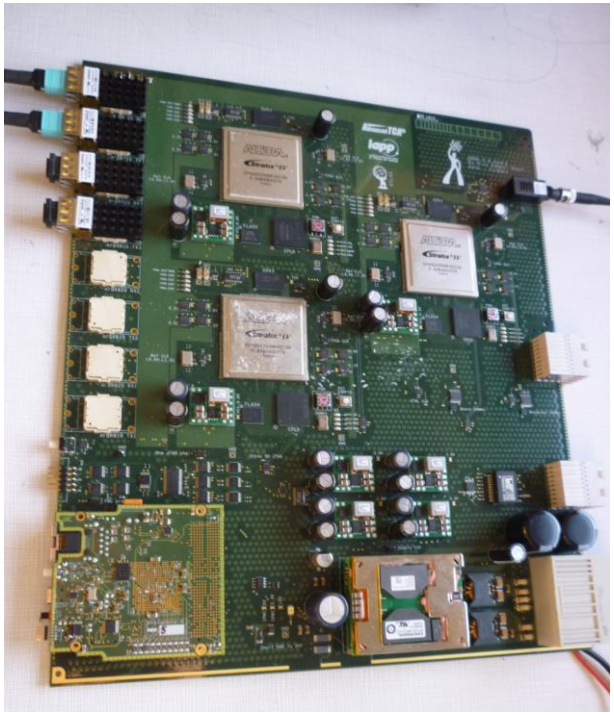
IPMC

- Ten boards produced in V2.0
  Only a few still available
- Basic firmware with no AMC and User support. No evolution foreseen
- Twenty boards being produced in V2.1
  Ten available end November, the others in December
- Complete firmware available middle December. User tools only next year

IPMC Test Board

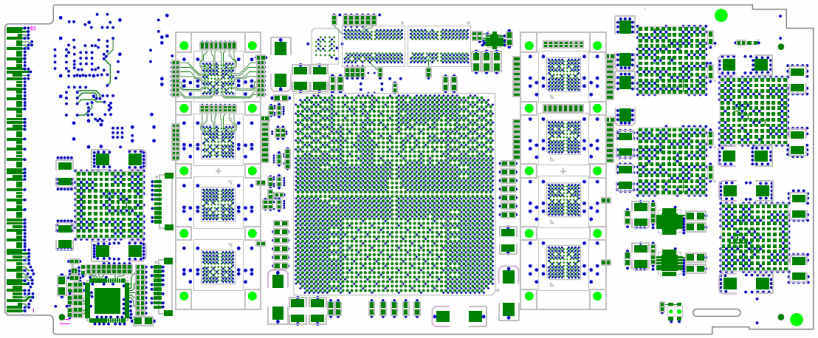
- Four Boards received in March
  Three Boards OK, one to be repaired
- Five more boards being produced.
  Availability End November
- Manual and design files available

Trigger Towers Readout Developments



"ROD" Evaluator

- Takes data from front end trigger digitizer and outputs to the future L1Calo system.
- To evaluate link performances, DSP computing performances
- High speed and density optical links (48 Rx, 48 Tx, 8.5 Gbps)
- 3 High density FPGA for computing (Altera Stratix IV)
- Two boards used by LAPP and two more in production ready by end of year. More boards built by Tokyo
- One card will be installed in each CERN EMF (Q4 2013)
- Two cards in USA15 (2014/5) for first readout of Lar Trigger Digitizer Board (LTDB)



AMC Based Optical test Board

- To evaluate front optical links placement and techniques
- Based on Xilinx Virtex-7 and Avago micro-pods arrays
- 8 micro-pods (4 as receivers and 4 as transmitters)
- Specific non commercial radiator for cooling 4 micro-pods
- Optical pigtail between 4 micro-pods and one front panel 48 fibers MPO/MTP connector.
- 8 PCBs but only 2 boards built end November

Next: Design of final prototypes of AMC and Carrier blade

MicroTCA Summary for TWEPP

Ray Larsen

PICMG Standards Extensions

- Standards Activities
  - MTCA.4 & Guideline for Clocks, Gates & Triggers for ATCA, MicroTCA approved, published
  - Software WG on hold past year
    - lack of time from key contributors and lack of urgency from users
    - Now advanced in real applications, SW and FW architectures, guidelines, roadmaps will be revived

- SLAC Infrastructure
  - Continuing evaluation program
  - Crates, cooling, blockers (Schroff, Elma, Vadatech, PT)
  - MCH (NAT, Vadatech)
  - Processors (Several)
  - Timing (MRF EVR on Vadatech adapter in use, 2-Wide Timer from DESY-Stockholm under test)
  - Power Supplies (Telkoor, Wiener, Vadatech)
  - Application modules (Struck, Vadatech, TEWS, NAT etc.)

MRF: Mirco-Research, Finland
EVR: Event receiver

MTCA.4 Adopted for LCLS-II Injector & 4 Stations of Main Linac

- **Injector LLRF System**
  - Racks completely assembled with 4Ch LLRF control in single 12 slot MTCA.4 crate
    - 1 Ch Prototype system fully tested on-beam in 2012
    - Production 4Ch System plus Legacy support system completed in water-stabilized rack system
- **Injector BPM System**
  - BPM Crates (2) completed for 15 BPMs
    - 3 Ch Prototype system fully tested on beam early 2013
    - 15Ch 2-Crate System completed in dual water-cooled rack system
    - Resolution 3X improved over Legacy 1U Chassis

LLRF Crate in Dual Rack

4Ch LLRF Crate

BPM Crate 8Ch Digitizers

BPM Crate 8Ch RTMs

Future Planning

- MTCA.4 candidate to replace all CAMAC
  - Upgrade of all SLAC controls proposed to DoE
  - Scope includes all RF stations, BPMs, Beam Charge Monitors, Beam Size Monitors, Wire Scanners, Movers, Machine Protection Interlocks etc.
  - Upgrade in 3 10-sector stages over ten-years (~340 MTCA systems)
- Standards
  - SLAC will continue supporting lab-industry xTCA collaboration, standards and guidelines
- Lab & Industry Collaborations
  - Will continue collaborations underway with DESY, Lund, Pohang, others in discussion in areas of LLRF, BPMs, Timing systems and with supporting companies for infrastructure, applications modules

For your agenda

Deadlines:
Abstract submission: 20 October
Registration: 22 November