Contribution ID: **164** Type: **Oral**

An optical data transmission ASIC for the ATLAS liquid argon calorimeter upgrade

Thursday 26 September 2013 10:15 (25 minutes)

We present several ASICs of optical data transmission for the ATLAS liquid argon calorimeter trigger upgrade. These ASICs include a two-channel serializer (LOCs2), a single-channel and a four-channel VCSEL driver (LOCld1 and LOCld4), each channel operating at 8 Gbps. The serializer ASIC implements a low-latency, low-overhead, quick-resynchronization interface chip (LOCic) between ADCs and serializers. These ASICs are designed and fabricated in a commercial 0.25-μm silicon-on-sapphire (SoS) CMOS technology, which is suitable for high energy physics front-end electronics applications. The designs and test results will be presented.

Summary

The ATLAS liquid argon calorimeter trigger upgrade requires high-speed, low-power and low-latency data transmission. The commercial serializer and laser driver do not work in the front-end radiation environment. Based on a commercial radiation-tolerant 0.25-um SoS CMOS process, we have designed high-speed serializer and laser driver ASICs for the ATLAS ATLAS liquid argon calorimeter trigger upgrade.

LOCs2 is a two-channel serializer, each channel operating at 8-Gbps.LOCs2 consists of two 16:1 serializer channels. Each channel has a 16-bit parallel data input in LVDS logic and a serial data output in CML logic. The two channels share an LC-tank-based phased-locked loop (LC-PLL), which has been prototyped and tested. The tuning range of the LC-PLL has been slightly modified to match to the speed requirement of the serializer. The PLL loop bandwidth is programmable from 1.3 to 7.0 MHz. Post-layout simulations indicate that the deterministic jitter is about 15 ps (peak-to-peak) at 8 Gbps at nominal process corner and room temperature. The random jitter has been verified to be about 1.4 ps in previous prototype chip. The power consumption of LOCs2 is estimated to be 1.2 W. The first version was submitted in June, 2012. A bug in the divider chain of the PLL was found in the test. The second version was submitted in February, 2013. More test results of LOCs2 will be presented in the paper.

LOCs2 will implement a low-latency, low-overhead, quick-resynchronization interface chip (LOCic) between ADC and serializer. The data frame with 14% overhead provides 12-bit bunch crossing identification (BCID) information, fast resynchronization and strong error detection capability. The latency is less than 10 ns. LOCic is designed and will be submitted in October, 2013. It will be integrated into the serializer in the future. The firmware on the receiver side is implemented in an FPGA to verify the design logic and performance.

LOCld1 is a single-channel VCSEL driver and will be used in a low footprint dual-channel optical transmitter module called MTx. The LOCld1 core analog circuit has been tested with previous prototype chip. When LOCld1 drives a VCSEL, the total jitter is 30-ps at the bit error rate of 1E-12 and the optical modulation amplitude is -1.3 dBm at 8-Gbps and room temperature. The modulation current, biasing current and shunt-peaking strength is programmable via I2C. To immune from the single event upsets (SEU), internal registers are protected with Triple Modular Redundancy (TMR). We adopt the HDL code of I2C module developed by CERN and slightly modified to adapt the foundry digital library.

LOCld4 is a four-channel VCSEL driver array to drive a four-channel VCSEL array with single-end outputs. LOCld4 or the future multiple-channel VCSEL driver array will be used in a VCSEL array based optical transmitter module. The test results of LOCld4 will be presented in the conference.

Primary author: LI, Xiaoting (Central China Normal University, Southern Methodist University)

Co-authors: Mr DENG, Bingwei (Hubei Polytechnic University, Huangshi, Hubei 435003, P. R. China); LIU, Chonghan (SMU); GONG, Datao (Southern Methodist Univeristy); GUO, Di (University of Science and Technology of China, Southern Methodist University); LIANG, Futian (University of Science and Technology of China); LIU, Gang (Institute of High Energy Physics, Beijing, P.R. China); JIN, Ge (Fachbereich Physik); HUANG, Guangming (Central China Normal University); LIANG, Hao (University of Science and Technology of China); YE, Jingbo (Southern Methodist University, Department of Physics); Mr CHEN, Jinghong (Southern Methodist University); TENG, Ping-Kun (Academia Sinica-Unknown-Unknown); Prof. HOU, Suen (Academia Sinica (TW)); LIU, Tiankuan (Southern Methodist University); ZHAO, Xiandong (Southern Methodist University); SUN, Xiangming (Lawrence Berkeley National Lab. (US), Central China Normal University); XIANG, annie (Southern Methodist University)

Presenter: LI, Xiaoting (Central China Normal University, Southern Methodist University)

Session Classification: Optoelectronics and Links

Track Classification: Opto