Continuous-Time Analog Filter Design in CMOS Nanoscale Era

Andrea Baschirotto[(1)], Marcello De Matteis[(1)], Alessandro Pezzotta[(1)], Stefano D'Amico[(2)]

[1] Dept. of Physics "G. Occhialini"
University of Milano-Bicocca
Milan – Italy

[2] Dept. of Innovation Engineering
University of Salento
Lecce – Italy

Continuous-Time Analog Filter Design in CMOS Nanoscale Era

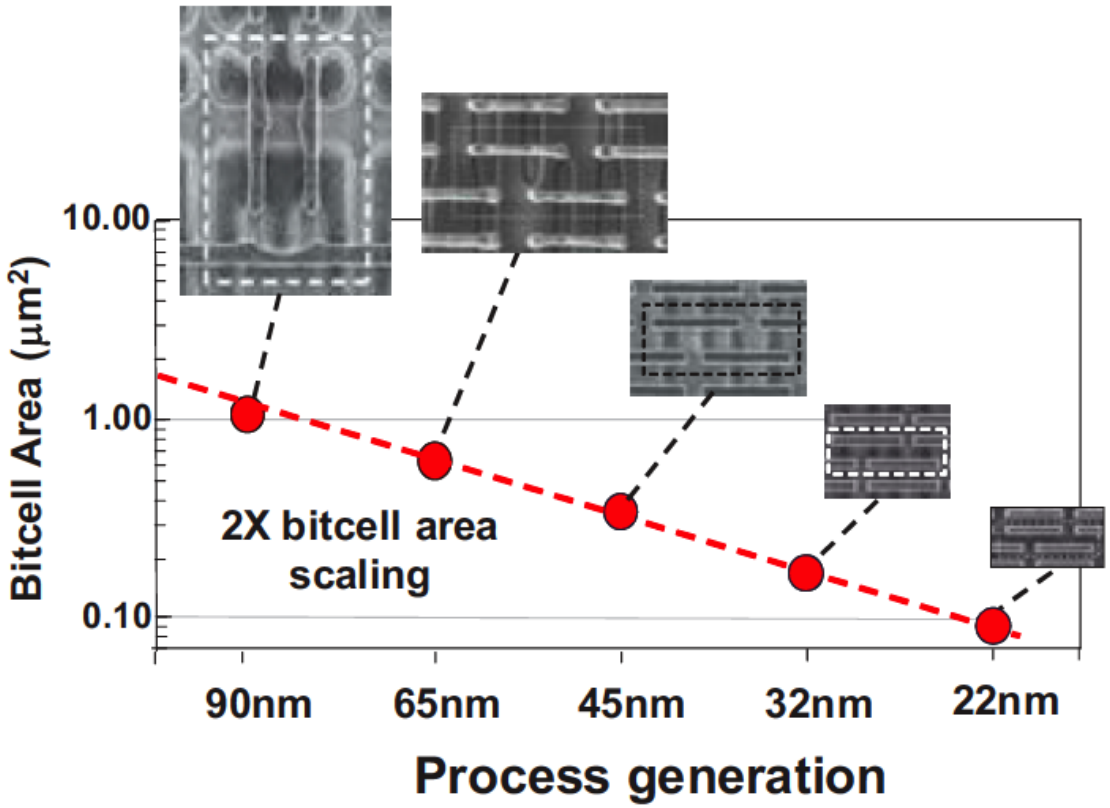
Outline

- Analog filter applications ←←←←
- Analog Design vs. CMOS Nanometer Technologies
- Analog filter recent developments
- Conclusions

Nanometer Technology

Outline

- **Digital circuits**
  - Smaller area
  - Lower power consumption
    - More circuit complexity and larger functionality

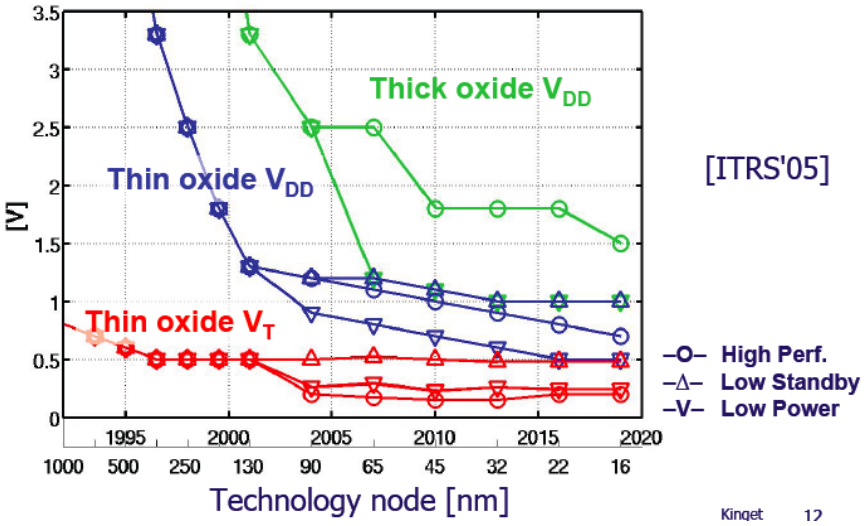


Nanometer Technology

Outline

- **Analog circuits**
  - Lower supply ➔ No cascode
  - Higher power for noise reduction ➔ Lower swing for the same SNR
  - Lower gain
  - Leakage current
  - Larger Threshold voltage variabity
    - STI, WPE

Node	Nm	250	180	130	90	65	⇓
L_{GATE}	Nm	180	130	92	63	43	
t_{OX}(inv.)	Nm	6.2	4.45	3.12	2.2	1.8	⇓
Peak g_m	µS/µm	335	500	720	1060	1400	⇑
g_{ds}**	µS/µm	22	40	65	100	230	⇑⇑
g_m/g_{ds}	-	15.2	12.5	11.1	10.6	6.1	⇓
V_{DD}	V	2.5	1.8	1.5	1.2	1	⇓⇓
V_{TH}	V	0.44	0.43	0.34	0.36	0.24	⇓
f_T	GHz	35	53	94	140	210*	⇑⇑



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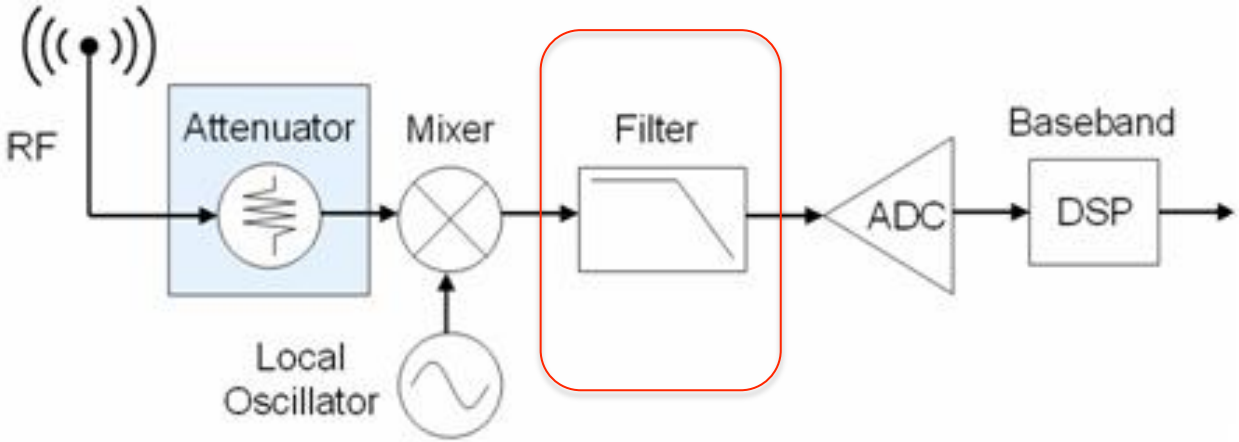
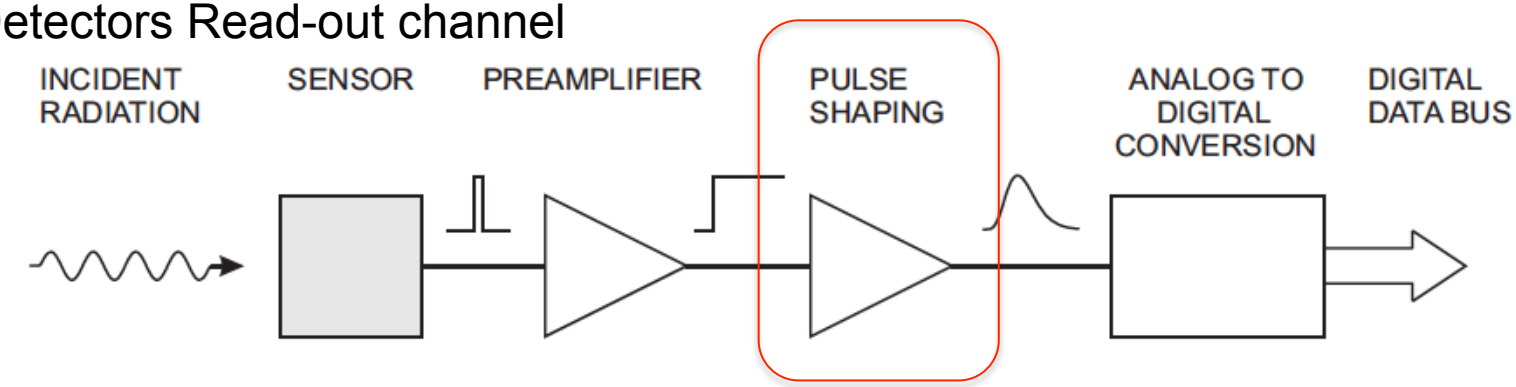
Outline

Analog filter applications

- Analog filters are key blocks in analog signal processing
  - Telecom transceiver



  - Detectors Read-out channel



Outline

Analog filter applications

- Analog filters are typically required to perform:
  - Low-voltage operation (<1V)
    - Bias
    - Bias vs. Signal amplitude
  - High-speed
    - Large bandwidth (≈2GHz)
    - Small time-of-response
  - Large linearity
    - THD (<60dB @ 500mVpp)
    - Linear range
  - Low-noise
    - PSD (<5nV/√Hz)
- Lowpass filters are considered
  - Bandpass could be considered too

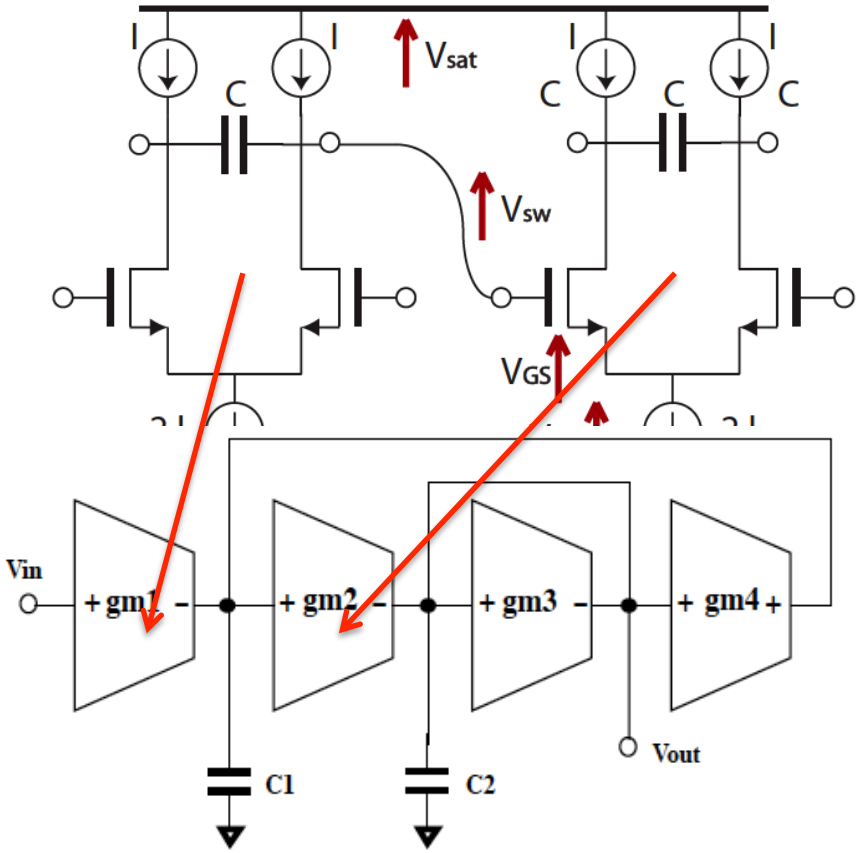
g_m-C Filters
Pros & Cons

- g_m-C filters features
  - Open-loop structure (MOS-based)
    - ***Transconductor problems***
      - Parasitic cap sensitivity
      - Lower linearity (***No Rail-to-rail***)
        - **Linearity ≈ V_{ov}**
      - Larger bandwidth
        - $g_m \approx 2 \cdot I/V_{ov}$

$$gm = \frac{I}{Vov}$$

$$Bandwidth = \frac{Power}{Linearity}$$

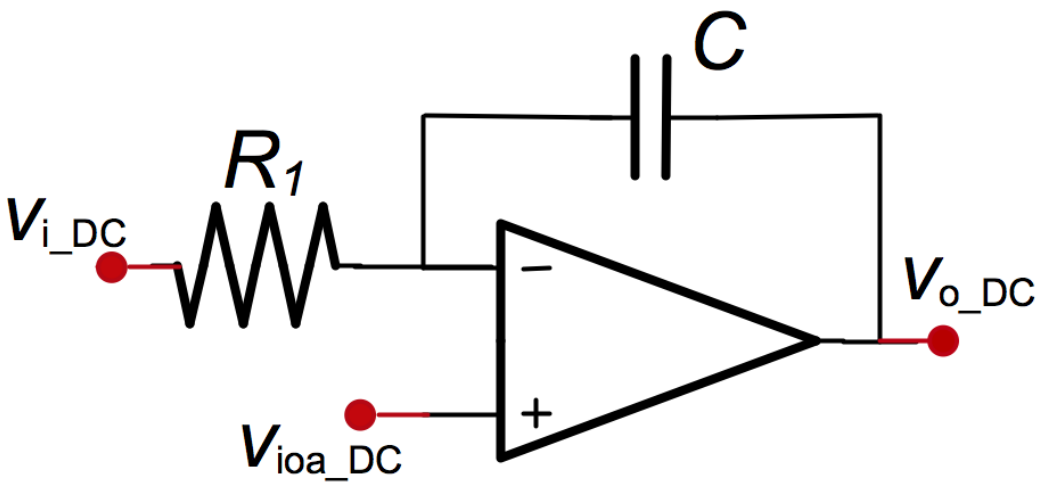
    - ***Biquad cell problem***
      - One branch per-transconductor
        - Four transconductors per-biquad



Active-RC Filters

Pros & Cons

- Active-RC filters features
  - Closed-loop structure
    - Smaller bandwidth
      - UGB spec ➔ $\mathbf{UGB_{opamp} > 50 \cdot f_{cut\text{-}off}}$
    - Parasitic cap **IN**sensitivity
    - Larger linearity (***Rail-to-rail***)
      - Critical DC-bias @ LV



Continuous-Time Analog Filter Design in CMOS Nanoscale Era

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Continuous-Time Analog Filter Design in CMOS Nanoscale Era

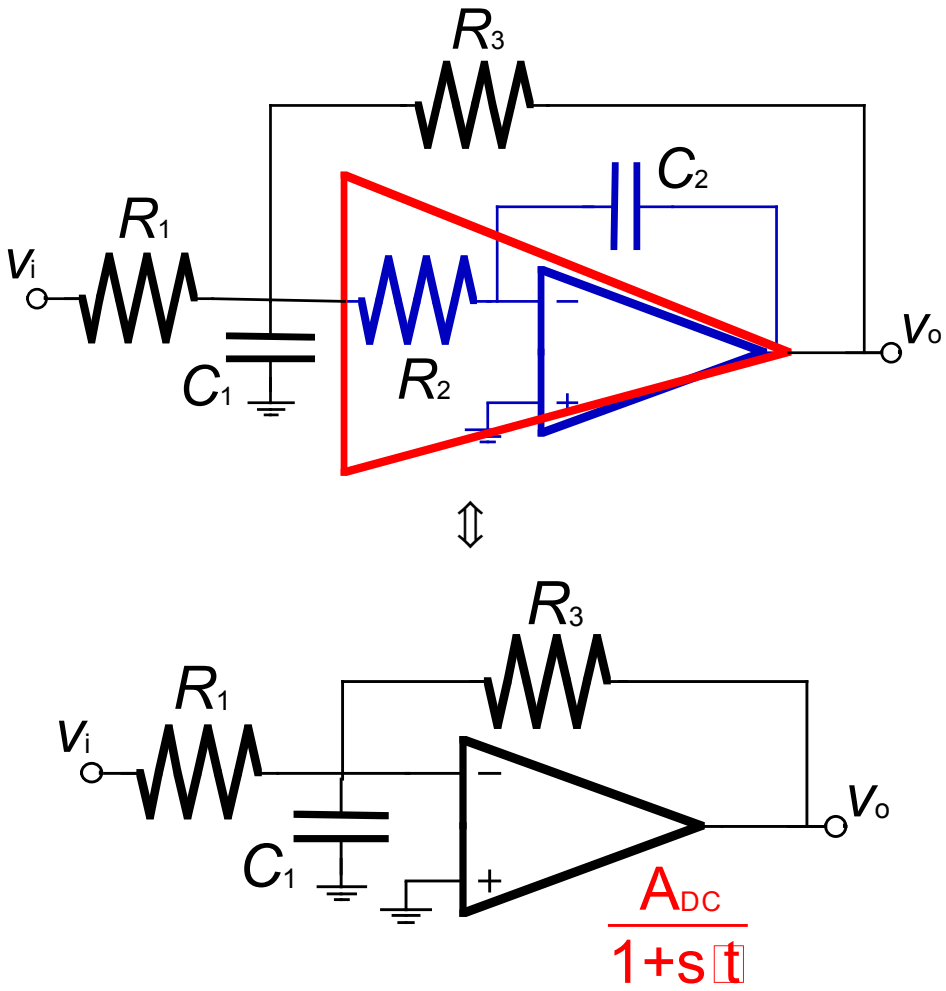
Advanced Filter solutions

- Advanced technologies & Advanced Application
  - No optimum filter
  - Advanced custom filter design
    - ***Large signal*** processing ➔ ***Closed-loop*** ➔ Active-RC
      - UGB spec reduction ➔ Active-g_m-RC
      - LV ➔ Current-based level-shift
      - Noise reduction (➔ DR increase) ➔ IFLF
      - Bandwidth increase ➔ Current-feedback
      - Bandwidth increase ➔ Advanced source-follower
    - ***Small signal*** processing ➔ ***Open loop*** ➔ g_m-C
      - Power reduction ➔ Source-follower based
      - ➔ Diode-C

Active-RC filters: UGB spec reduction

From the Rauch Cell to the *Active-Gm-RC* Cell

- The Low-Pass Cell



- R_2-C_2 ➔ integrator in the frequency range of interest
- ➔ replaced by a bandwidth-controlled opamp

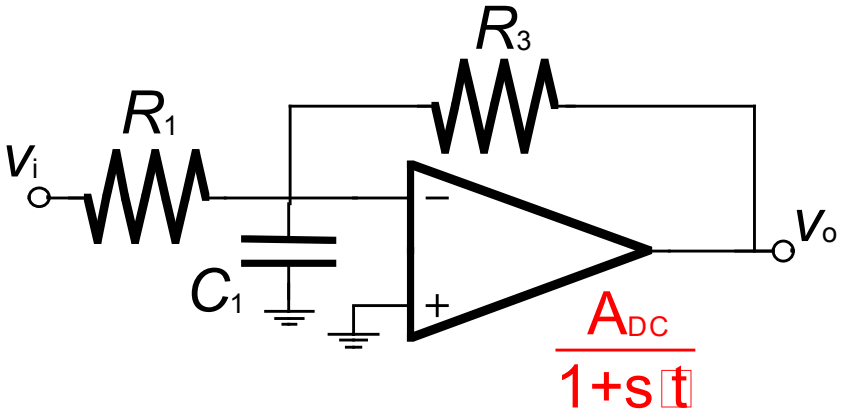
$$A(s) = \frac{A_{DC}}{1 + s \cdot \tau} = \frac{\omega_u \cdot \tau}{1 + s \cdot \tau}$$

- $1/\tau$ is the 1st-pole angular frequency
- A_{DC} is the DC-gain
- Unity gain angular frequency:

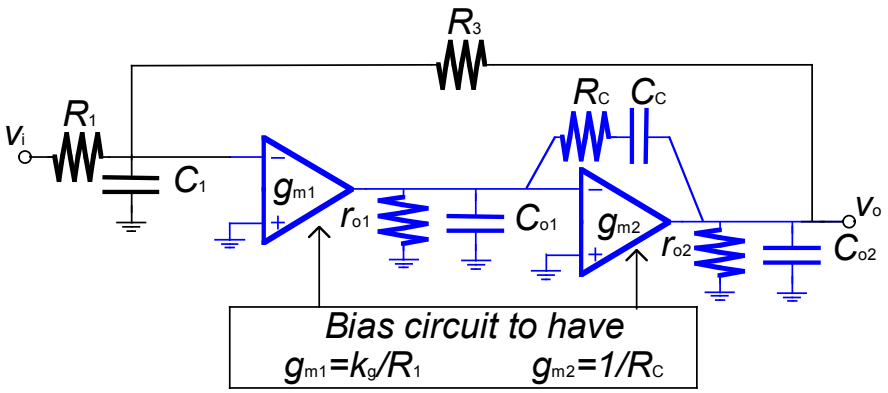
$$\omega_u = \frac{A_{DC}}{\tau}$$

Active-Gm-RC Filters

The Low-Pass Cell



Miller opamp



$$A_{DC} = g_{m1} \cdot R_{o1} \cdot g_{m2} \cdot R_{o2}$$

- The adjusting circuit sets

$$g_{m1} = 1/\left(k_g \cdot R_1\right)$$

dependence on the opamp frequency response parameters (g_{m1}, & C_C) ➔ dependence on parasitic component values (R_1, R_2 , & C_1)

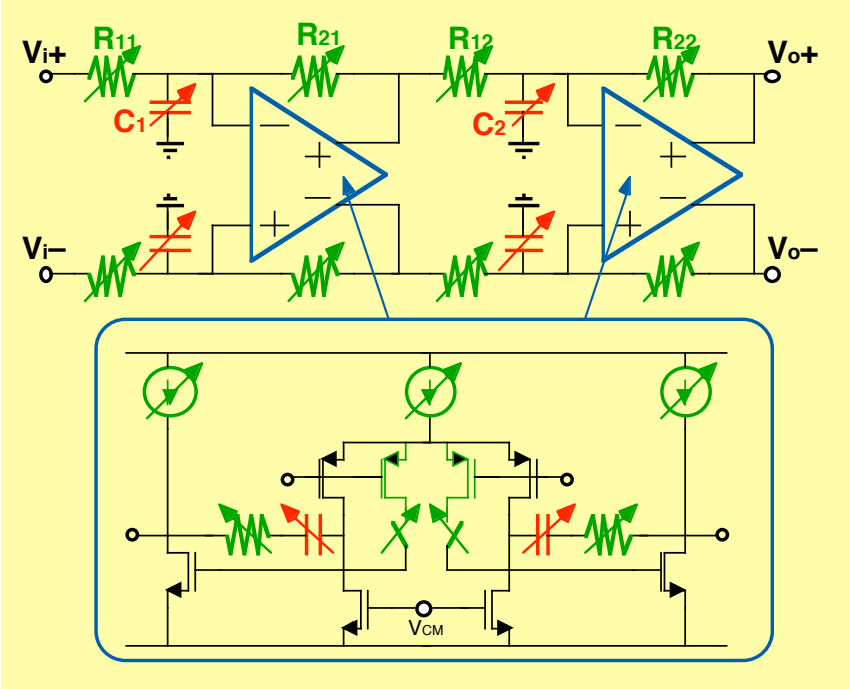
Active-Gm-RC Filters

The Low-Pass Cell

- 4th-order UMTS&WLAN reconfigurable filter

	UMTS		WLAN	
	1st cell	2nd cell	1st cell	2nd cell
$f_{cut\text{-}off}$ [MHz]	3.39	3.02	19.27	17.19
Q	0.806	0.522	0.806	0.522
k	1.26	1.26	1.26	1.26
UGB_{opamp} [MHz]	6.17	3.56	35.08	20.27
$UGB_{opamp}/f_{cut\text{-}off}$	**1.82**	**1.18**	**1.82**	**1.18**

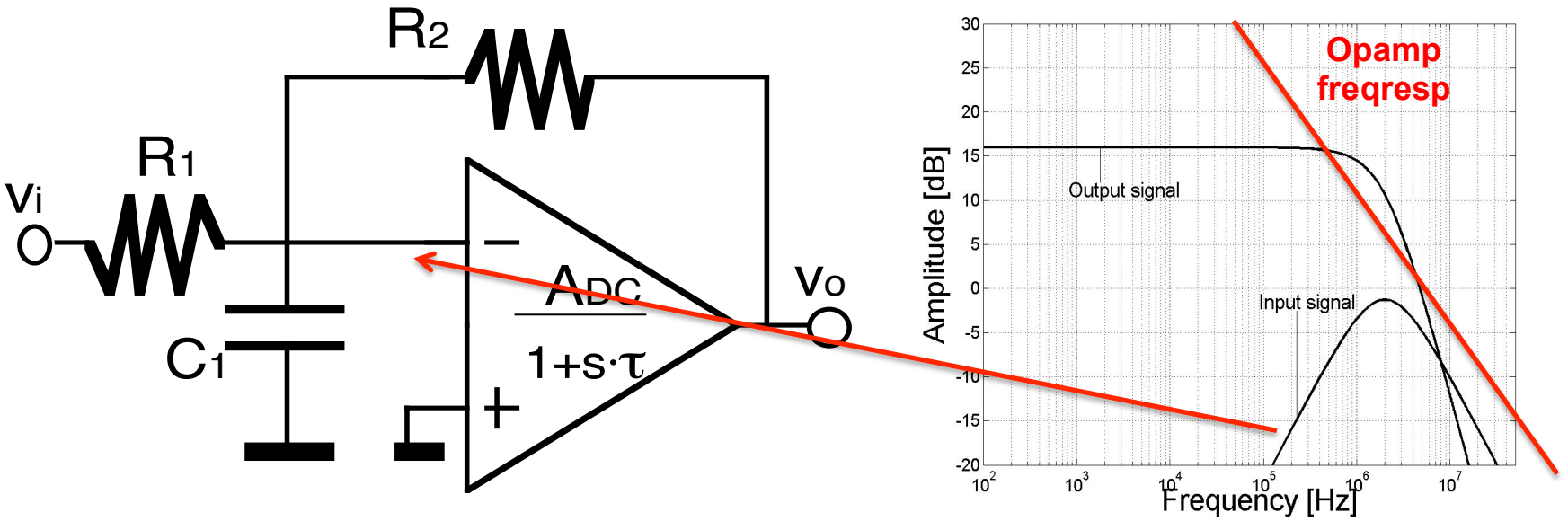
- Active-g_m-RC
  - ➔ $UGB_{opamp} \approx f_{cut\text{-}off}$
- Active-RC
  - ➔ $UGB_{opamp} \approx 50 \cdot f_{cut\text{-}off}$



Active-Gm-RC Filters

In-band & Out-of-band Linearity

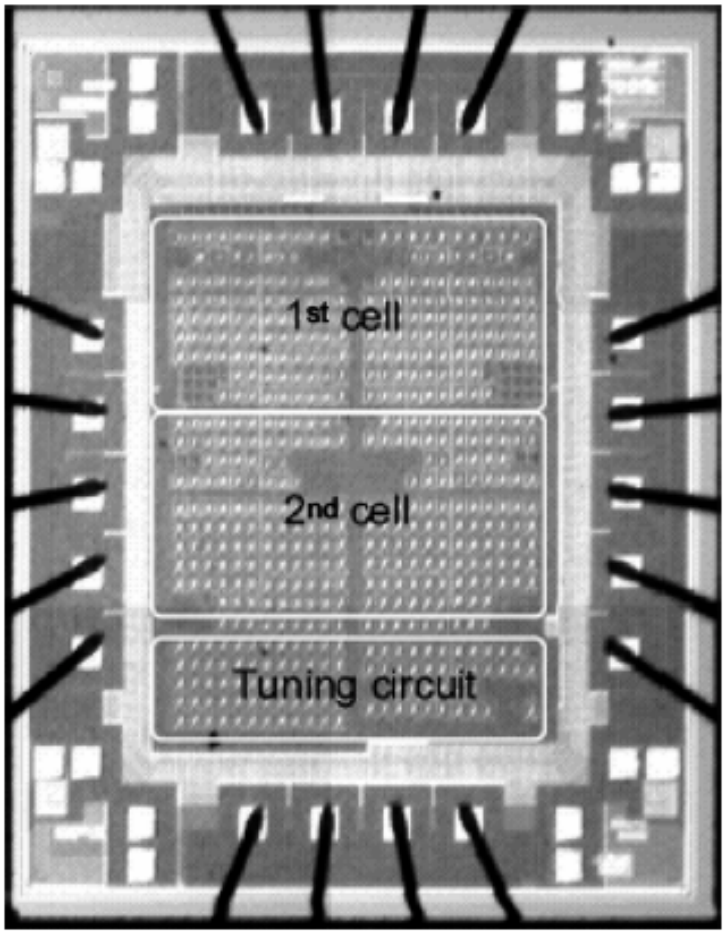
- Large linear range
  - In-band Signals
    - The closed loop operation guarantees large linearity
  - Out-of-band Signals
    - The larger signal part is processed by passive linear elements (R_1, R_2 and C_1)
    - The smaller part is processed by the non-linear opamp stages



Active-Gm-RC Filters

Experimental results (130nm)

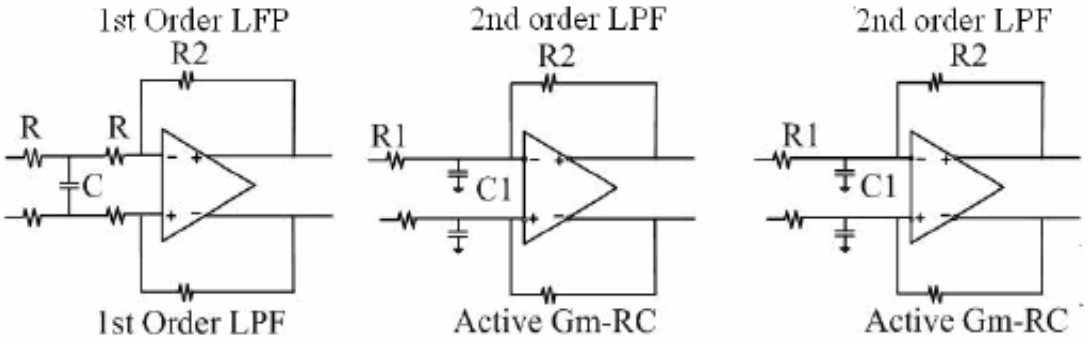
	UMTS	WLAN
Technology	0.13µm CMOS	
Supply voltage	1.2V	
Die area occupation	0.9mm^2	
Transfer function	4th order Bessel	4th order Bessel
f_{-3dB}	2.11MHz	11MHz
f_{-3dB} Programmable Range	[1.45-3.6] MHz	[5.87-19.44] MHz
Max f_{-3dB} deviation	5%	
DC-gain	4dB	4dB
Input-referred noise	36µV_{rms}	36µV_{rms}
In-band IIP3	21dBm	21dBm
DR(@THD=-40dB)	81dB	81dB
Out-of-band IIP3	31dBm	n.a.
Power consumption	3.4mW	14.2mW



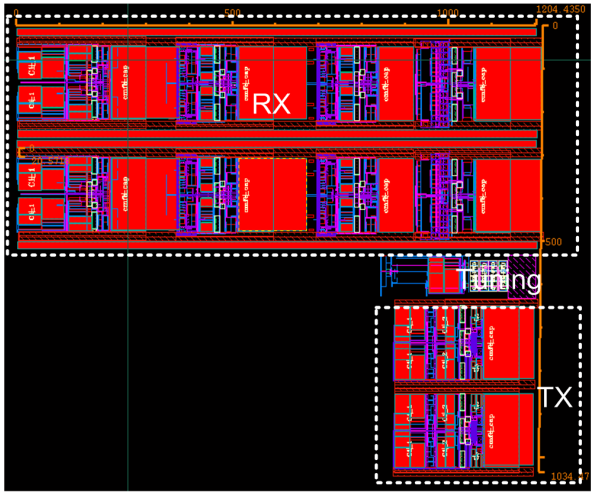
Active-Gm-RC Filters

Large-bandwidth implementation – UWB standard (90nm) *

- 5th-order structure



	Cell1	Cell2 & Cell3	
Gain		0dB	15dB
Opamp f_u	2.9GHz	650MHz	2.15GHz
Opamp Cc	200fF	1.5pF	200fF
C1	3.3pF	0.6pF	0.4pF
R1	1.4kΩ	2.09kΩ	2.09kΩ
R2	7.9kΩ	2.09kΩ	11.7kΩ



Parameter	Simulation Results
Technology	90nmCMOS
VDD	1.2 V
Gmax	58.2dB
fo	255MHz
Attenuation@660MHz	-60dB
Group Delay	2.5ns

* Cito, PRIME 2008

LV Active-RC Filters

Bias Point Design

- Closed-loop structure ☹ Bias point vs. Swing

➔ ***Rail-to-rail swing***

$V_{o_DC} = V_{DD}/2$

➔ Cell DC-coupling

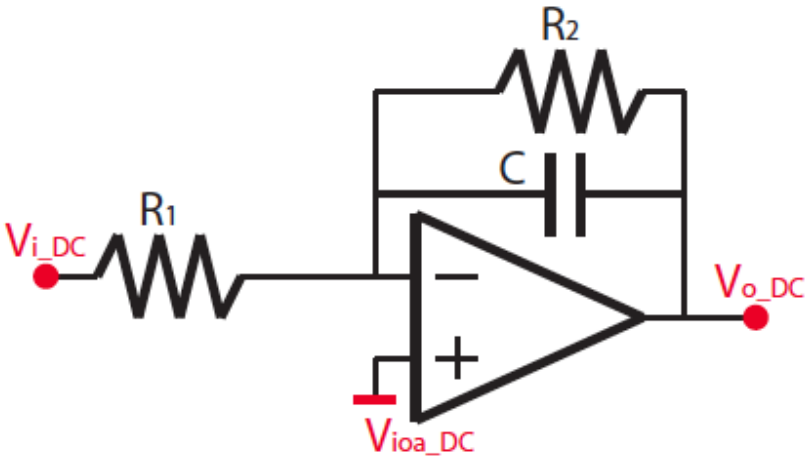
$V_{i_DC} = V_{o_DC} = V_{DD}/2$

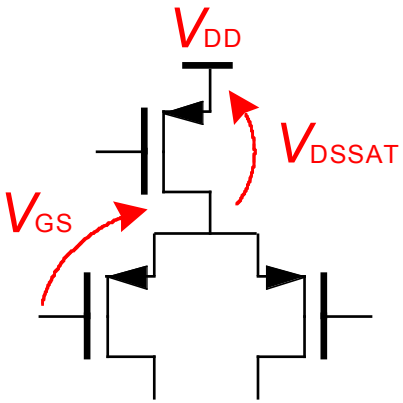
➔ DC-currents balance

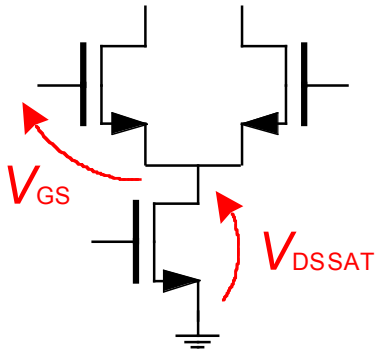
$V_{ioa_DC} = V_{i_DC} = V_{o_DC} = V_{DD}/2$

➔ PMOS input pair bias

$V_{ioa_DC} = V_{DD} - (V_{GS_inputpair} + V_{DSsat}) = V_{DD}/2$







➔ $V_{DDmin} = 2 \cdot V_{ioa_DC} = 2 \cdot (V_{GS_inputpair} + V_{DSsat})$

➔ $V_{DDmin} = 2 \cdot V_{TH} + 4 \cdot V_{ov}$

Current-based Level-shift Active-RC Filter

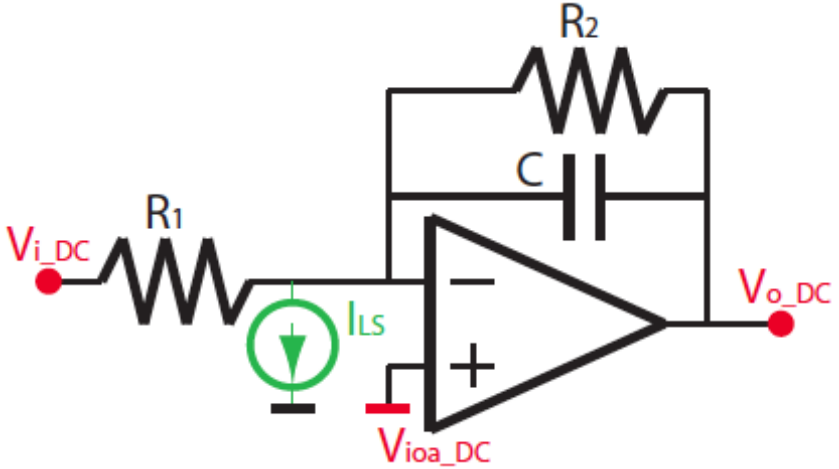
Bias Point Design

- I_1 reduces V_{DDmin}

$$I_{LS} = \frac{V_{i_DC} - V_{ioa_DC}}{R_1} + \frac{V_{o_DC} - V_{ioa_DC}}{R_3}$$

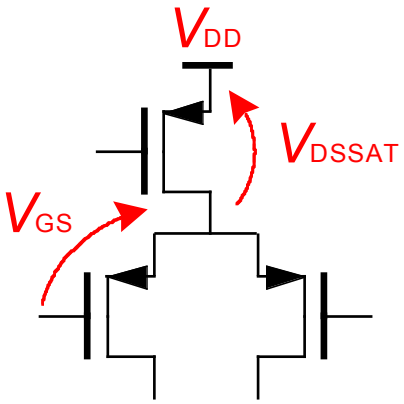
$$I_{LS} = \frac{V_{DD}/2 - V_{ov}}{R_1} + \frac{V_{DD}/2 - V_{ov}}{R_3}$$

$$I_{LS} = \left(V_{DD}/2 - V_{ov}\right) \cdot \left(\frac{1}{R_1} + \frac{1}{R_3}\right)$$



- ➔ $V_{DDmin} = V_{ov} + V_{GS_inputpair} + V_{DSsat}$

$$V_{DDmin} = V_{TH} + 3 \cdot V_{ov} \quad << 2 \cdot V_{TH} + 4 \cdot V_{ov}$$

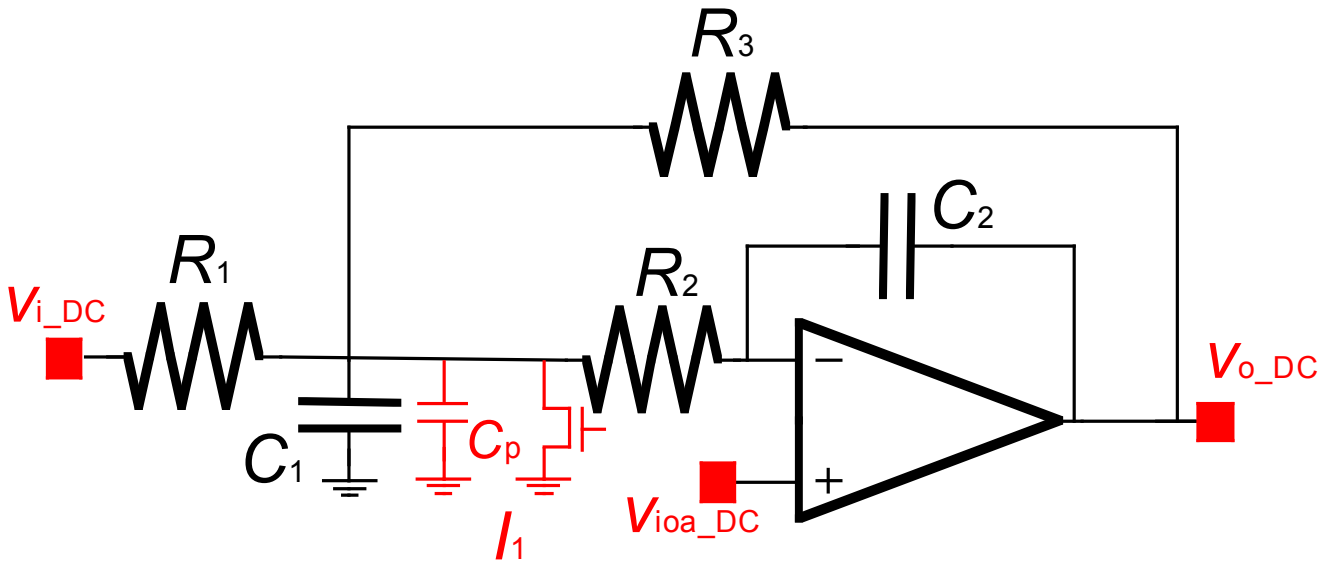


- Example:
  - V_{TH} = 0.35V
  - V_{ov}= 0.1 V
    - ➔ V_{DDmin} = 0.65V << 1.1V

Current-based Level-shift Active-RC Filter

LV Rauch Cell

$$V_{DDmin} = V_{TH} + 3 \cdot V_{ov}$$

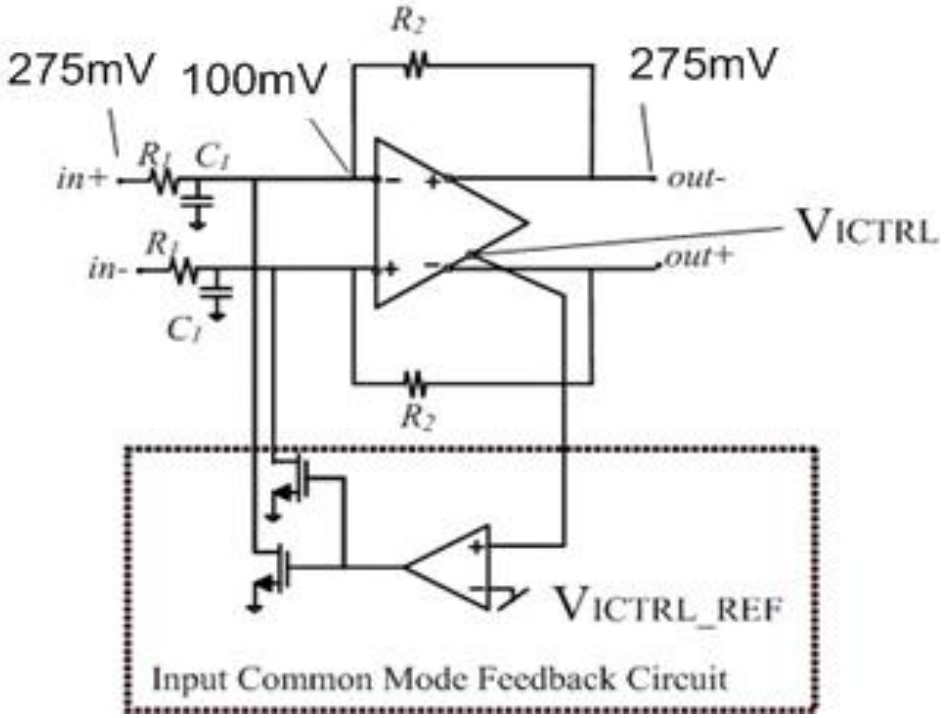


- Inserting I_{LS}
  - reduces V_{DDmin}
- BUT
  - Increases noises
  - Reduces DR !!
  - Increases parasitic capacitance sensitivity

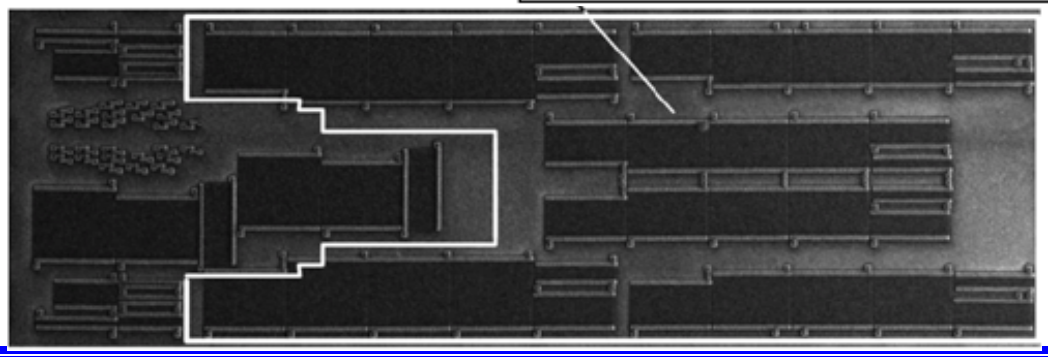
Current-based Level-shift Active-RC Filter

LV Active-g_m-RC (130nm) *

- WLAN Receivers baseband filter design
  - Control loop to adjust I_{LS} vs PVT variations



V_{DD} [V]	0.55
CMOS [µm]	0.13
V_{TH} [V]	0.3
Current Cons. [mA]	5.8
Power Cons. [mW]	3.5
Filter Order	4^{th}
G [dB]	0
f_{-3dB} [MHz]	11.3
In-band IIP3 [dBm]	10
Out-Band IIP3 [dBm]	13
1dBcP [dBm]	0.5
Noise [μV_{rms}]	110
DR[dB] - THD@40dBc	60
Area [mm^2]	0.43

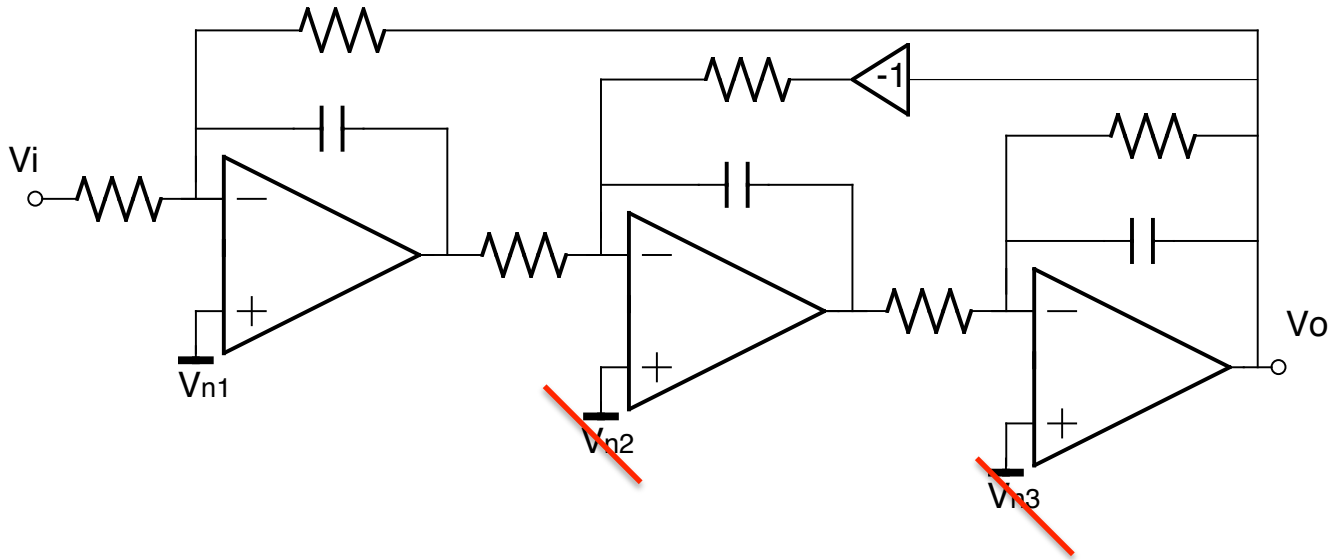


* De Matteis, ESSCIRC07

Low-Noise Active-RC Filter

Inverse-Follow-the-Leader-Feedback (IFLF)

- Low-noise solution



$$N_o = N_{opamp1} + N_{R1} + N_{R2}$$

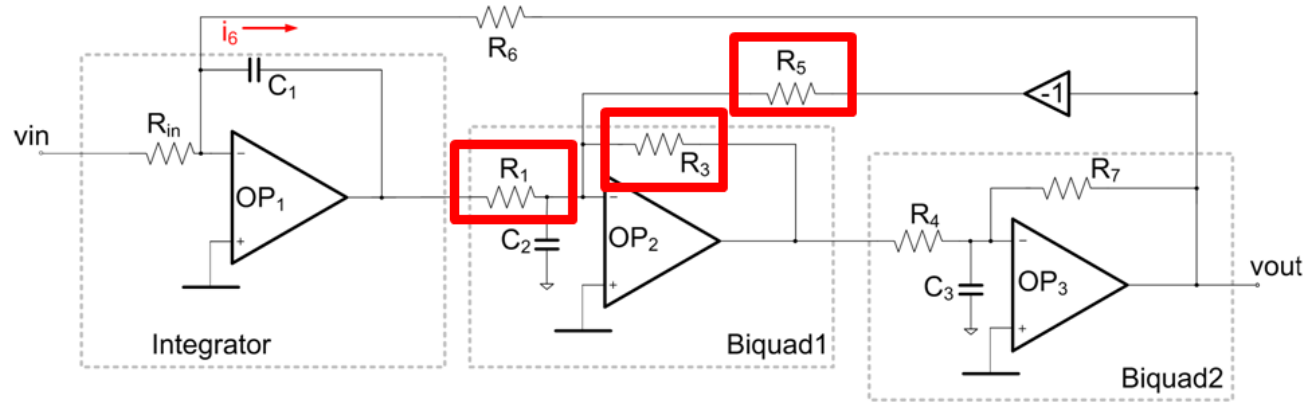
$$N_{opamp1} = N_{in} \cdot \left(1 + \frac{R_2}{R_1}\right)$$

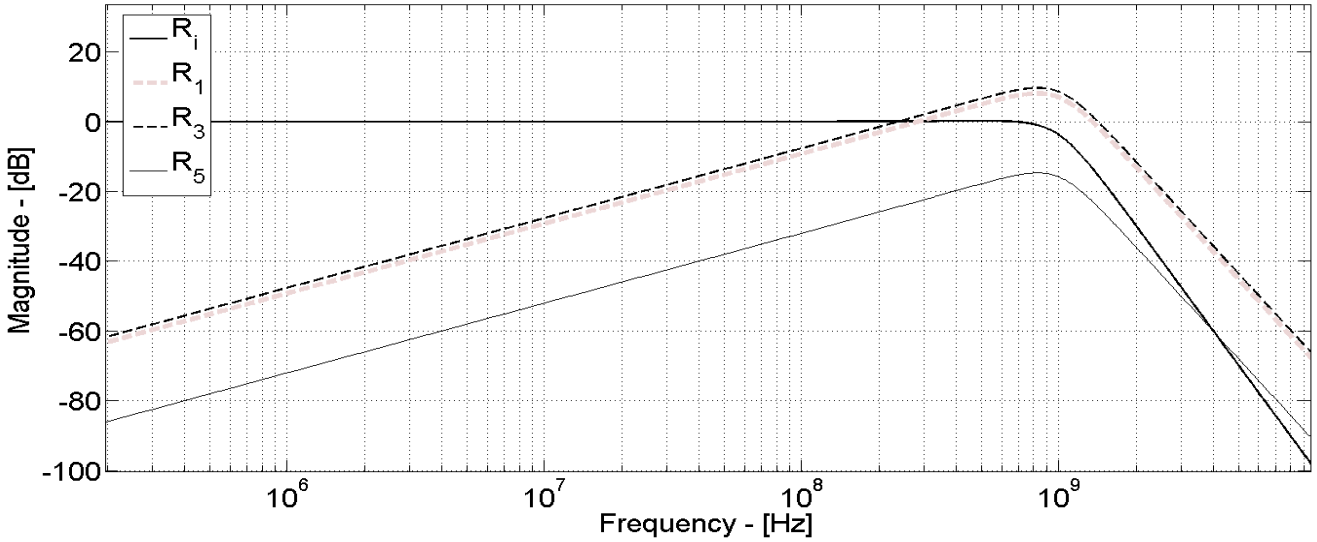
- **At low frequency** only the noise v_{n1} reaches the output node
  - V_{n2} & v_{n3} do not reach the output

Low-Noise Active-RC Filter

Advanced High-order IFLF

- IFLF architecture + Active-g_m-RC
  - Two internal biquad ➔ Active- g_m-RC
  - ➔ 3 Opamps for 5 poles





Low-Noise Active-RC Filter

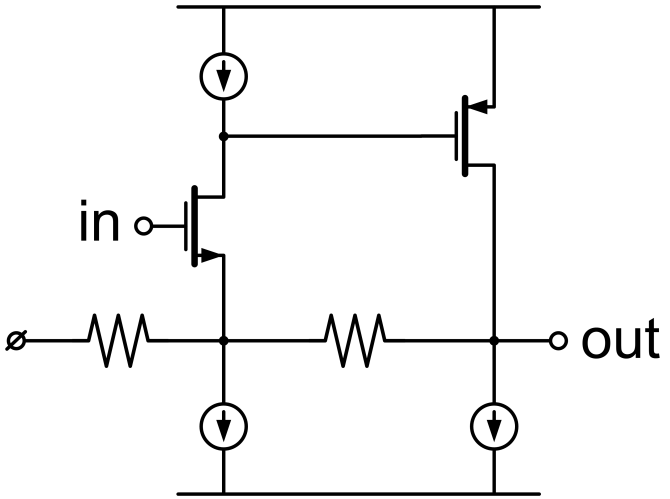
Advanced High-order IFLF (45nm)

Parameter	Value
G[dB]	0
$f_{@-3dB}$[MHz]	1.01GHz
avdd[V]	1.2
CMOS Technology	45nm
Power Consumption[mW]	9mW
Output Integrated Noise[μV_{rms}] - (100kHz÷1GHz)	500
IRN Spectral Density@100MHz [nV/√Hz]	12
THD[dBc] – v_{out}=0.45$V_{zero\text{-}peak}$@100MHz	40
SNR@THD=40dBc - [dB]	55

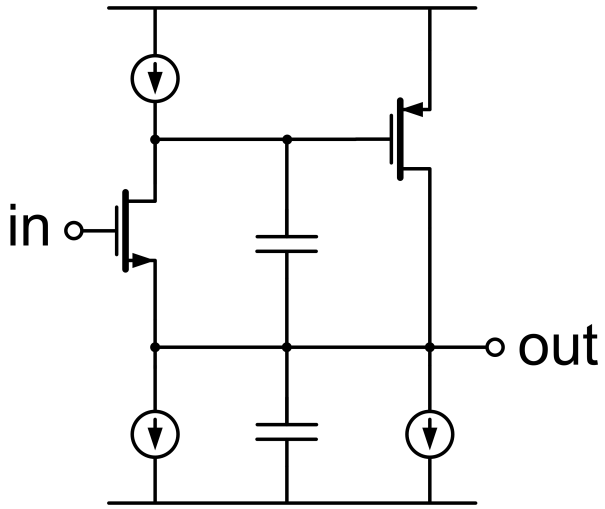
Filter Bandwidth Extension

Advanced Source-follower

- Source follower as:
  - VGA cell
    - 1st-order + Gain stage



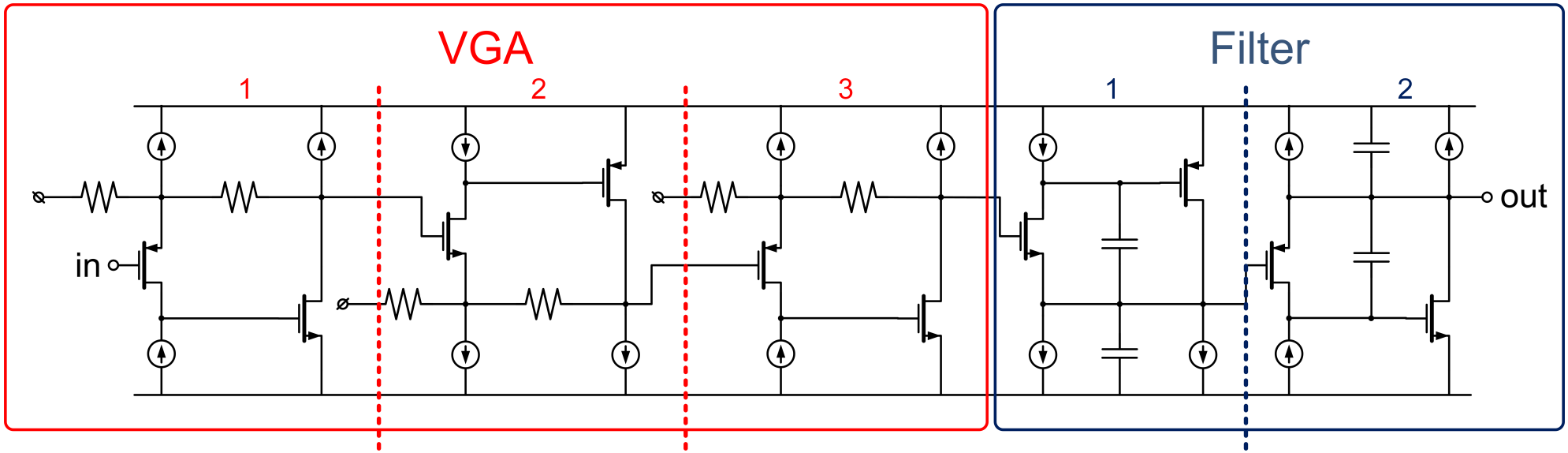
  - Biquad cell



Filter Bandwidth Extension

Advanced Source-follower

- 7^{th}-order filter
  - 3 VGA cells (3 poles)
  - 2 biquad cells (2 complex poles)



- Alternate P-type and N-type based cell for maintaining operating point

Filter Bandwidth Extension

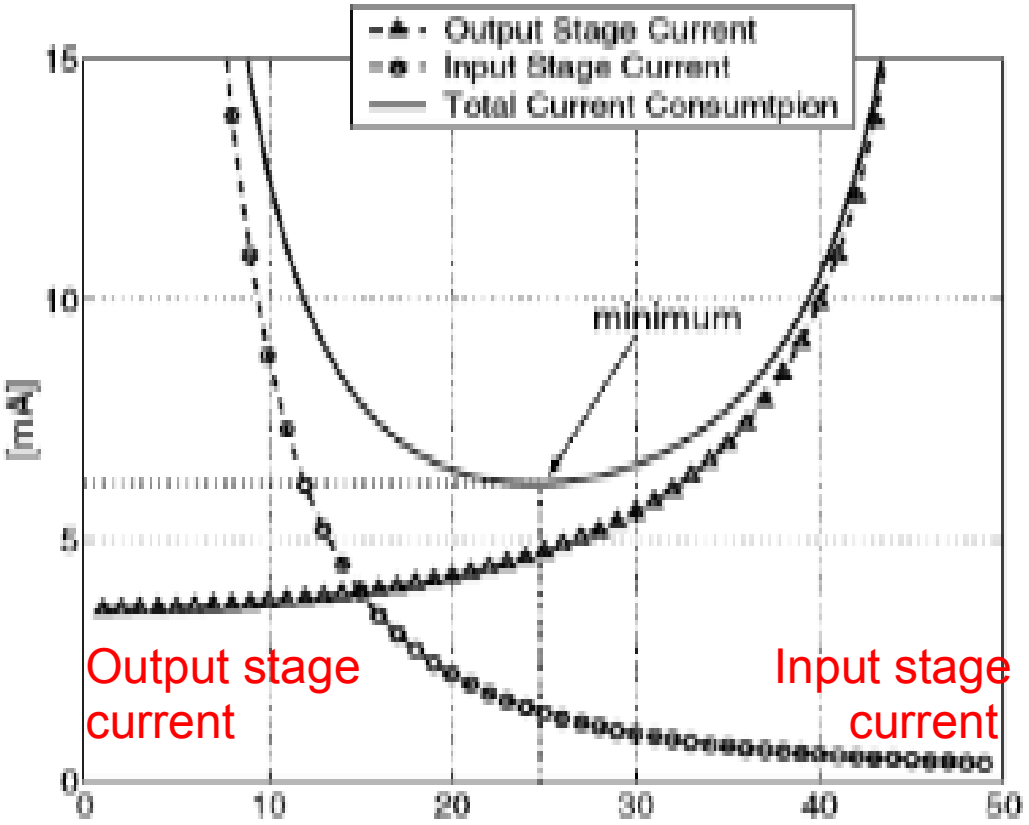
Advanced Source-follower - Global Performance (28nm)

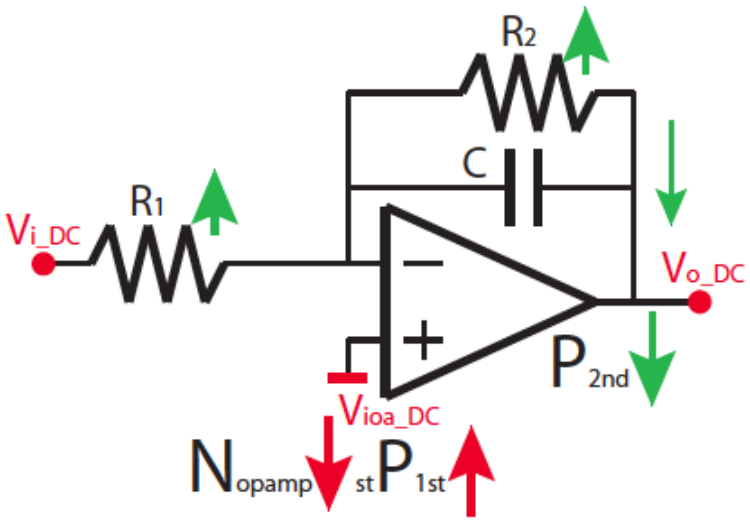
	CUT-OFF Freq=1.76GHz		CUT-OFF Freq=870MHz	
	DC-GAIN 5dB	**DC-GAIN 25dB**	**DC-GAIN 5dB**	**DC-GAIN 25dB**
Supply Voltage	1.1V	1.1V	1.1V	1.1V
-3dB Bandwidth	1.87GHz	1.81GHz	889MHz	868MHz
IRN	5.01nV/√Hz	5.07nV/√Hz	5nV/√Hz	4.7nV/√Hz
PN,OUT (In-Band Integrated Noise at the filter output, between 100kHz and 2GHz)	285μVrms	2.99mVrms	283μVrms	2.3mVrms
$V_{OUT,SWING}$@THD≥30dBc	$0.3V_{0\text{-}pk,diff}$ (THD=33dBc)	$0.28V_{0\text{-}pk,diff}$ (THD=31dBc)	$0.3V_{0\text{-}pk,diff}$ (THD=34dBc)	$0.2V_{0\text{-}pk,diff}$ (THD=31.5dBc)
SNR	57.13dB	36.5dB	57.4dB	35.77dB
Power	13mW	20mW	5mW	7mW
Output IP3 (1GHz&1.1GHz for 1.76GHz)	7dBm	2dBm	-	-

Active-RC Filters Optimum Design

Automatic Design Approach ? *

- Case-A: Dominant resistance noise
  - ➔ Opamp noise ⇓ ➔ Opamp input stage current ⇑
  - ➔ R ⇑ ➔ Opamp output stage current (driving R) ⇓





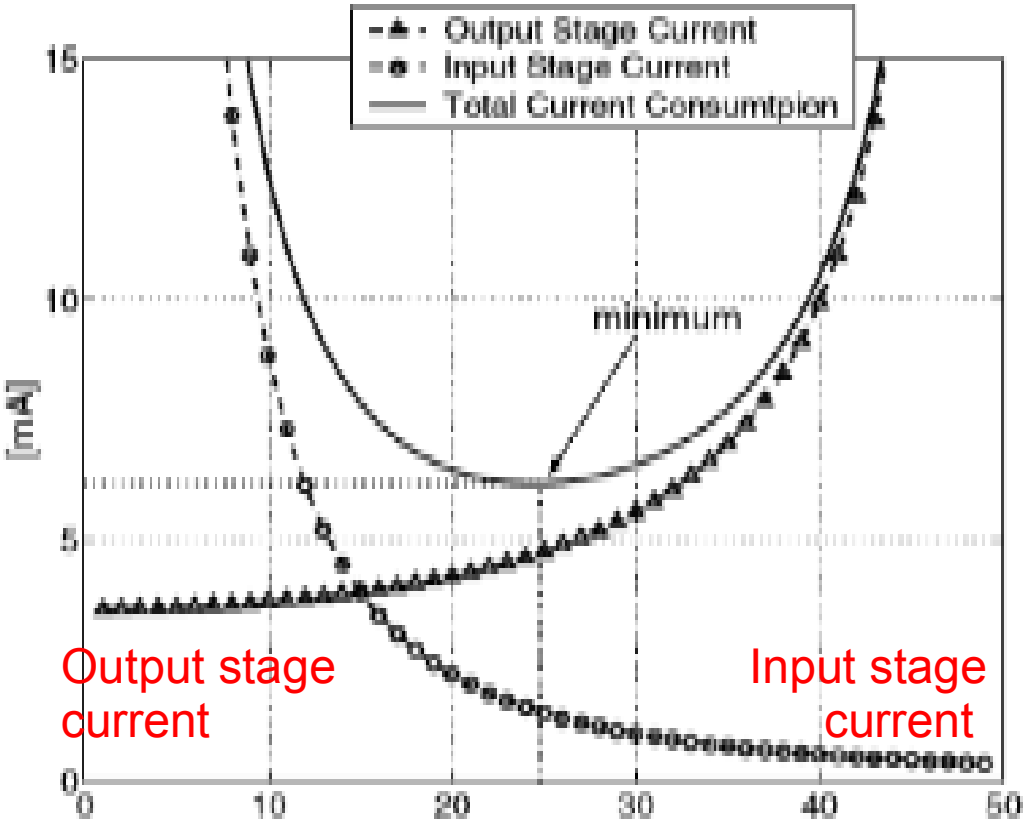
$$\alpha_N = \frac{IRN^2_{opamp}}{IRN^2_{cell}}$$

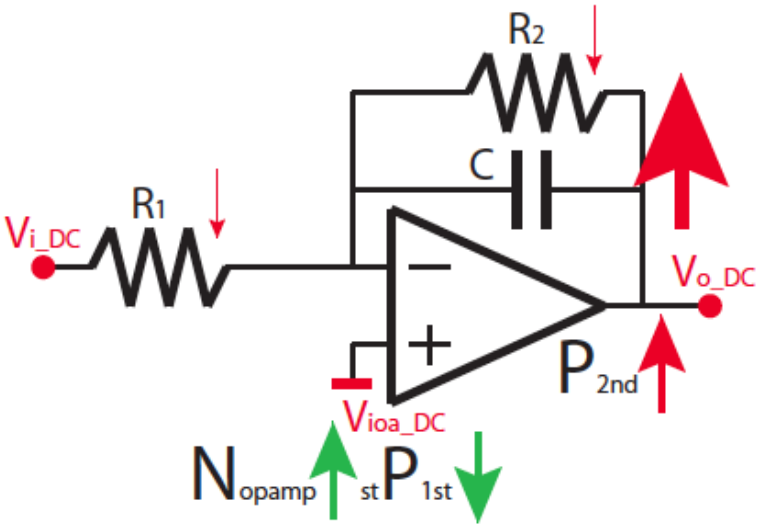
* De Matteis, IEEE PRIME 2006

Active-RC Filters Optimum Design

Automatic Design Approach ? *

- Case-B: Dominant opamp noise
  - ➔ Opamp noise ⇑ ➔ Opamp input stage current ⇓
  - ➔ R ⇓ ➔ Opamp output stage current (driving R) ⇑





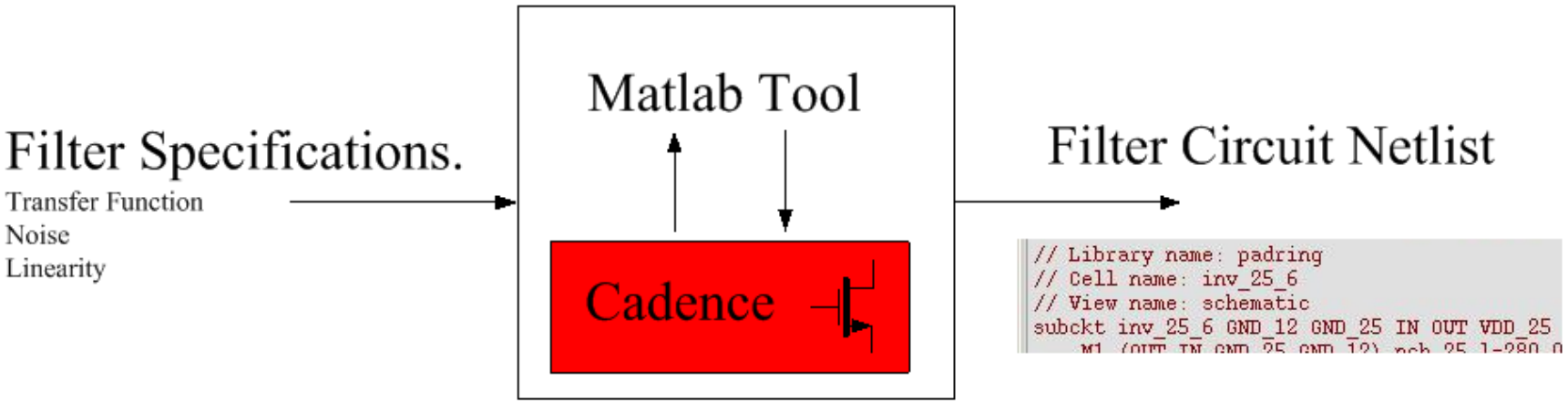
$$\alpha_N = \frac{IRN^2_{opamp}}{IRN^2_{cell}}$$

* De Matteis, IEEE PRIME 2006

Active-RC Filters Optimum Design

Automatic Design Approach ? *

- Linear design
  - Transfer function
  - Noise
    - Preliminary MATLAB routines
- Non-Linear design
  - THD
    - Iterative SPICE simulations

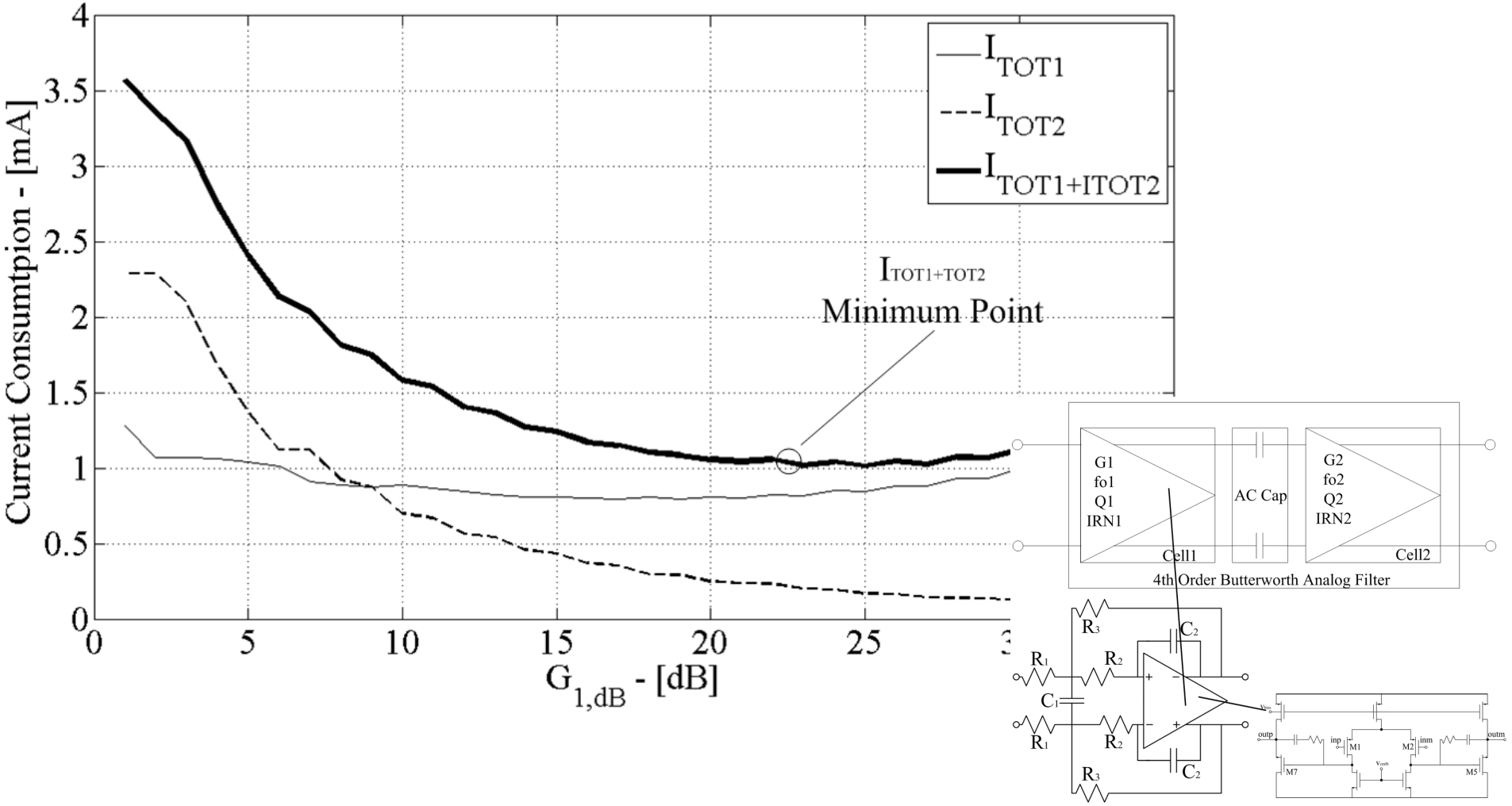


* De Matteis, IEEE PRIME 2006

Active-RC Filters Optimum Design

Automatic Design Approach - Cascade design *

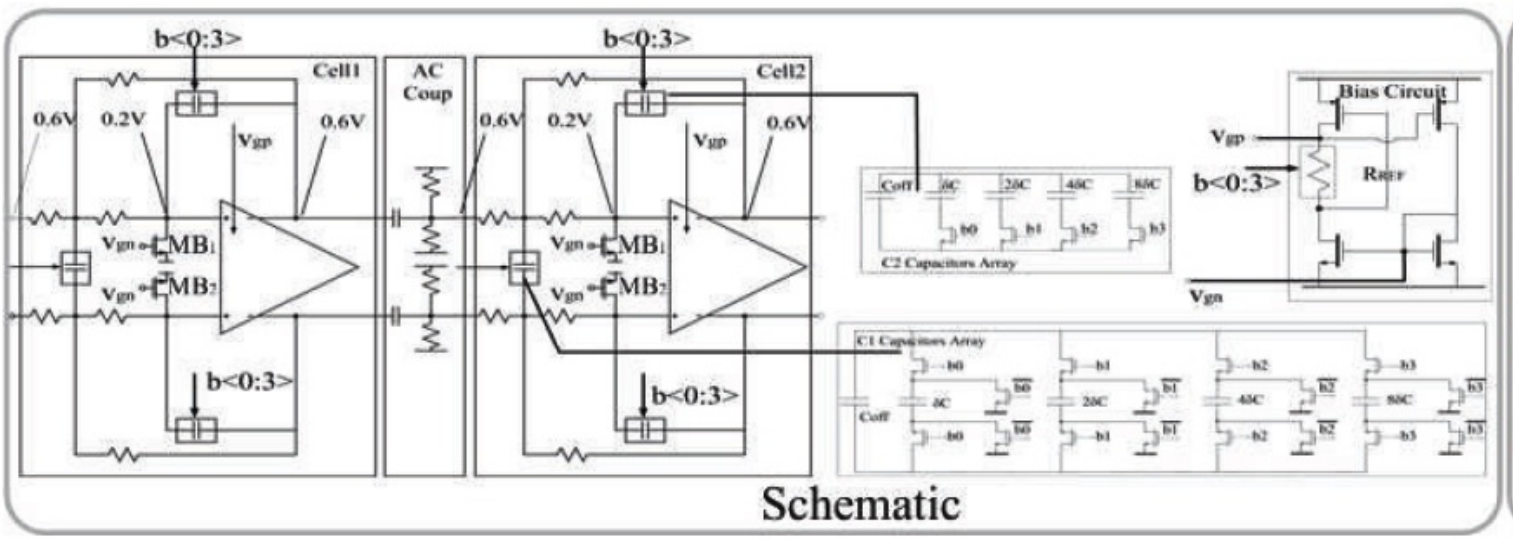
- Power minimization (4th-order filter ➔ 2-biquad cascade)
  - ➔ ***Cell sequence*** & ***gain*** amount optimization

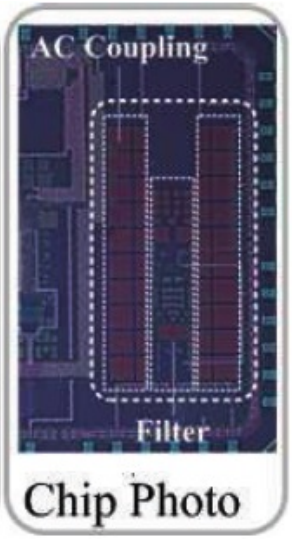


* De Matteis, ICECS 2009

Active-RC Filters Optimum Design

Automatic Design Approach (65nm) *





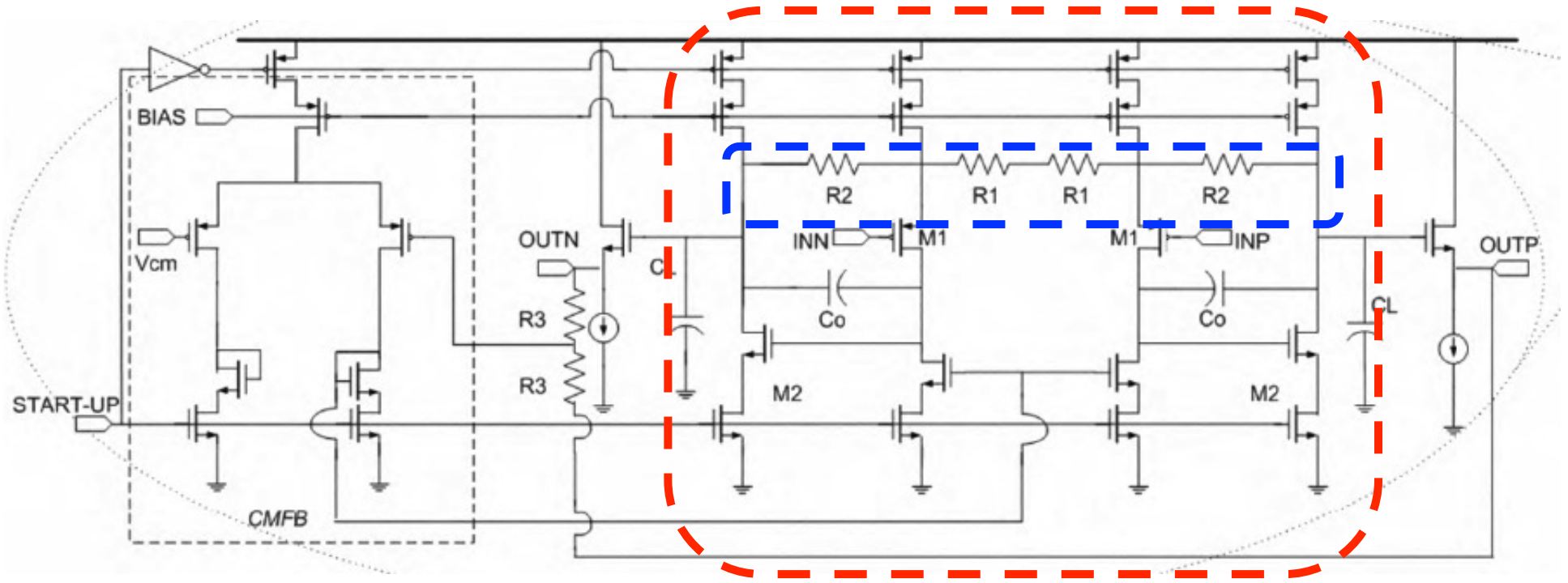
Parameter	Value
G[dB]	31
$f_{@-3dB}$[MHz]	8.2
V_{DD}[V]	1.2
CMOS Technology	65nm
Power Consumption[mW]	1.3
Output Integrated Noise[mV_{rms}] - (100kHz÷10MHz)	1.63
IRN Spectral Density@7MHz [nV/√Hz]	18
Output 1dBcP – [$V_{zero\text{-}peak}$]	0.9
THD[dBc] – v_{out}=1.05$V_{zero\text{-}peak}$@3MHz	40
DR@THD=40dBc - [dB]	52
IIP3 [dBm] $v_{in}=v_{in1}+v_{in2}$ - v_{in1}@2MHz, v_{in2}@3MHz	-10
OIP3 [dBm] $v_{in}=v_{in1}+v_{in2}$ - v_{in1}@2MHz, v_{in2}@3MHz	21.3

* De Matteis, AVLSI 2010

Shunt-feedback Filter

Filter & PGA

- Shunt feedback configuration
  - ☺ Wide band
  - ☺ Merge ***Filter & PGA*** functions
  - 2^{nd}-order transfer function

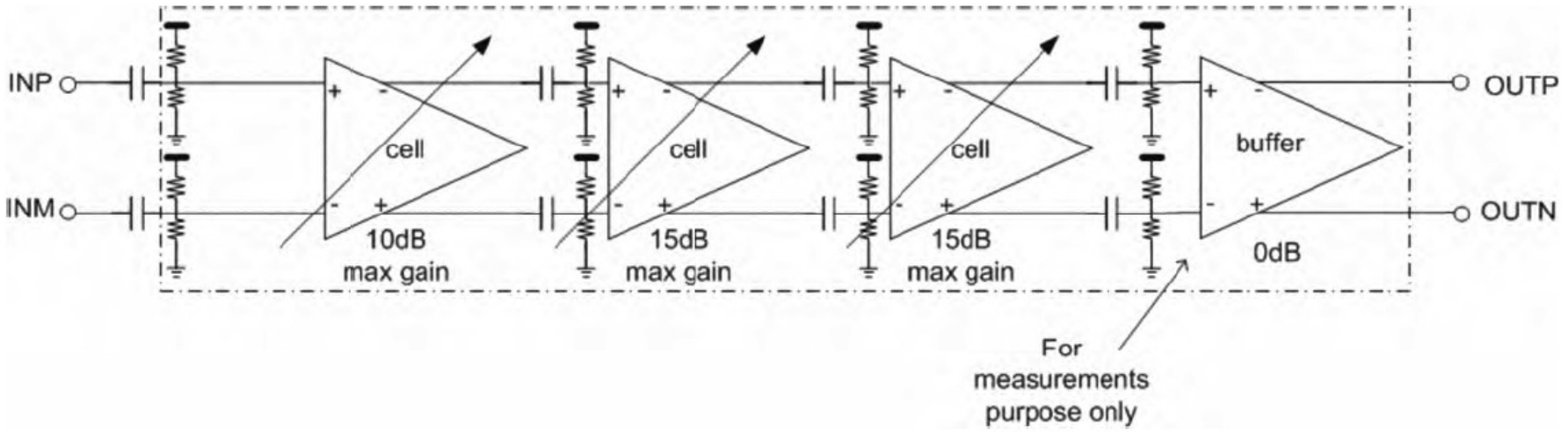


Shunt-feedback Filter

Filter & PGA

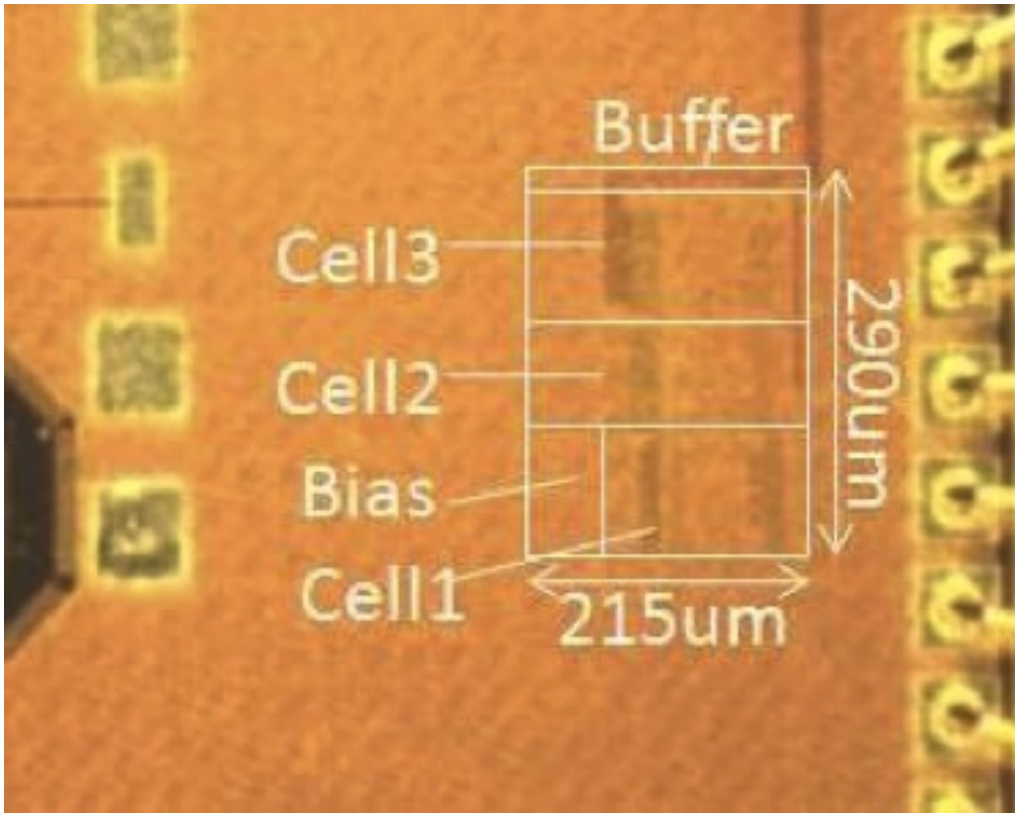
- Large gain programmability

  Gain up to 15dB-20dB per stage



Shunt-feedback Filter

Experimental results (90nm) *

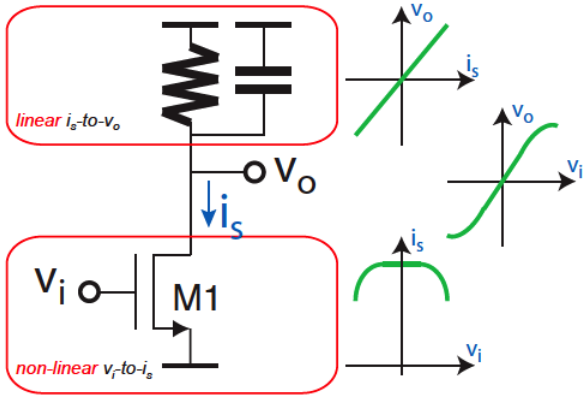


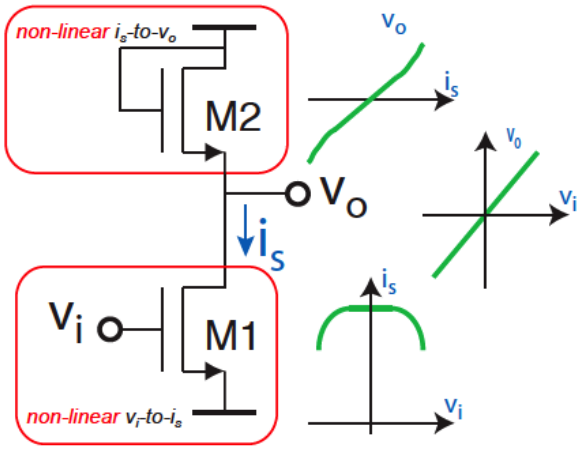
Technology	CMOS 90nm	
Power supply	1.2V	
Die size	290x215μm^2	
Input Referred Noise	4.6nV/√Hz @ 40dB gain	
Noise Figure	14.3dB @ 40dB gain	
Gain range	0-40dB	
Gain step	5dB ±1dB accuracy	
Bandwidth	240MHz	
Linearity	In-band 1dBcp=–44.8dBm PGA gain=40dB, f_{in}=50MHz	THD=–30dB PGA gain=40dB, f_{in}=80MHz, V_{out}=–6dBm
Current consumption	1.9mA (PGA gain =0dB) 2.9mA (PGA gain =40)	

* D'Amico, ESSCIRC2009, TCASI2012

g_m-g_m-C Filter
1st-order cell – Linearity

- Standard design approach
  - Assume linear output load
    - Linearize input driver
      - ➔ ☹ Larger V_{ov}
        - No LV
      - ➔ ☹ Larger power
- Alternative design approach
  - Assume non-linear input driver
    - Design non-linear output load to compensate input driver non-linearity
      - ➔ ☺ Smaller V_{ov}
        - Good for LV
      - ➔ ☺ Lower power
- ☹ Non-linearity compensation is valid for small linear range

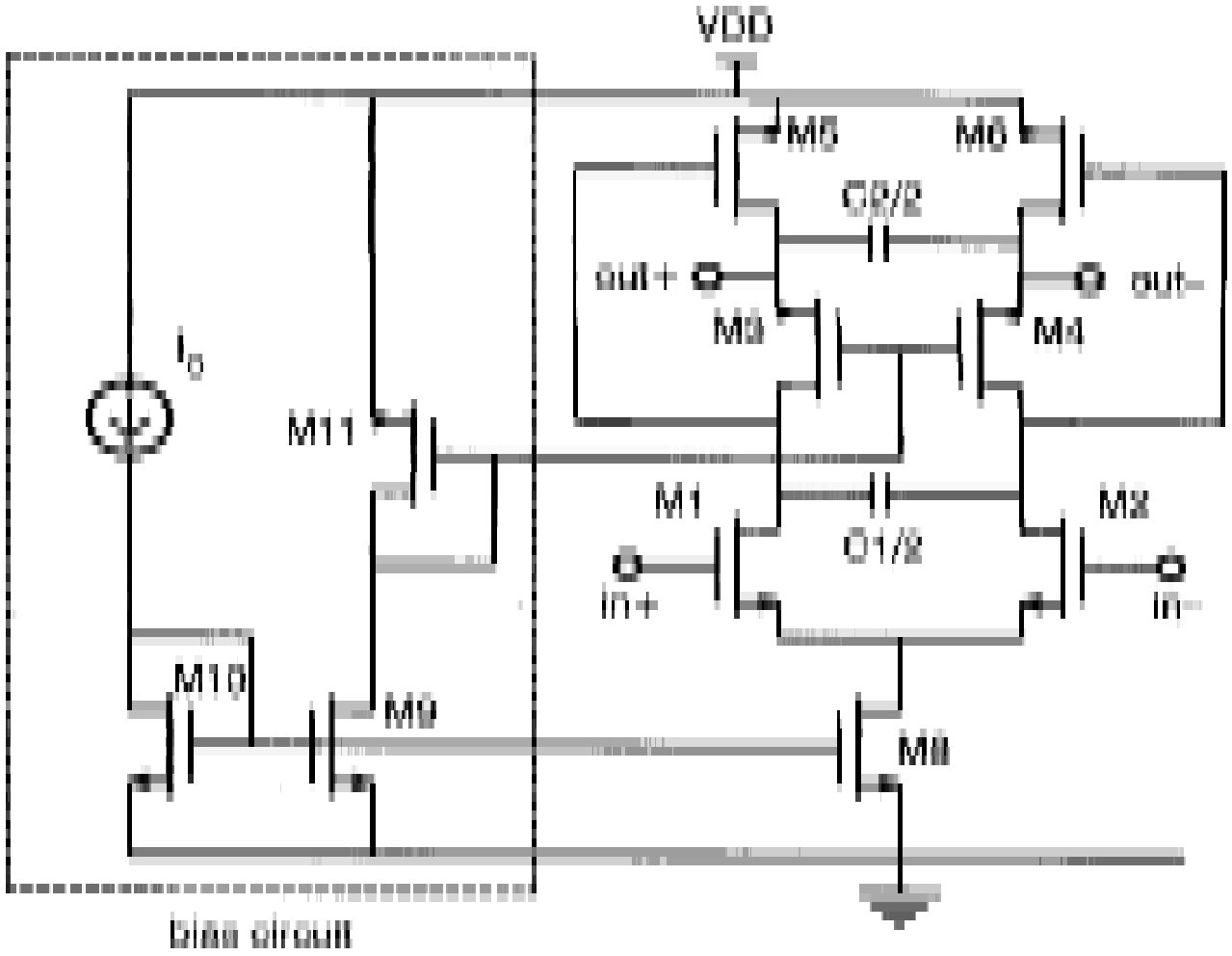




g_m-g_m-C Filter

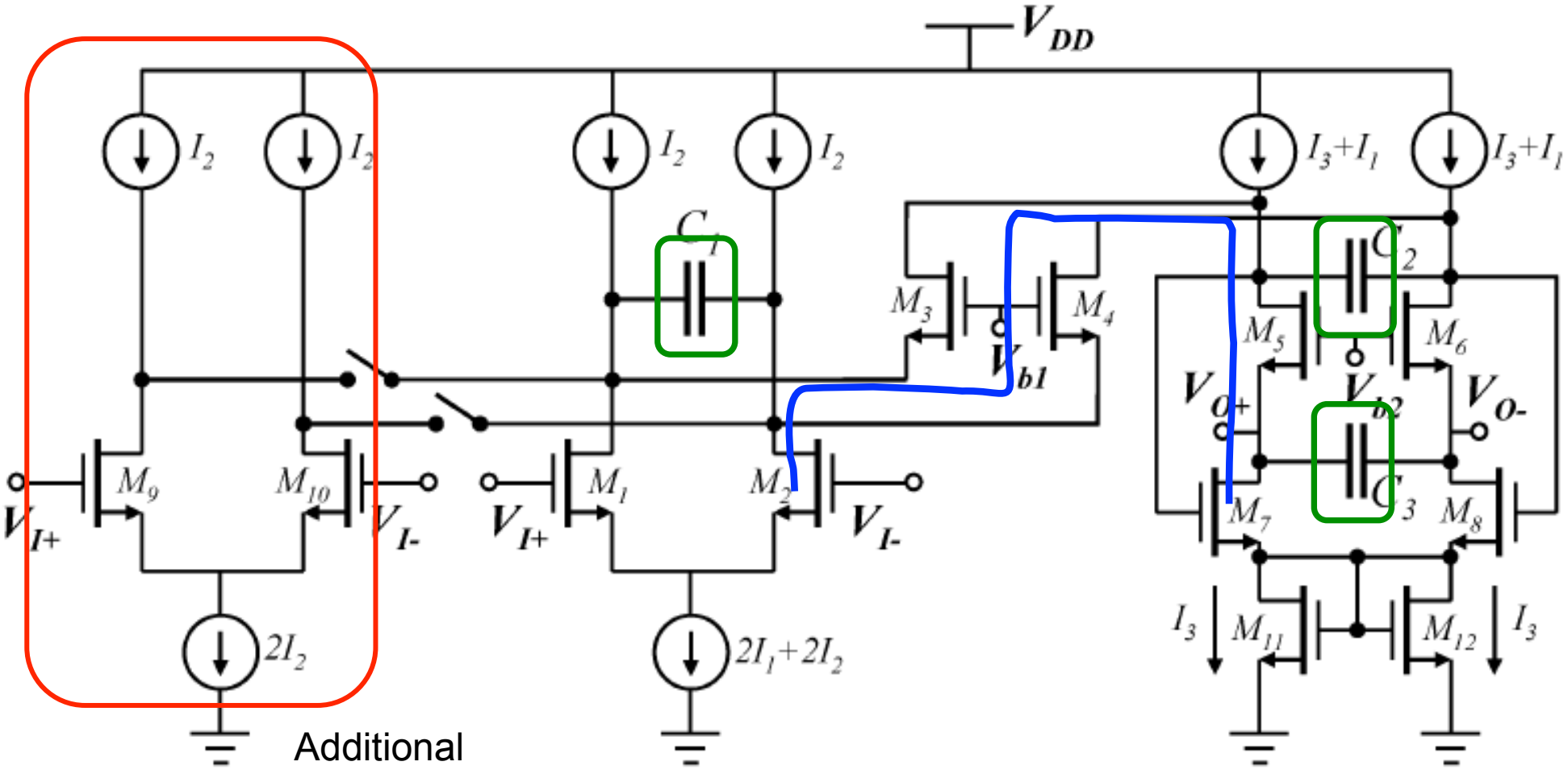
2nd order cell

- Complex pole ***in the active (non-linear) load***
  - Single–Branch biquad !!!



g_m-g_m-C Filter

3rd order cell *

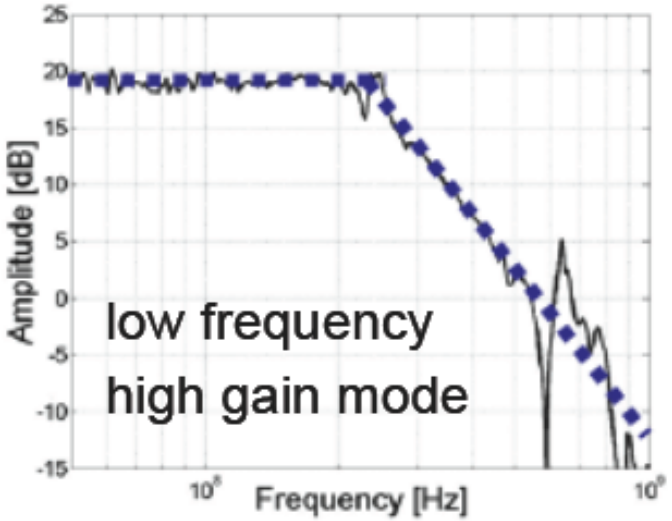


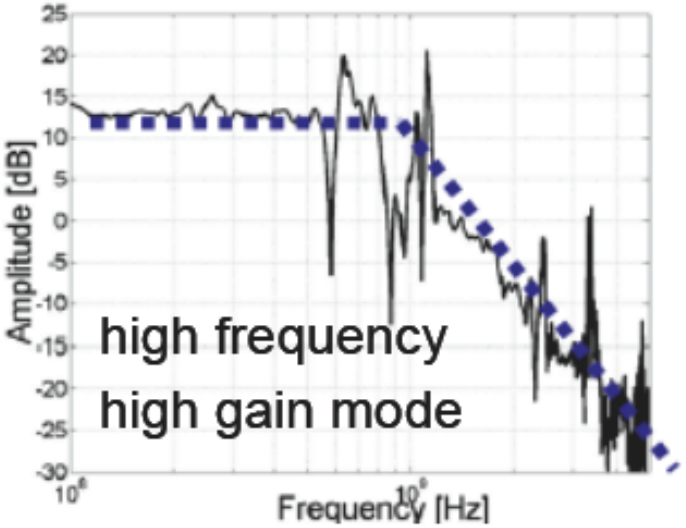
Additional input stage for gain control

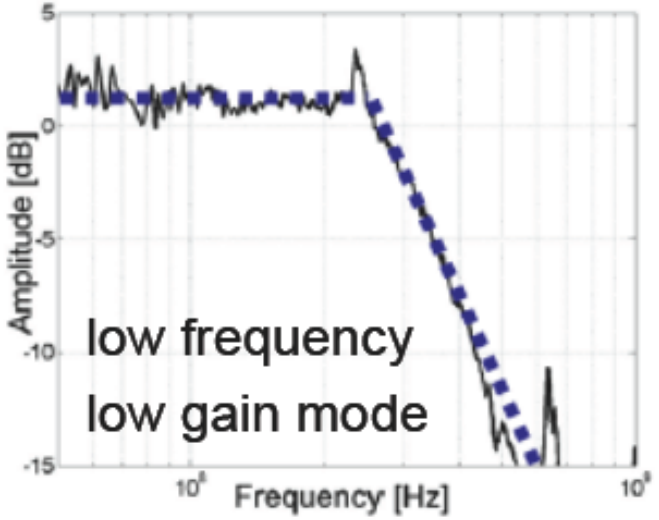
* Ruckaert, IEEE-JSSC2007

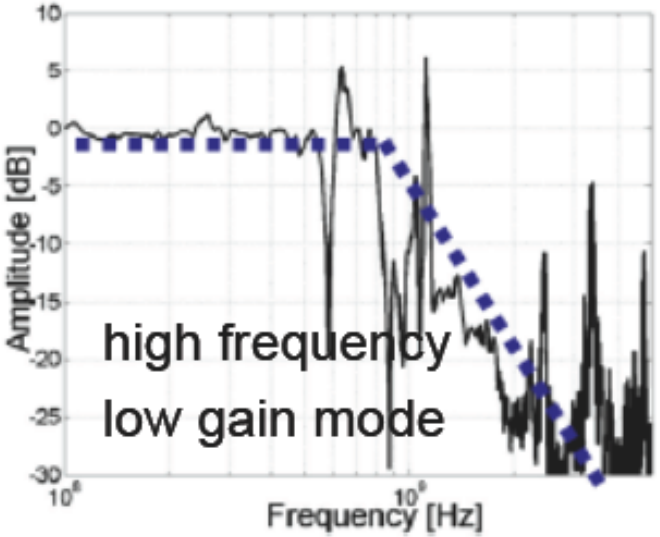
g_m-g_m-C Filter

Experimental results – (180nm - UWB) *







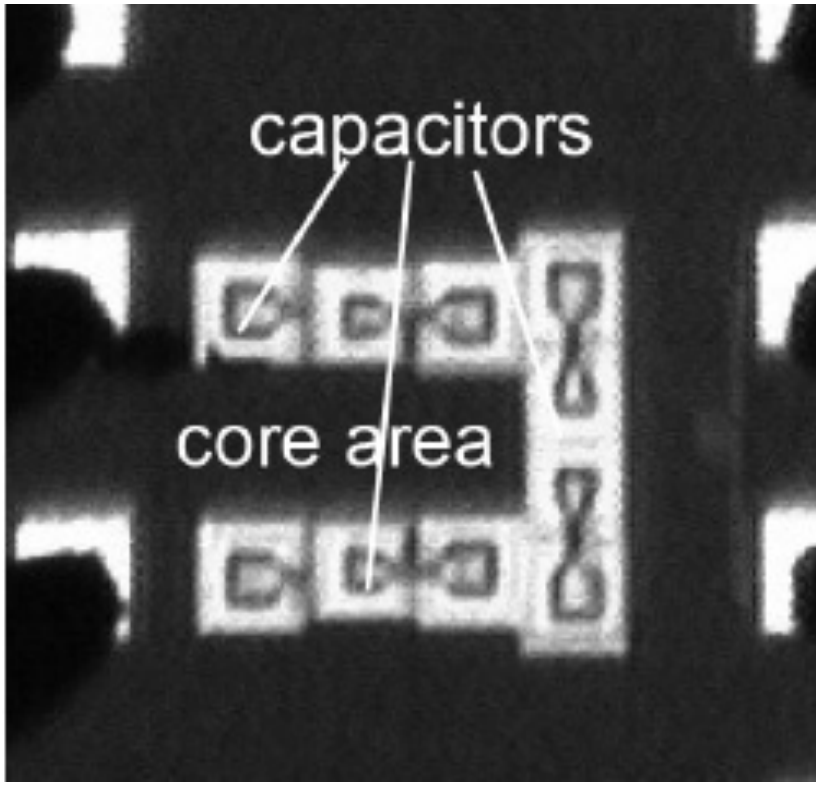


* D'Amico, ESSCIRC2007

g_m-g_m-C Filter

Experimental results (180nm) *

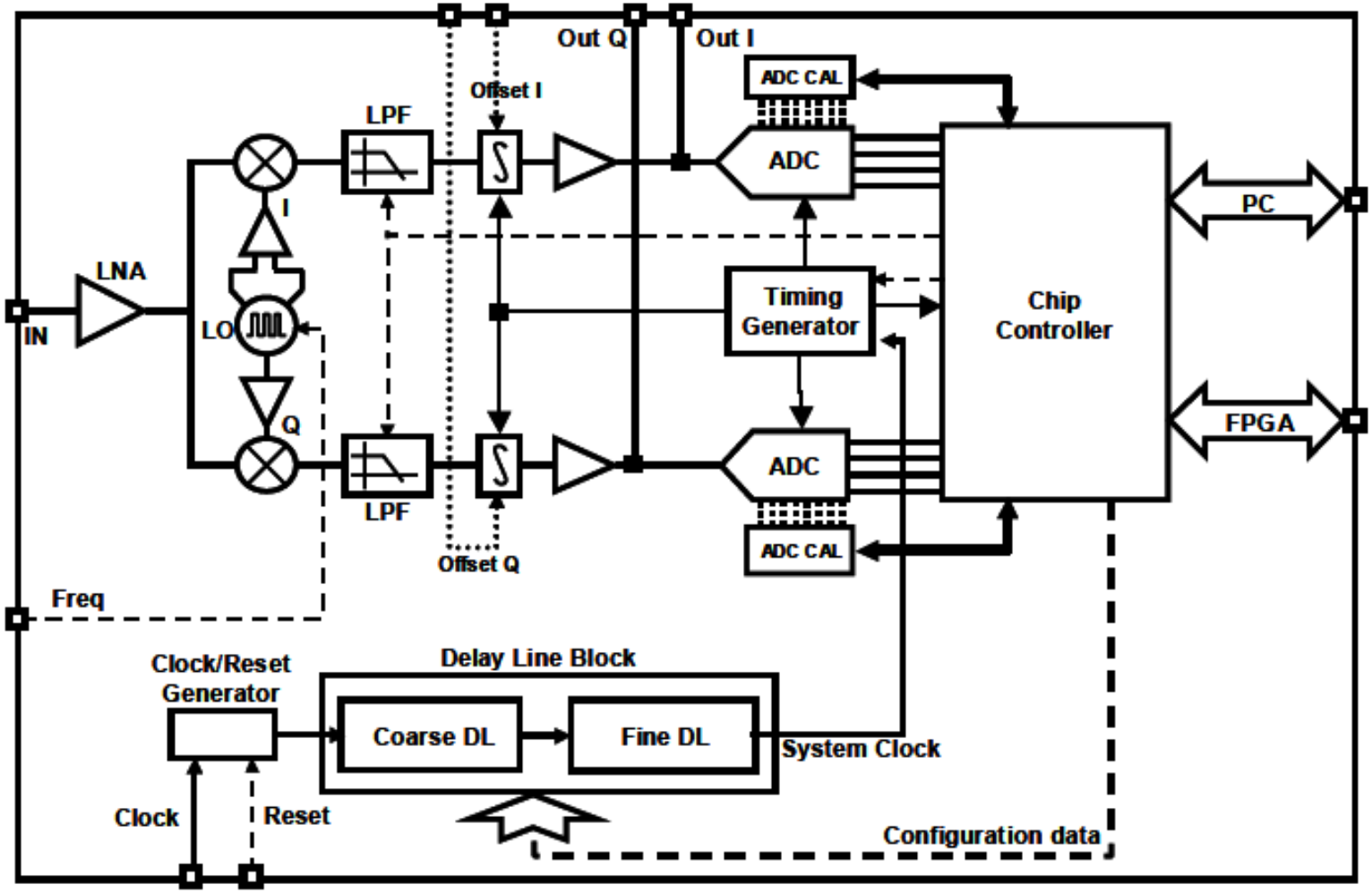
Case	I	II	III	IV
f_o [MHz]	250		1000	
DC-Gain [dB]	2	19	0	14
IR-Noise Level [nV/ √Hz] (simulated)	18	4.5	10	2.5
IR-In-band Noise [μV_{rms}] (simulated)	285	71	320	80
THD@100mVpp [dB] (simulated)	-30	-30	-32	-37
SNR [dB]	45	53	44	53
Power consumption [mW]	0.21	1.2	0.59	3.2
Technology	CMOS 180nm			
Power supply	1.8V			

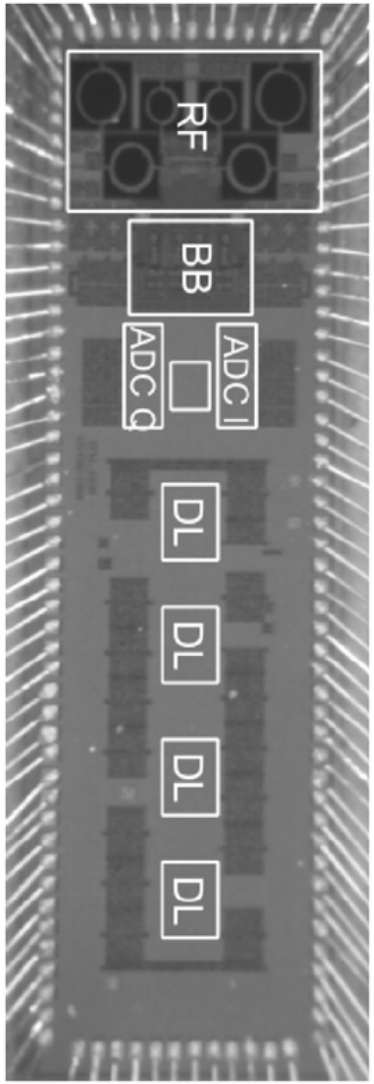


* D'Amico, ESSCIRC2007

g_m-g_m-C Filter

Complete system – UWB receiver *





* Ryckaert, ISSCC2006

Source-follower-based Filter

1st-order LP cell

Source-follower as an analog filter

$$H(s) = \frac{1}{1 + s \cdot C / g_m}$$

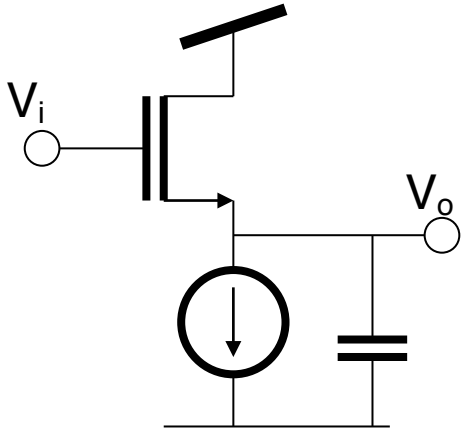
- Feedback structure
  - ➔ The linearity improves with a larger closed-loop gain ($g_m \cdot R_{out}$)
    - Linearity ≈ 1/ V_{ov}

$$V_{ov} \Downarrow \rightarrow THD \Uparrow$$

$$Bandwidth = \frac{Power}{Linearity} \rightarrow Bandwidth = Power \cdot Linearity$$

$V_{ov} \Downarrow$ ➔ $I \Downarrow$ for a given g_m (=I/ V_{ov})

- ➔ Power reduction for the same linearity
  - In Active-RC & G_m-C filters
    - ➔ linearity requires larger V_{ov}



- ➔ Unitary gain

Source-follower-based Filter

1st-order LP cell

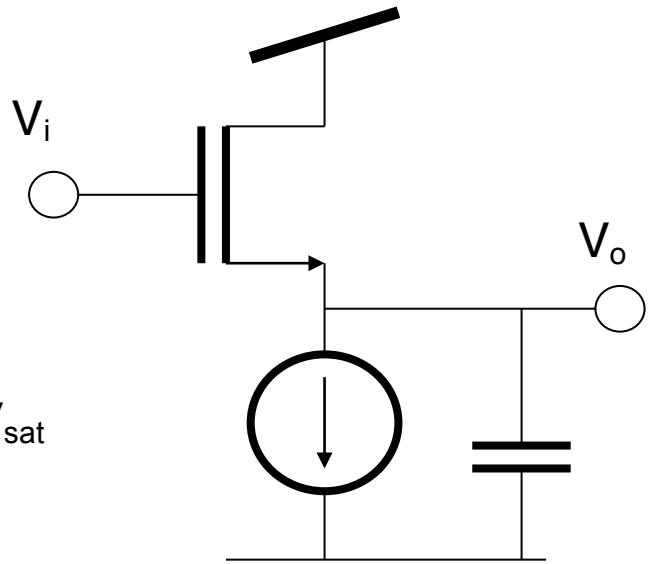
- ☺ Large g_m (with a low current)
  - ➔ good noise performance (at low power)
  - ➔ large cap for a given f_o
    - ➔ t.f. robustness w.r.t. parasitic cap
- ☺ No parasitic poles,

  No extra power to push non-dominant singularities at high frequency
- ☺ No CMFB circuit

  Output CM voltage is fixed ➔ $V_{o_CM} = V_{i_CM} + V_{GS}$
- ☺ Low output impedance

  ➔ **Power reduction**
- ☹ Large V_{DDmin}

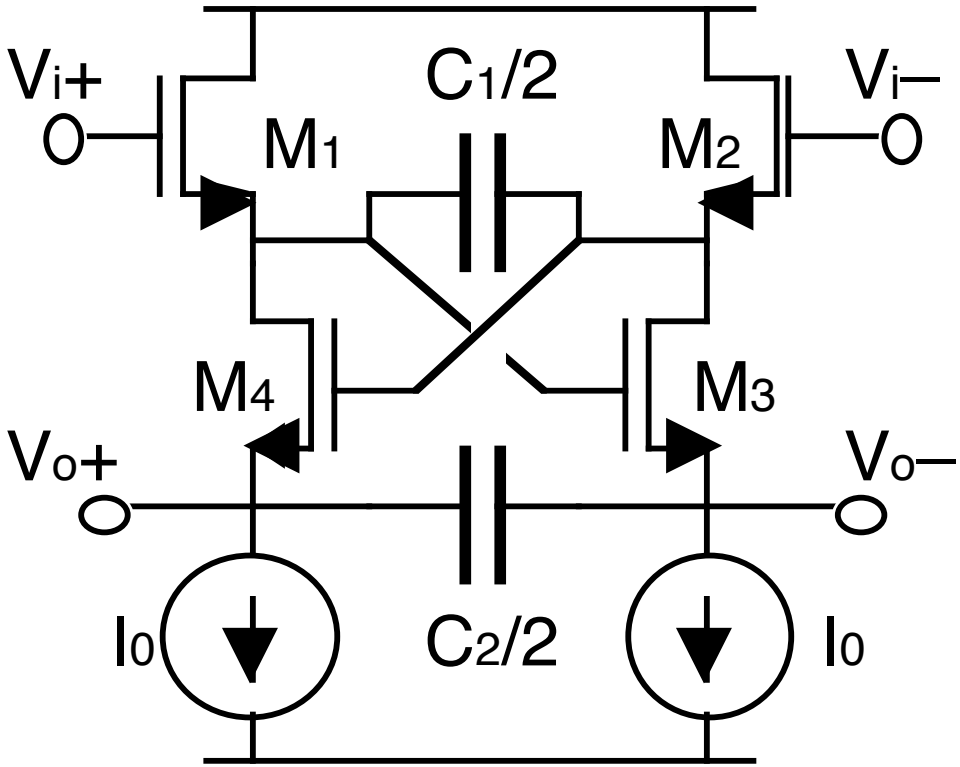
  ➔ $V_{DDmin} = V_{sat}+V_{swing}+V_{GS}+V_{sat}$



Source-follower-based Filter

2nd-order LP filter

- A ***single-branch biquad*** structure
  - Complex pole ***in the active (non-linear) degeneration load***



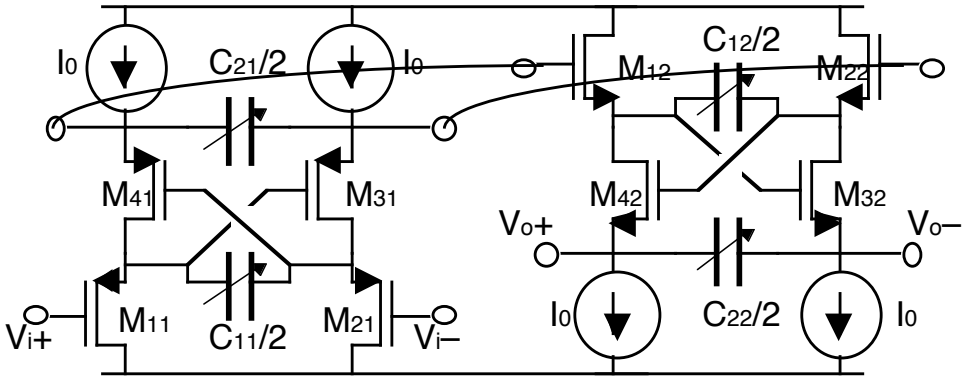
$$V_{DDmin} = 3 \cdot V_{ov} + 2 \cdot V_{TH} + V_{swing}$$

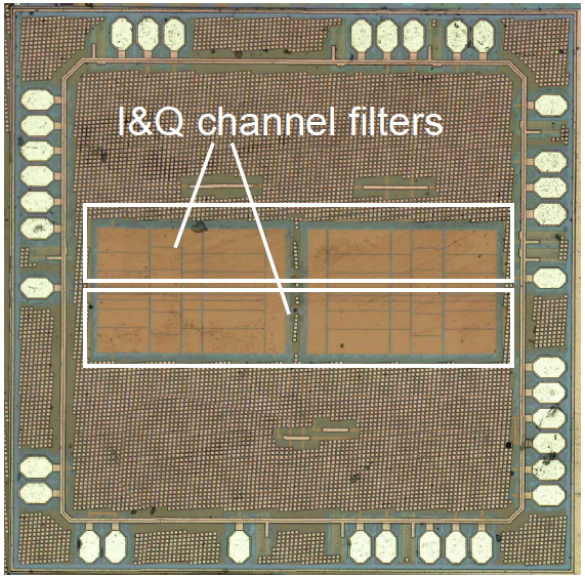
Source-follower-based Filter

Experimental results (180nm) *

- 4th-order Lowpass filter performance summary

Technology	CMOS 0.18µm
Die Area	0.26mm²x2
Power supply	1.8V
Current consumption	2.28mA
Power consumption	4.1mW
DC-gain	-3.5dB
f_{-3dB}	10MHz
f_{-3dB} tuning range	±40%
IRN	7.5nV/ Hz
$V_{in,noise}$	$24\mu V_{rms}$
DR (HD3=-40dB)	79dB
in-band IIP3 (f_1=3MHz, f_2=4MHz)	17.5dBm
1dBcp	5dBm
HD3 ($600mV_{pp}$@3MHz)	-40dB



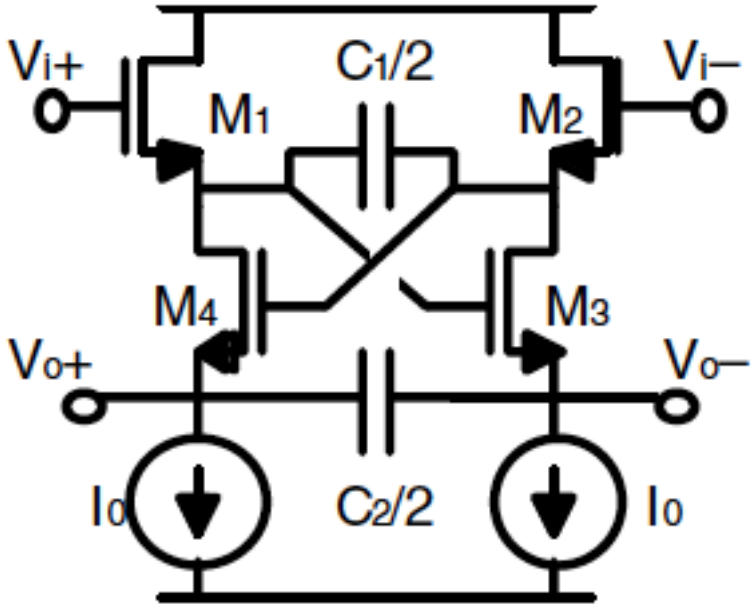


* D'Amico, ISSCC06

Source-follower-based Filter

2nd-order LP filter

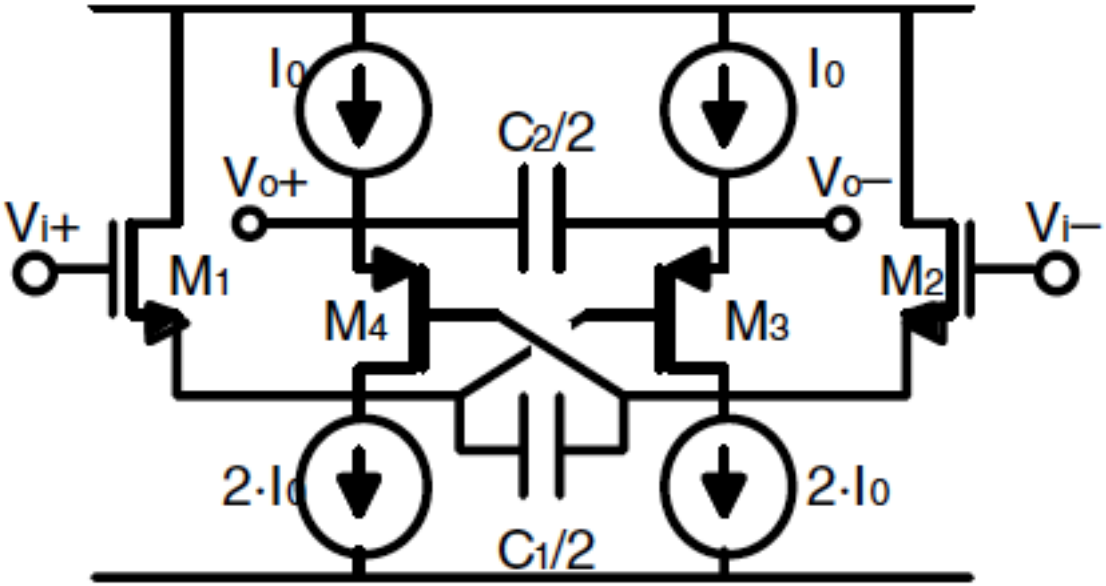
Single branch



$V_{DDmin} = V_{sat} + 2 \cdot V_{GS} + V_{swing}$

$V_{DDmin} = (3 \cdot V_{ov} + V_{TH}) + V_{TH} + V_{swing}$

Folded structure



$V_{DDmin} = 2 \cdot V_{sat} + V_{GS} + V_{swing}$

$V_{DDmin} = (3 \cdot V_{ov} + V_{TH}) + V_{ov} + V_{swing}$

Diode-C Filter

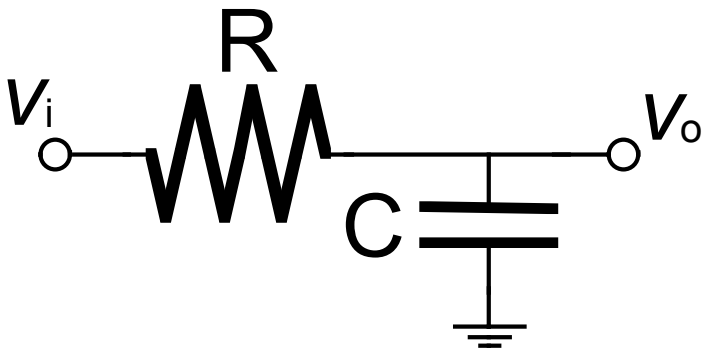
Basic concept

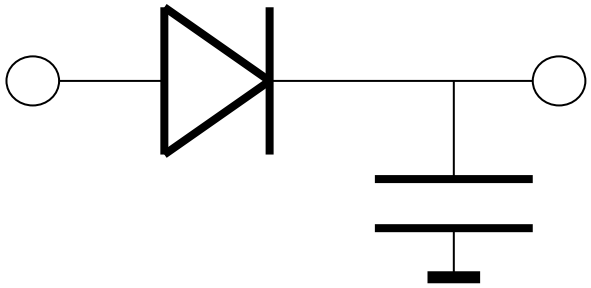
Use non-linear devices for linear t.f. ➔ P⇓

- In a passive RC filter

Concept_1: R can be highly non-linear

- ☺ At LF ($f<f_{pole}$)
  - C is open
  - No current through R
  - $V_o=V_i$ *independently* on R linearity
- ☺ At HF ($f>f_{pole}$)
  - C is short
  - $V_o=0$ *independently* on R linearity
- ☹ Pole ($f\approx f_{pole}$)
  - $Z_R\approx Z_C$
  - ➔ Large R-non-linearity effects





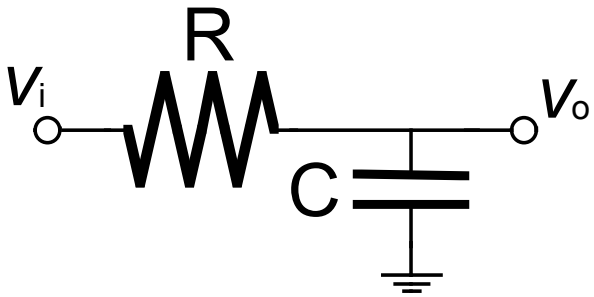
Diode-C Filter

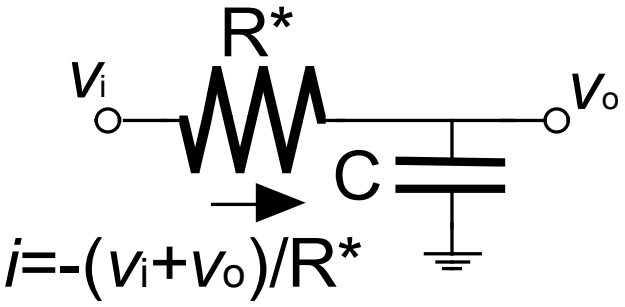
Basic concept

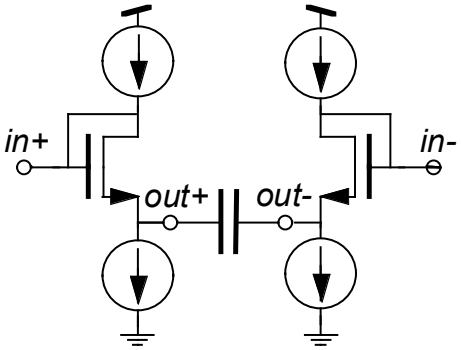
Concept_2: Cascade-RC's do not synthesize complex poles

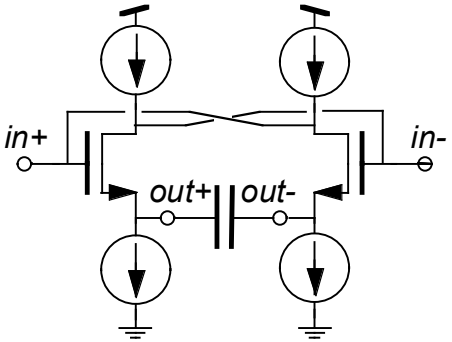
➔ New architecture solutions

- Two building blocks







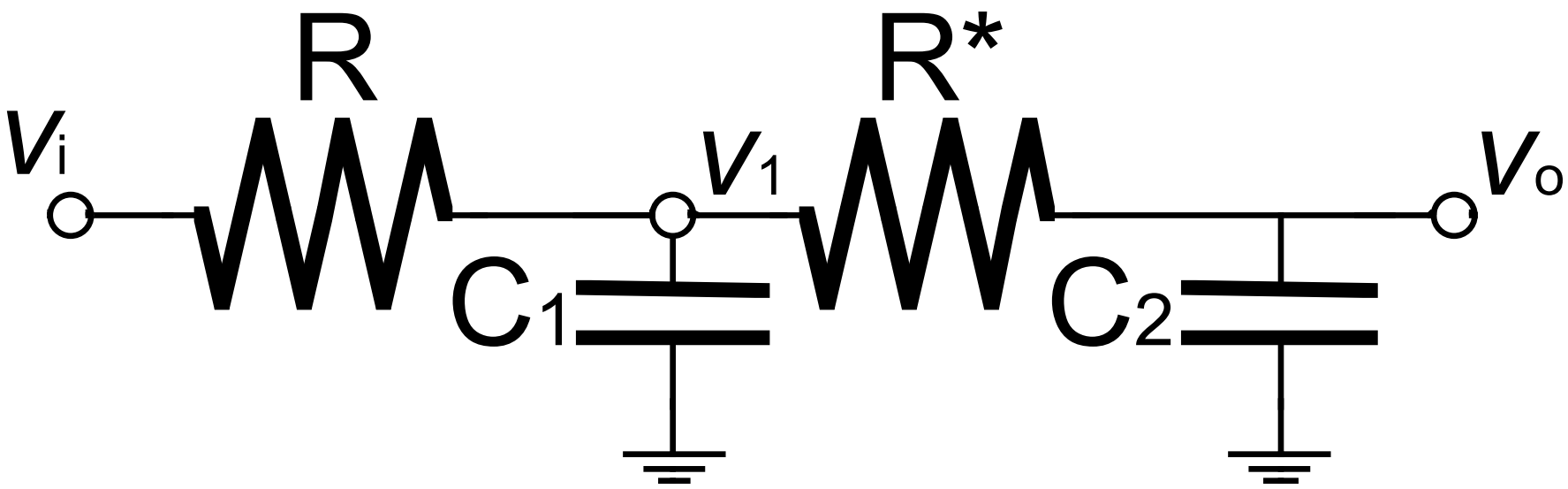


NMOS Positive source-follower RC cell NMOS Negative source-follower RC cell

$$V_{min} = 3 \cdot V_{ov} + V_{th} + V_{swing}$$

Diode-C Filter

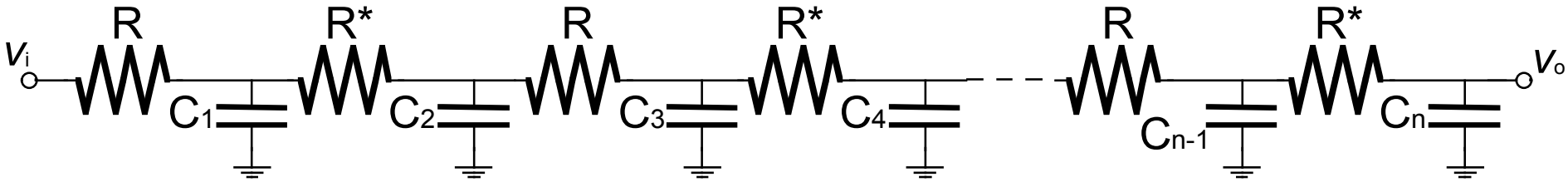
2nd-order filter

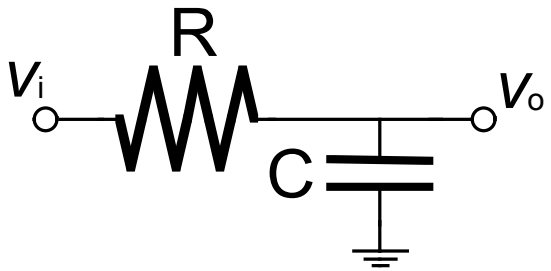


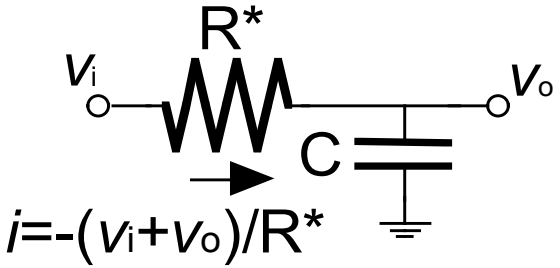
Diode-C Filter

High-order filter

- Cascade of positive and negative cells
  - No DC current



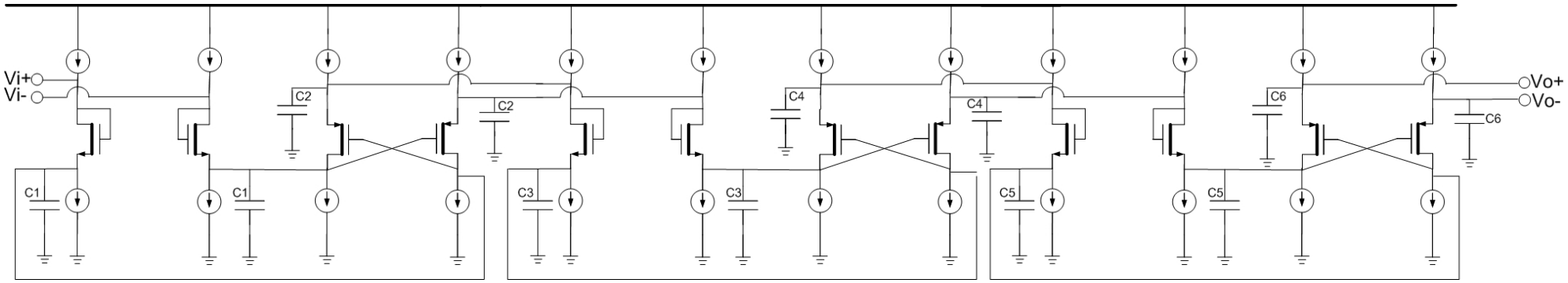


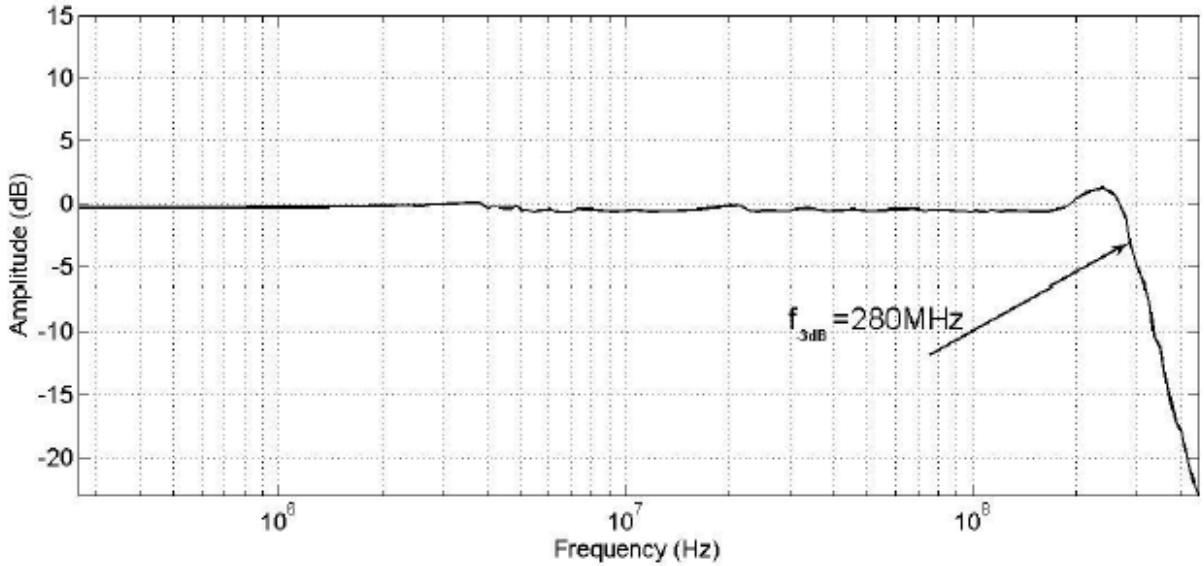


Diode-C Filter

Experimental results (130nm – UWB) *

- A 6th-order filter for UWB receiver
  - f_o = 280MHz

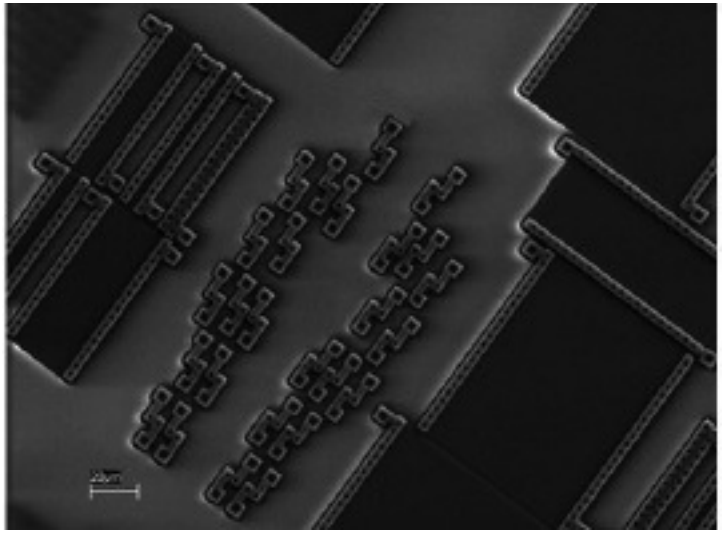


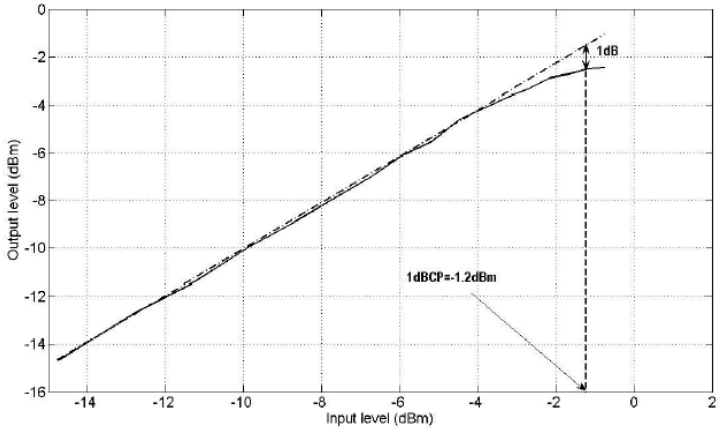


* D'Amico, ISSCC2008

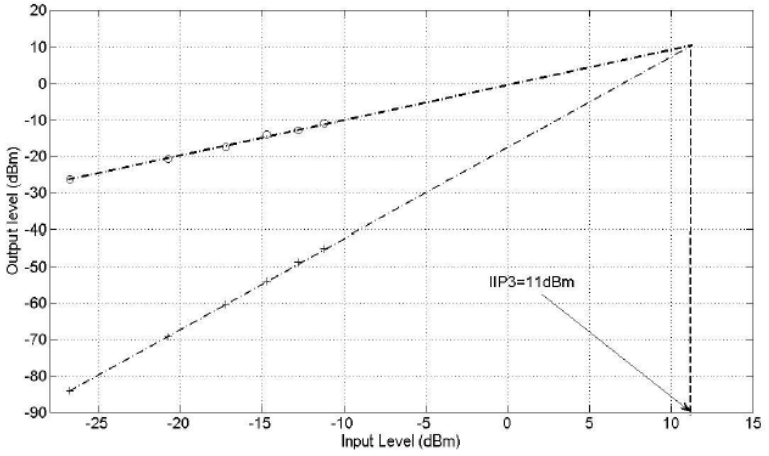
Diode-C Filter

Experimental results (130nm) *





V_{DD}[V]	1.2
CMOS	0.13µm
Power Cons. [mW]	0.12
Filter Order	6th
G [dB]	0
f_{-3dB}	280
DR [dB] (THD>40dBc)	50
Area	0.018mm^2



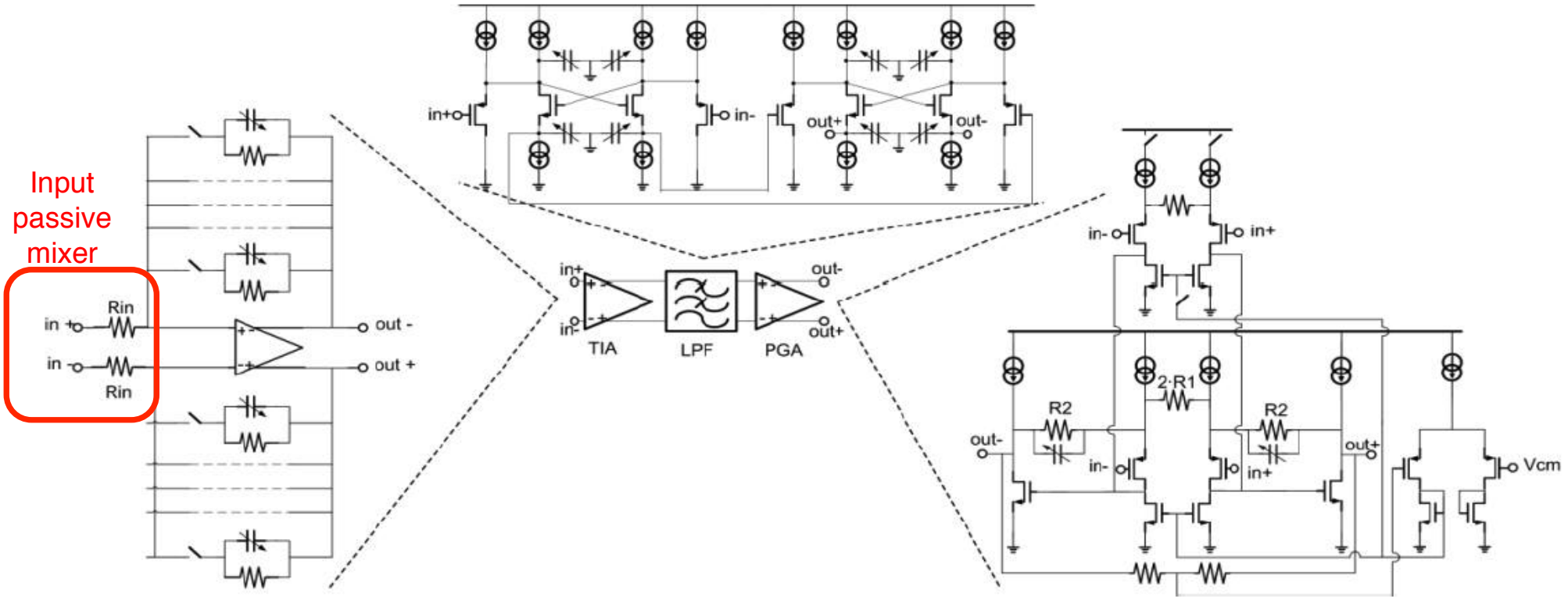
* D'Amico, ISSCC2008

Application: Radar (60GHz) receiver

Architecture

- Exploit the best solution for different blocks

6^{th}-order LPF
20dB-gain
f_o>900MHz



Active-RC
Good virtual ground

Source-follower-based
Low-power

Current-feedback
Gain-programmability

Application: Radar (60GHz) receiver

Experimental results (90nm) *

Work	*Tech.*	*Order*	*f_{-3dB}*	*Gain*	*Linearity*	*Noise*	*Supply*	*Power*	*Notes*
This work	**90nm**	**6th**	**915MHz @0dB**	**0.1dB÷19.6dB**	**IIP3=5.6dBm @0dB gain**	**IRN= -145 dBm/Hz**	**1V**	**9.5mW@0dB 10.8mW@20dB**	
C. Wu et al.- ISSCC 2004	0.18µm	N/A	2GHz	-16dB÷34dB	N/A	N/A	1.8V	40mW	High power
H. Lee et al.- IEEE TMTT	0.18µm	N/A	900MHz	-39dB÷55dB	1dBcp= -10.8÷-59.1dBm	NF= 6.8dB÷67dB	1.8V	20.52mW	Poor linearity
E. O'hAnnaidh et al.- ISSCC 2010	45nm	N/A	800MHz	0dB	THD= -47dB@f_{3dB}/3	SNDR=33dB	1.1V	47.96mW	High power
T. Laxminidhi et al.-TCASI 2009	0.18µm	5th	44-300MHz	0dB	N/A	ORN= 860µVrms	1.8V	54mW	High power
S. Pavan et al.- ESSCIRC 2006	0.35µm	5th	70-500MHz	0dB	18dBm@20MHz (@70MHz BW)	ORN= 366µVrms	3.3V	100mW	High power
J. Harrison et al.- ISSCC 2003	0.18µm	5th	500MHz-1GHz	0dB	IIP3=28.7dBm	IRN= 18nV/√Hz	1.8V	90mW	High power
S. D'Amico et al.- ISSCC 2008	0.13µm	6th	280MHz	0dB	IIP3=11dBm	IRN= 22nV/√Hz	1.2V	0.12mW	No DC-gain
P. Pandey et al.- TCAS I 2006	0.35µm	4th	550MHz	N/A	IIP3=10dBm	-151dBm/Hz	1.65V	140.25mW	High power
T.-Y. Lo et al.- ASSCC 2007	0.18µm	4th	1GHz	0dB	IIP3=17.5dBm	N/A	1.5V	175.5mW	High power

* D'Amico, RFIC2011