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Continuous-Time Analog Filter Design in CMOS Nanoscale Era

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The CMOS nanometer technologies represent a key opportunity for performance improvements, in terms of signal processing quality, power and area, but at the same time is an exciting challenge for analog designers to face MOS second-order effects present in scaled technologies which strongly modifies transistor behavior and operations.
Innovative solutions will be presented to mitigate the problems of:
- biasing Active-RC structures (critical for low VDD-VTH)
- designing large bandwidth closed-loop (Active-RC) filter (critical for high-speed signals)
- reducing the input referred noise (critical for achieving the same DR al lower VDD and, then, lower signal amplitude)
- reducing the power consumption (critical for medium-linearity very high-speed applications)

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