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# Performance evaluation of multiple (16 channels) sub-nanosecond TDC implemented in low-cost FPGA

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NA62 experiment Straw tracker frontend board serves as a gas-tight detector cover and integrates two CARIOCA chips, a low cost FPGA (Cyclon III, Altera) and a set of 400Mbit/s links to the backend. The FPGA houses 16 sub-nanosecond resolution TDCs with derandomizers and an output link serializer. Evaluation methods, including simulations, and performance results of the system in the lab and on a detector prototype are presented.

## Summary

The frontend board (cover) receives the signals from the straws over a flexible PCB called a web board. The cover has been designed to serve several functions, such as distribution of the high voltage for the straws, gas tight detector encapsulation and electronics read out. The charge received is processed in an 8 channel CARIOCA chip, each channel consists of a preamplifier, shaper, base line restorer, comparator and LVDS driver. The LVDS output is fed to the low cost FPGA where the time to digital conversion (TDC) takes place.
The implementation of the TDC on the FPGA is based on the multiple phase-shifted clocks generated by the embedded PLL. Though the maximum clock frequency allowed is still on the sub-GHz region, one can achieve sub-nanosecond resolution by using two 320 MHz clocks at 90 degrees of relative phase. Sampling the LVDS inputs at rising and falling edges of both clocks and carefully designing the tracks and clock domain crossings in the FPGA, we manage to have a fine time measurement of 0.774 ns at 40 MHz input clock. The transition times, along with the identifier of the signal's origin and signal quality information are formed in 24 bit words, which are queued, transformed using the 8b/10b protocol and serialized. The output of the FPGA is routed directly to the RJ45 connector, using the pre-emphasis function of the Cyclon III true LVDS transmitter and can be received at a rate of 400 Mbps per twisted pair up to 15 meters of cable away.
The initial approach for the evaluation of this system was the simulation of different firmware entities with realistic inputs. The TDC has shown outstanding behavior with a RMS of the measurements at 0.3 ns, while queuing structure and communications surpass the technical specifications given, making sure that data loss will be minimized. Several tests with the final prototype of the board have taken place, to support the simulation results. In the lab, routines to gather enough statistics for the TDC behavior with real inputs from the CARIOCA have been developed, which show no particular difference through the whole range of TDC fine measurement and RMS values between 0.7 and 1.5 ns, corresponding to rising or falling transitions, different pulses, attenuation, thresholds and CARIOCA channels. Further studies to verify the effect of different thresholds over realistic pulses in a range of duration and amplitude have been performed and the resulting resolution is fulfilling the requirements and even offering a safety margin. The system was connected to the 64
straw prototype and the tests were repeated over the length of the straw. With new software and small changes in the prototype, studies with cosmic radiation have taken place as a final evaluation of the system.
The performance evaluation of the frontend board shows that the architecture of the frontend electronics is fulfilling the NA62 experiment requirements with a large safety margin.

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