SPADIC – Self-triggered charge pulse processing ASIC

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TWEPP 2013, Perugia
26.09.2013
Introduction

- Self-triggered Pulse Amplification and Digitization ASIC
- main application: TRD readout at CBM (FAIR/GSI)
- development since 2006, latest version 1.0 available since 2012
Overview

Concept

- Single message stream: signal snapshot + metadata
- LVDS serial link

From detector pads

- Multiple channels
- Analog to digital conversion
  - CSA (Charge Sensitive Amplifier)
  - ADC (Analog-to-Digital Converter)
  - DSP (Digital Signal Processor)

- Hit Logic

- MUX (Multiplexer) for channel selection

- CBMnet

- ×32 scaling factor
Charge sensitive amplifier

- input range: 75 fC
- \( h(t) \propto t \cdot e^{-t/\tau} \)
- shaping time: \( \tau = 80 \text{ ns} \)

Two amplifiers per channel selectable:
- positive polarity (4 mW)
- negative polarity (10 mW, not optimized)

Layout & schematics: modular, scalable
CSA characterization

- simulation + previous testchips: ENC = 800 e⁻ @ 30 pF (300 e⁻ @ 0 pF)
- measurements with latest setup ongoing
- tuning of bias settings → local noise minimum found
- “900 ± 900” e⁻ → careful calibration of measurement procedure needed to give exact numbers
**Building blocks**

- ADC
- comparator
- DAC

result: $-1, 0, +1$

- 8 pipelined stages
- input current
- doubled residual current
- using current storage cell
- comparator
- DAC

- Current mode pipelined design
- 25 MHz sample rate, continuously running
- 9 bit nominal output (2’s complement)
- Resolution $\approx 8$ bits
- $4.8 \text{ mW, } 400 \times 300 \mu\text{m}^2$
ADC measurements

INL + noise: static measurements at 20 MHz sampling rate (preliminary bias settings)

![Graph showing INL and noise measurements]

- Red: mean value
- Purple: ±1σ

+2 LSB
-2 LSB

Limit of dynamic range
Digital signal processing

- IIR filter with 4 first order stages
- 16 bit internal resolution
- 6 bit coefficients
- Freely programmable \((-\frac{32}{32}, \ldots, +\frac{31}{32})\)

Average quantization error [LSBs]
Digital signal processing

**purpose:** “ion tail” cancellation

shorten pulses → reduce pileup/help hit logic

tail added using modified input

tail removed with IIR filter

normal pulse shape
(from δ input pulse)

effect on double pulses
Hit logic

- **ADC/DSP**
  - neighbor trigger
  - global trigger
  - dual threshold
  - optional differential mode

- **hit detector**

- **metadata generator**
  - timestamp, channel number, trigger type, etc.
  - message builder
    - 16 bit output format
    - snapshot of signal at trigger time (up to 32 samples according to mask)

- **data wrapper**
  - 9 → 15 bit format
  - 32 bit selection mask

- **Continuous stream of 9 bit samples (25 MHz)**
Selection mask examples

→ allows tradeoff between quality of signal reconstruction and data volume
Multi hits

What happens when a channel is triggered again, before the current message is completed?

First message would end here

New trigger

Timestamp: 3031
Data (24 values): -30, ..., -35
Hit type: self triggered
Stop type: multi hit

+24

Timestamp: 3055
Data (32 values): -31, ..., -32
Hit type: self triggered
Stop type: normal end of message

First message is gracefully aborted
Selection mask is restarted
(In this example, all samples are selected...)
Message output multiplexing

- Global logic
- Message output multiplexing
- Channel output buffers
- Channel numbers one-hot encoded
- Ordering FIFO
- MUX
- Sorted by timestamp!
- 
- Channel 0, 1, 15
- Epoch ch.
- Insert epoch markers
- $\times 2$ (group A, B)
- SPADIC – Self-triggered charge pulse processing ASIC
Error handling

What happens when a channel output buffer is full? Test case:

input signal: square wave, period = 30 time bins (>600 kHz hit rate)
reconstructed output signal: no problem with only one channel active

force buffer overflow with neighbor trigger → MUX can’t read fast enough

Similarly for ordering FIFO, incl. handling of flipped bits (SEU).
CBMnet interface

- error checking, retransmission
- deterministic latency messages (DLM)
- maps data + control traffic to serial LVDS links
- 500 Mbit/s (DDR), 8b/10b encoded (1 input, 2 outputs)
Current status & lookout

- complete test environment (firmware, software) built up during past months
- all parts/features of the ASIC in operation
- no major bugs discovered that can’t be worked around
- characterization of the analog part (CSA, ADC) ongoing
- soon: preparation of multi-chip modules for further beamtests next year
Current status

Layout view

- UMC 180 nm
- overall size: 5 × 5 mm²
- digital part:
  - 3.5 × 4.5 mm²
  - home-made standard cell library
  - 2.5 million transistors, 23k FF, 81k gates
  - 44 Faraday SRAMs
  - total wire length: 14.4 m
  - Power (200 MHz): 600 mW
Test setup

Current status

- Test setup
- Detector
- CBMnet (HDMI)
- Power
- Test pulse injection
- Voltage regulators
- Status LEDs
- FPGA board
  - Susibo → USB
Summary

SPADIC – complete system for charge pulse readout

- 32 channels
- self-triggered recording of whole pulse shapes @ 25 MHz
- programmable selection mask
- neighbor trigger, global trigger
- flexible digital signal processing
- handling of unusual/error conditions (multi hits, buffer overflow, …)
- CBMnet interface: reliable data transmission and synchronization features using 4 LVDS pairs
Spadic
Self triggered Pulse Amplification and Digitization asIC

http://spadic.uni-hd.de