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VIPRAM –2D Prototype and 3D Design

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Associative memory based track finding has been proven to provide a unique solution to fast silicon-based track trigger in the hadron collider environment. Future LHC experiments will demand greater speed and more patterns. While it is unlikely that scaling of 2D technology will satisfy the needs in a cost effective way, 3D Vertical Integration offers the possibility of dramatic improvements. The Vertically Integrated Pattern Recognition Associative Memory (VIPRAM) concept has been presented before. In this talk, we present details of the 2D prototype design, test results of fabricated chips with comparison to simulation studies and future project directions.

Summary

The VIPRAM R&D project has two goals. The first is the increase in pattern density through the use of vertical integration and circuit and geometrical (layout) enhancements. The second is the increase in speed and the improvements in system interface, especially with regard to Level 1 Tracking Trigger applications, through the use of system, circuit and layout enhancements. From the beginning, our design methodology has been to develop concepts and circuitry in 2D to confirm functionality as economically as possible and then translate, where necessary, those ideas into 3D. The first step taken by the VIPRAM Project was the development of a 2D prototype (protoVIPRAM1) in which the associative memory building blocks were laid out with an eye toward future vertical integration. In fact, the associative memory building blocks were laid out as if this was a 3D design. Room was left for as yet non-existent Through Silicon Vias and routing was performed to avoid these areas. The vertical integration approach taken thus far by the VIPRAM project reconfigures the pattern recognition algorithm into CAM cells and Control cells each of which ultimately will be integrated on different 3D Tiers. In protoVIPRAM1, there are four independent but identical CAM cells for each Control cell arranged into a unit called a protoLeg. Each protoLeg contains all the memory, comparison circuitry and evaluation logic necessary to perform the pattern recognition algorithm for one complete 4-layer road. protoVIPRAM1 is an array of 32 by 128 protoLeg cells. The readout circuitry is deliberately simplified to allow direct performance studies of the CAM and Control cells. protoVIPRAM1 was designed and fabricated in a 130nm Low Power CMOS process that has been used previously in High-Energy Physics 3D designs. The design has been thoroughly simulated at all levels and the prototype has been tested both for functionality and performance using a custom test setup. These simulation and test results will be presented and compared in this talk.

protoVIPRAM1 is a natural starting point for the project. The next two steps will be done in parallel and will, in fact, feed off of one another. protoVIPRAM3D takes the circuitry designed in protoVIPRAM1 and vertically integrates it. The Control cells are moved onto a Control Tier and the CAM cells become a CAM Tier. A maxim of this project is that given properly designed sub-circuits, vertical integration is a solution to pattern density limitations. protoVIPRAM2D, on the other hand, attempts to improve the readout speed of the associative memory chips and bring the system-level interface to maturity using conventional 2D VLSI with an eye towards Level 1 trigger applications. Several of the ideas created for protoVIPRAM1, most notably the square layout of the CAM cells and the simplified readout architecture, are being used as stepping stones for increasing readout speed and flexibility. The talk will cover the design and status of protoVIPRAM2D and protoVIPRAM3D as well as the goals and directions of the project.

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