A new Rad-Hard DC/DC buck converter ASIC for LHC experiment upgrades

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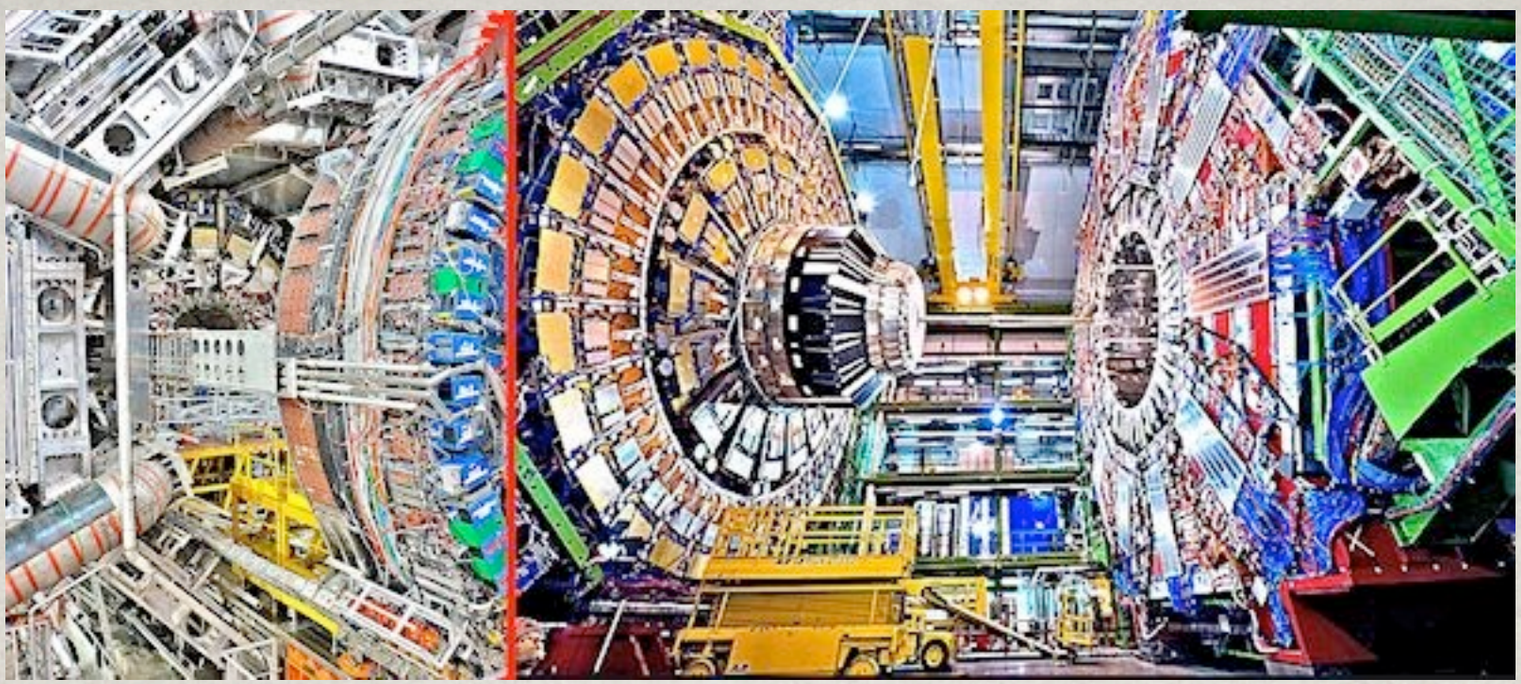
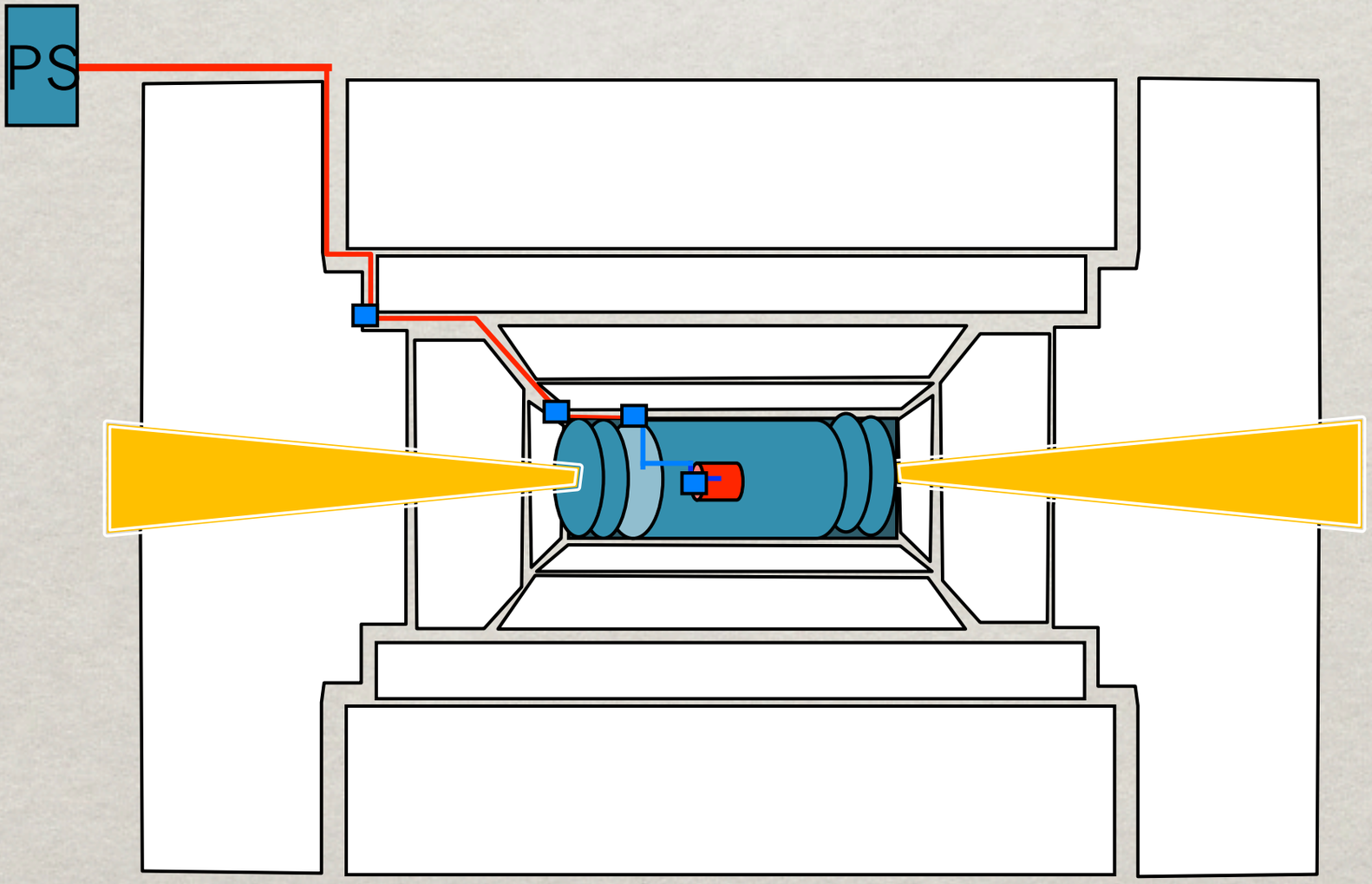
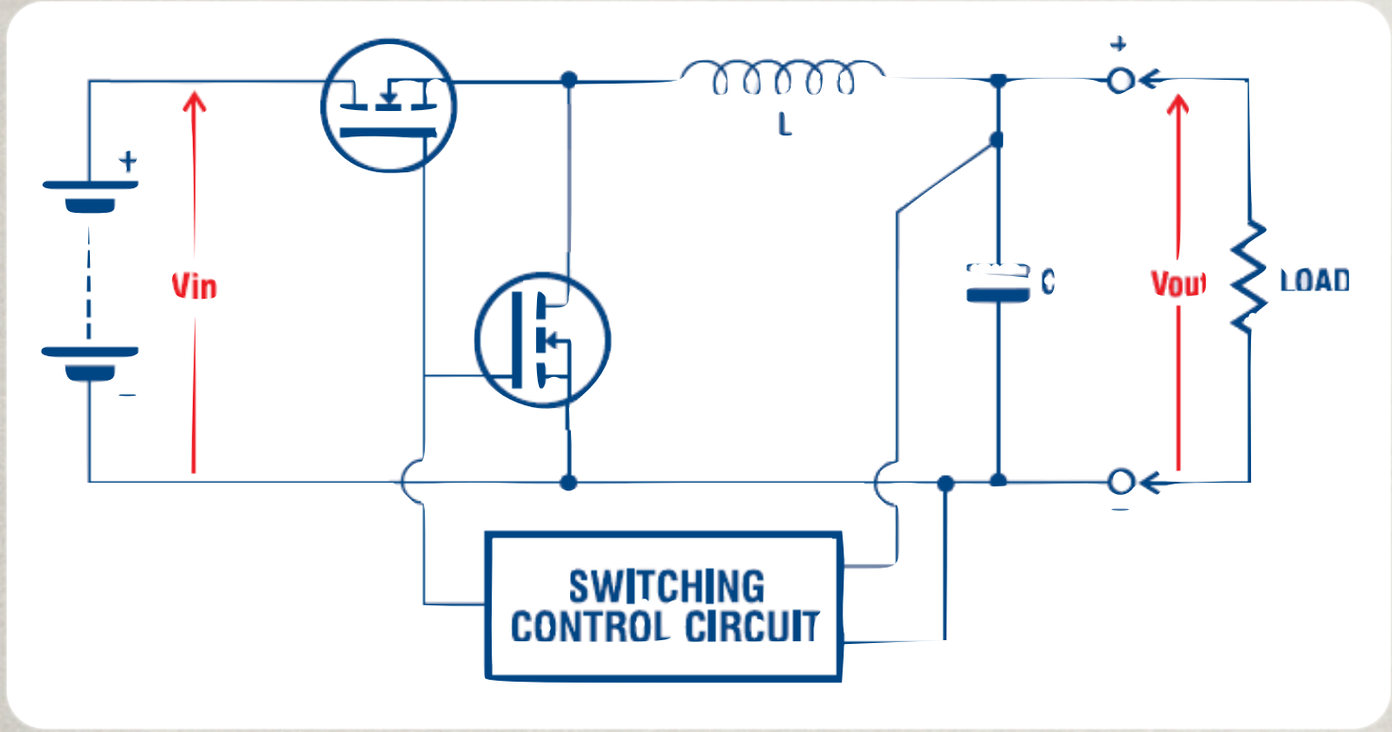



PS

Power distribution with DC-DC converters



Buck Converter

Specifications

Vin<=12V

Vout=0.6-5V

Iout<=4A

frequency=1.8 MHz

Constrains:

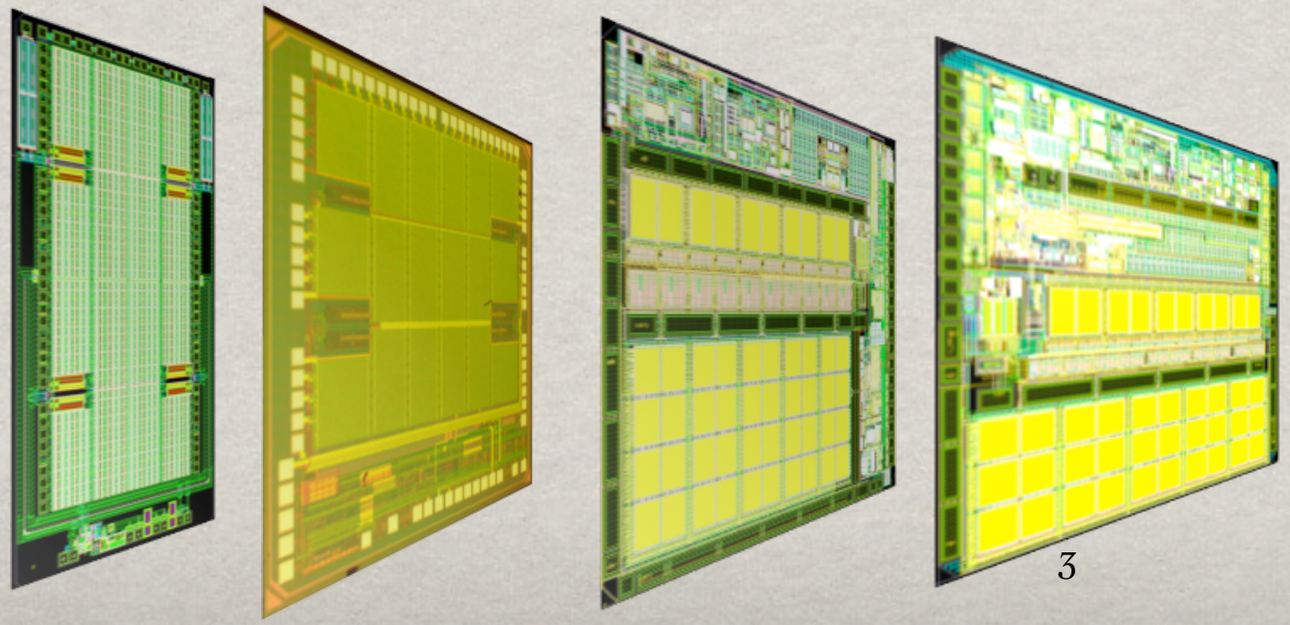
magnetic (2T-4T) fields

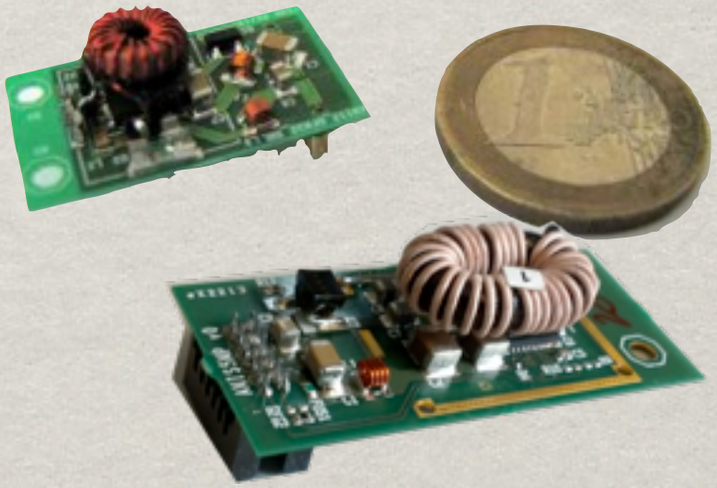
radiation (TID>100Mrd,

fluence < 7 10^{14} n/cm²

ions with LET<15MeV ·cm²/mg)

Amis1 Amis2 Amis4 Amis5

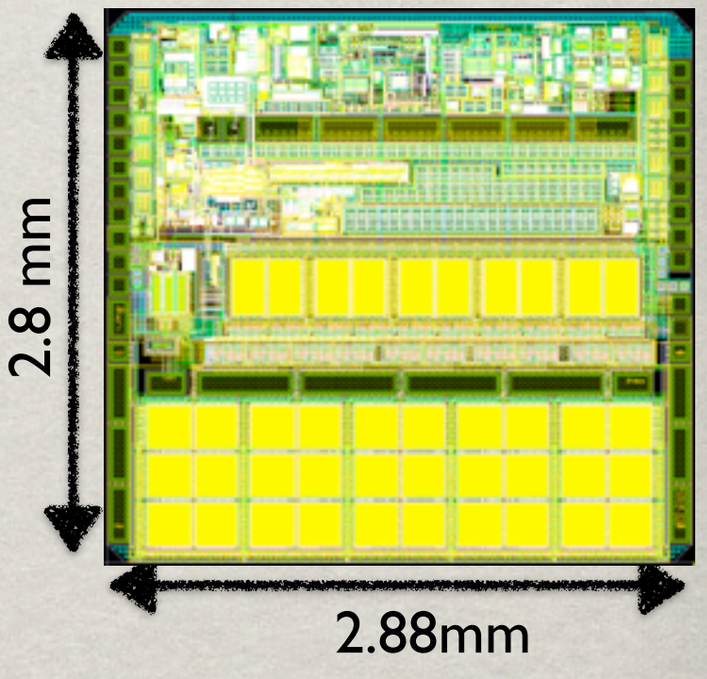




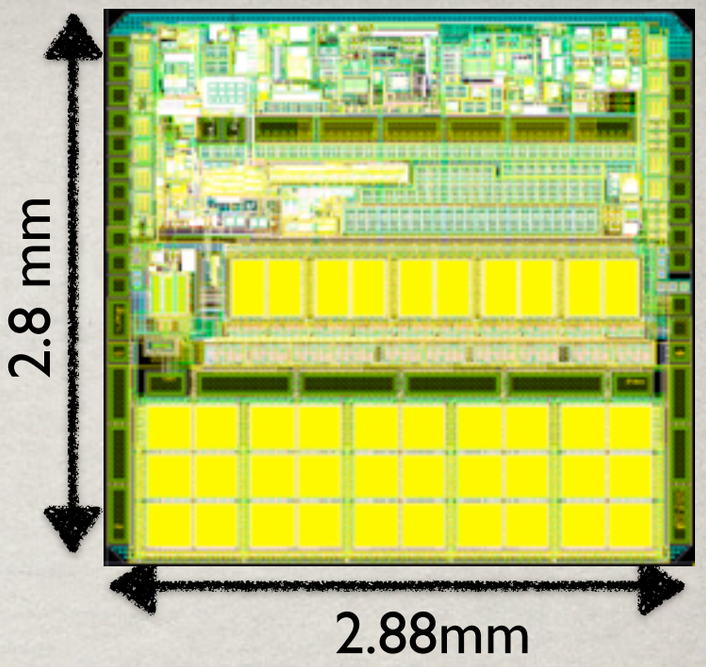
FEAST

Some features integrated in the prototype:

- Bandgap
- 4 linear regulators: Pre-Reg, Analog, Digital and Driver
- Handling of the dead time with adaptive logic
- Improved power transistors' design to reduce TID effects
- Possibility to enable only 2/5 of the power transistors for small Iout
- Enablers
  - Complete circuit
  - Dimension of the power transistors
- Pretection
  - Over-current (OVC)
  - Over temperature (OTP)
  - Input Under Voltage Lock Out (ULVO)
- State machine for more reliable start-up procedure and handling of the signal from protection circuitry
- Power good signal if Vout is the one selected



FEAST



- Following the evaluation of AMIS5, circuit modifications were implemented to address all of the observed 'problems'
- The design was completed in April tape out happened immediately. The chip has been included in an MPW in the I3T80 process where we were the only customer: all reticle available to repeat the circuit 9 times:
  - Chip size: 2880 x 2800 um^2
  - Number of good reticles per wafer: 148
  - Total number of good chips: 1,332
- Individual samples and 6 wafers (worth about 8,000 chips) delivered in mid-July
- Electrical evaluation, TID irradiation and Heavy ions SEE test performed since

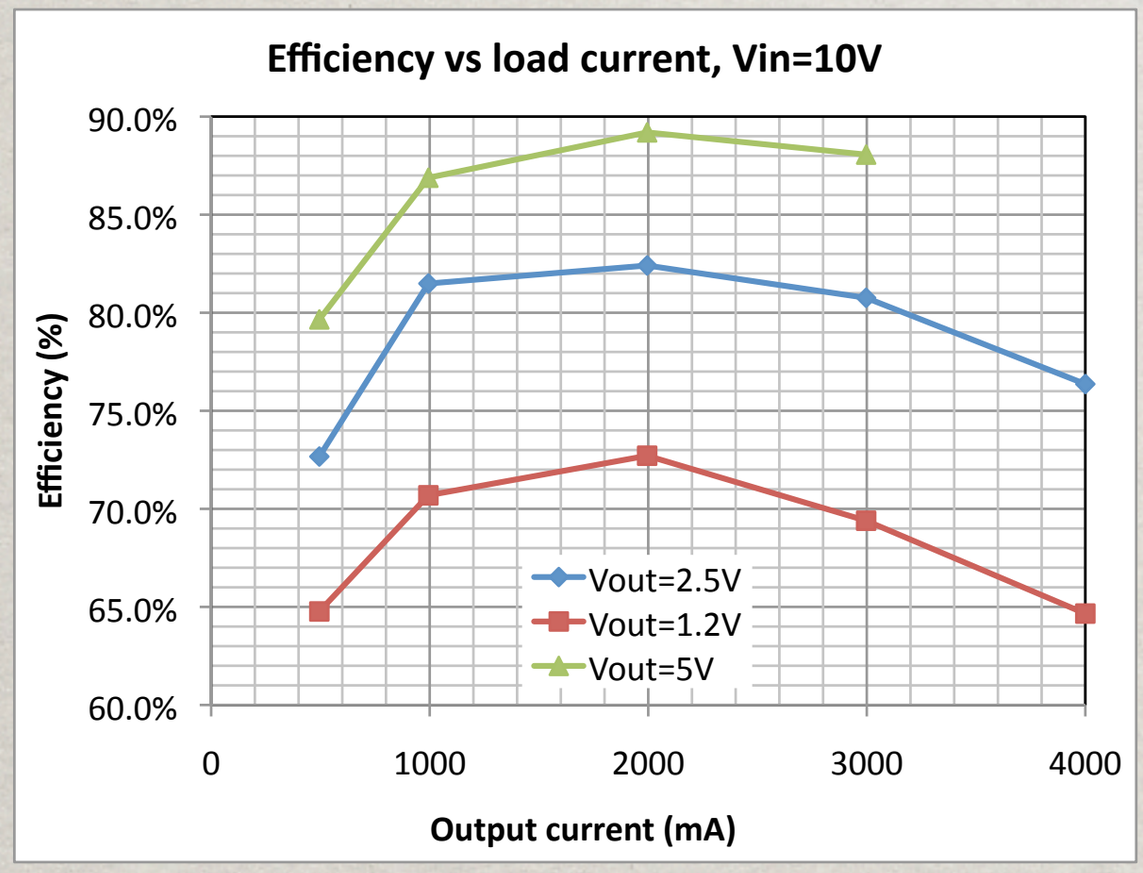
Electrical performance

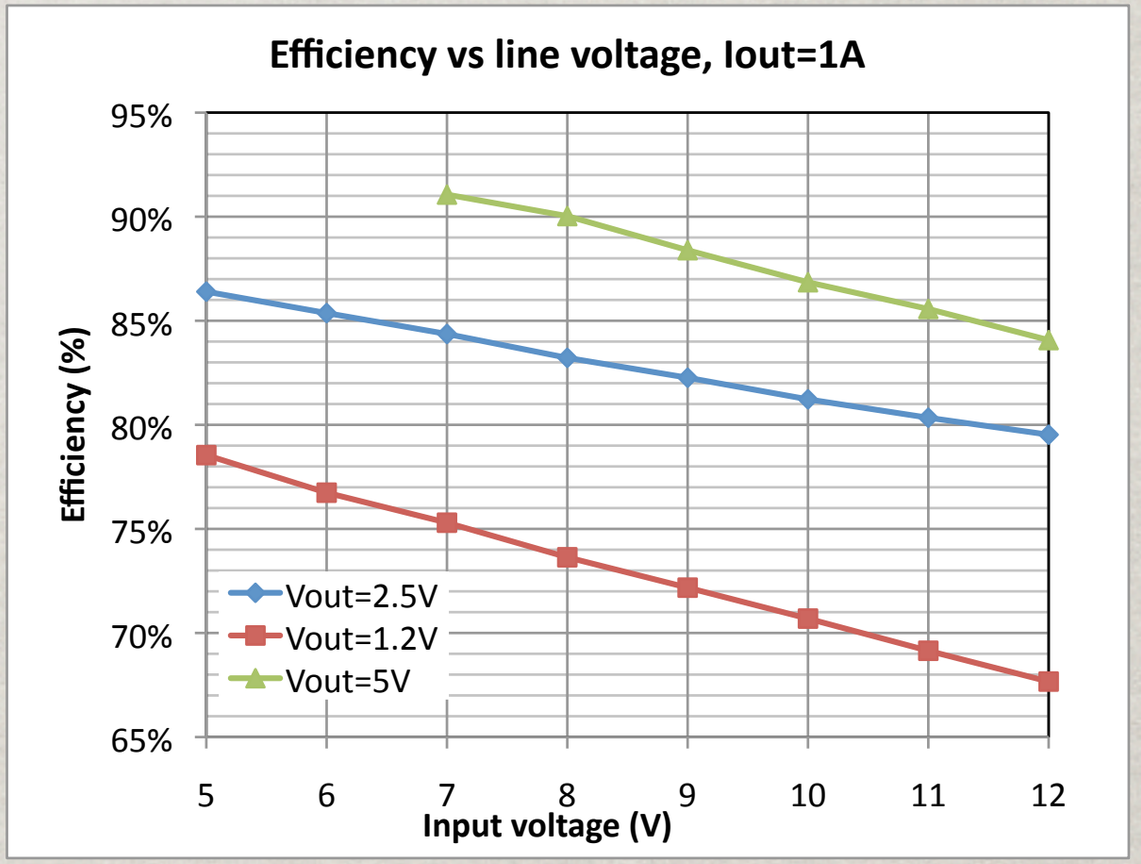
Electrical

- **FEAST is working with very good performances.**

- Issues found in AMIS5 are solved:
  - Vbg and frequency not affected by load
  - Vout is always pulled down to gnd when chip disabled
  - No problem at start-up: always a soft start
  - PG appears always correct, now it is linked to Vout
  - In no tested condition the converter enters an unforeseen state. It always turns off, then on again, as it should (we introduced a double threshold for Under Voltage Lock Out)

Efficiency

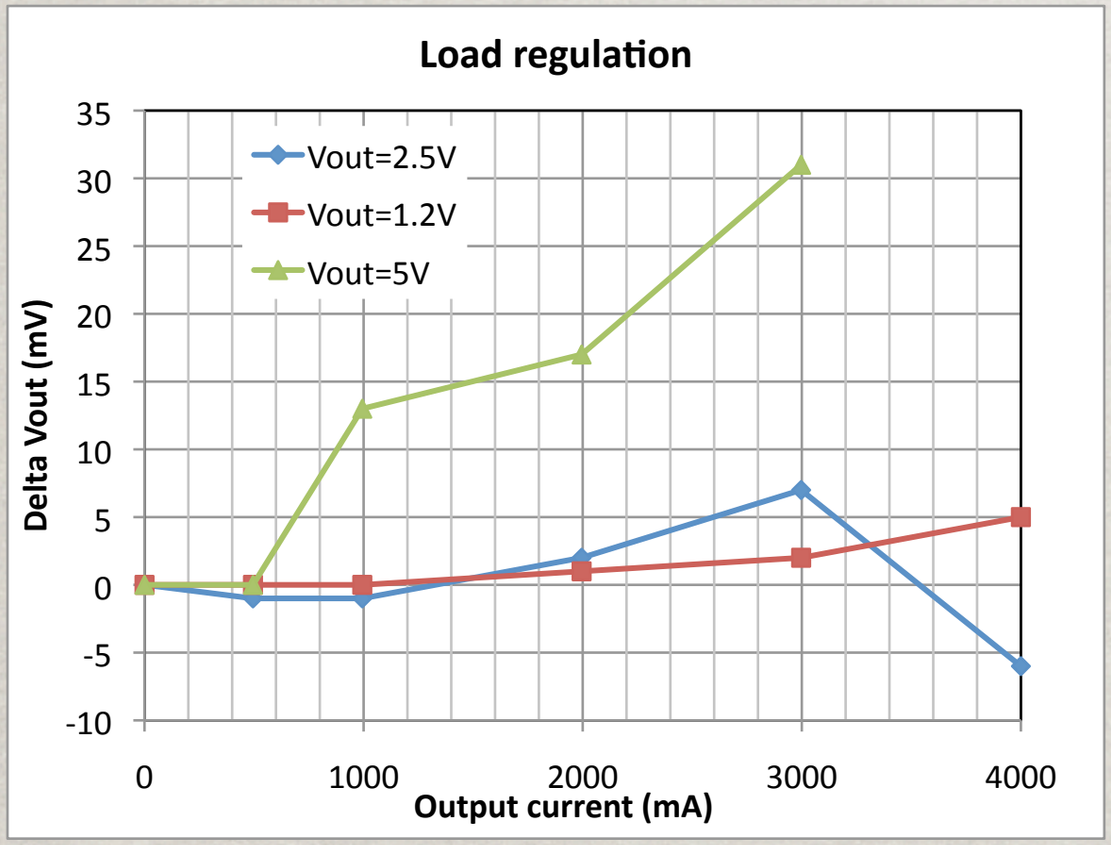




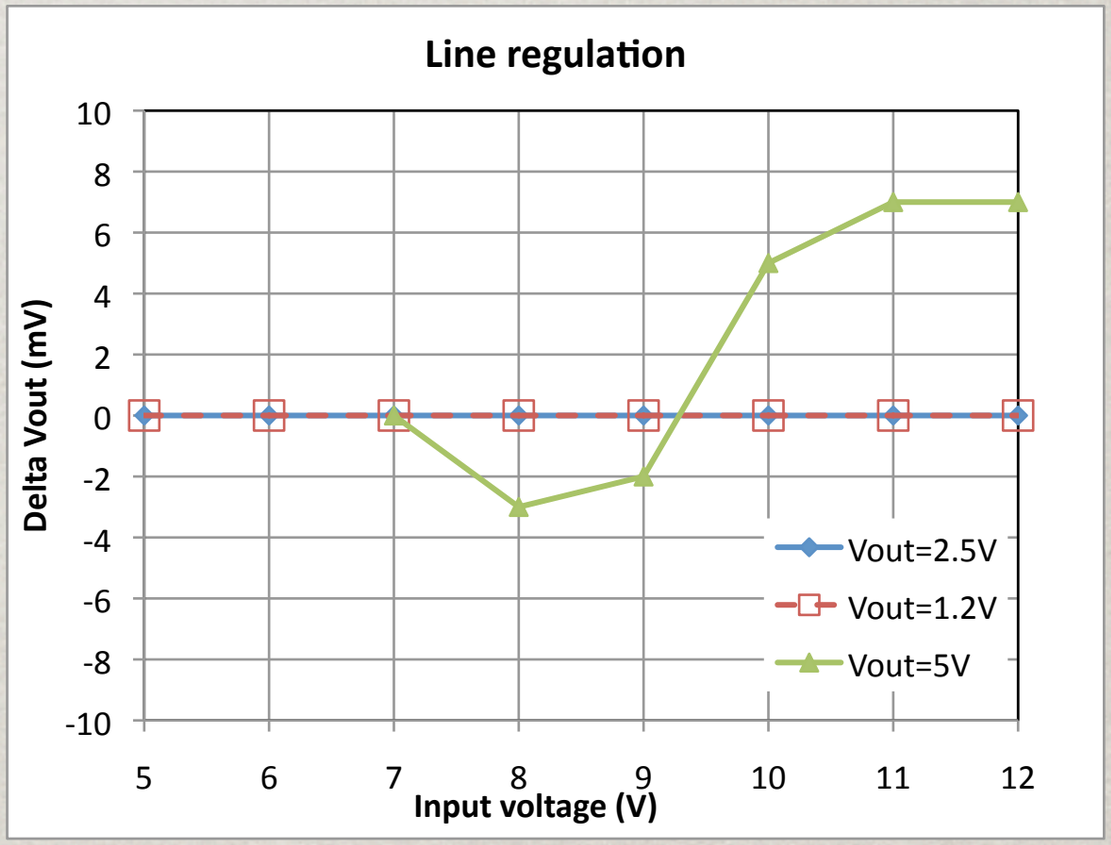
Conditions: cooling plate at about 18C, L=430nH oval toroidal (bulk Cu wire), f=1.8MHz

Regulation

Load regulation is the capability to maintain a constant output voltage level despite changes to the output current.



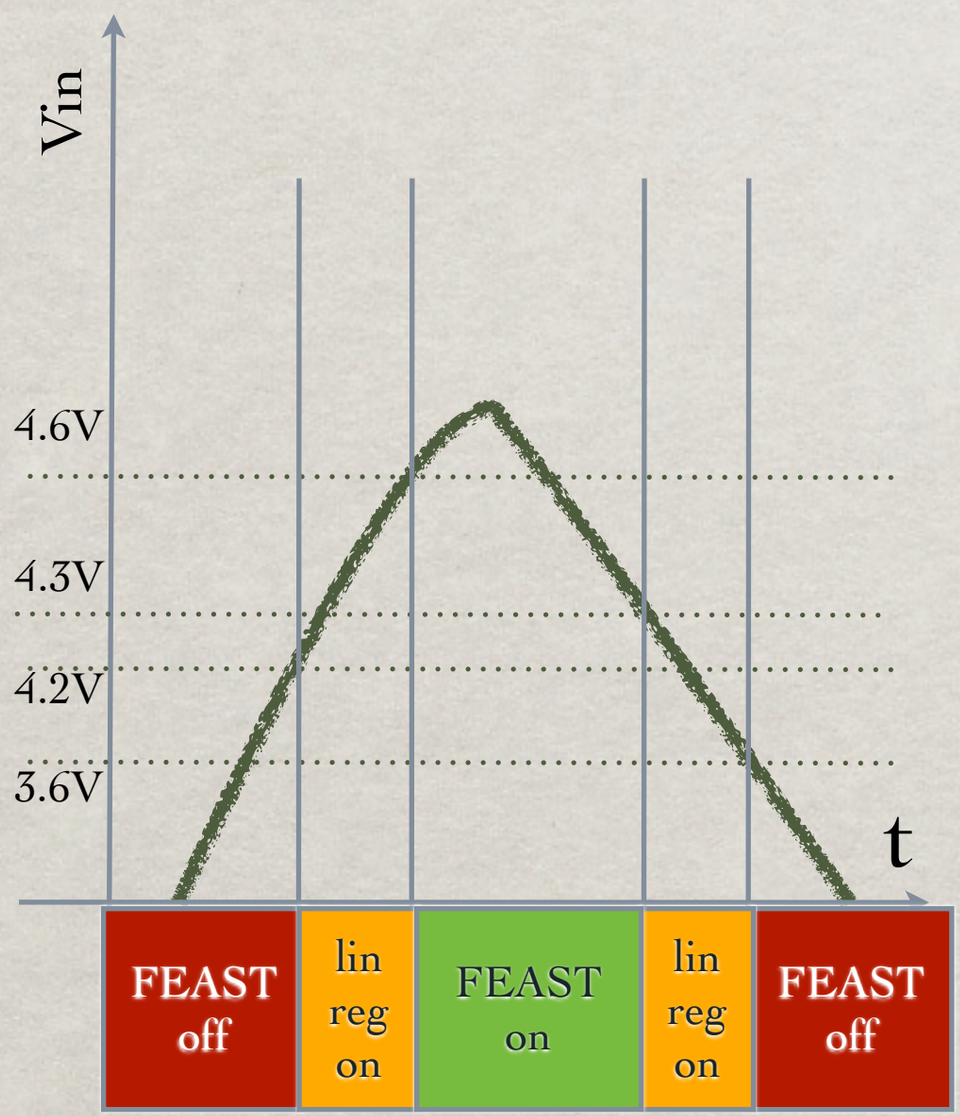
Line regulation is the capability to maintain a constant output voltage level despite changes to the input voltage level.



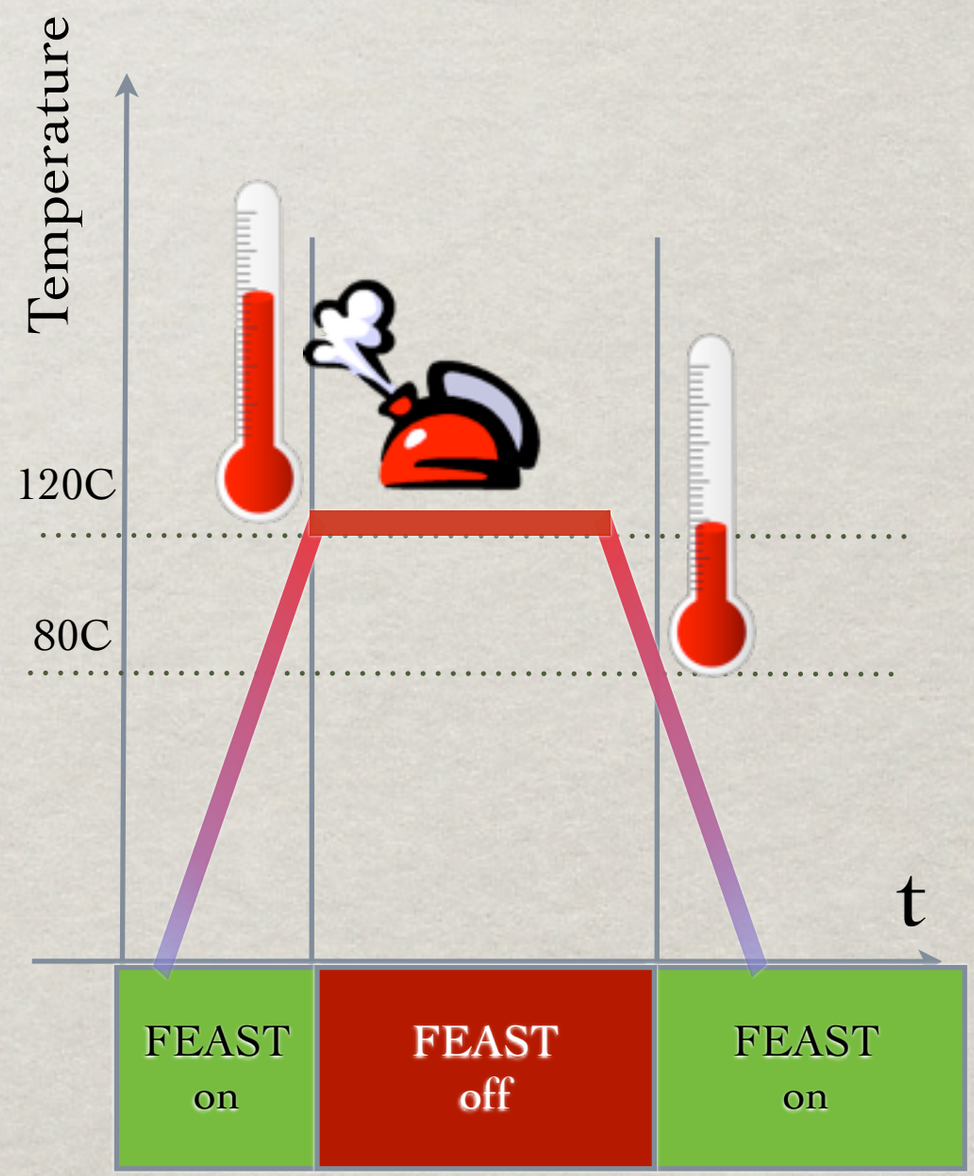
Conditions: cooling plate at about 18C, L=430nH oval toroidal (bulk Cu wire), f=1.8MHz

Protections

Input Under-Voltage lock-out

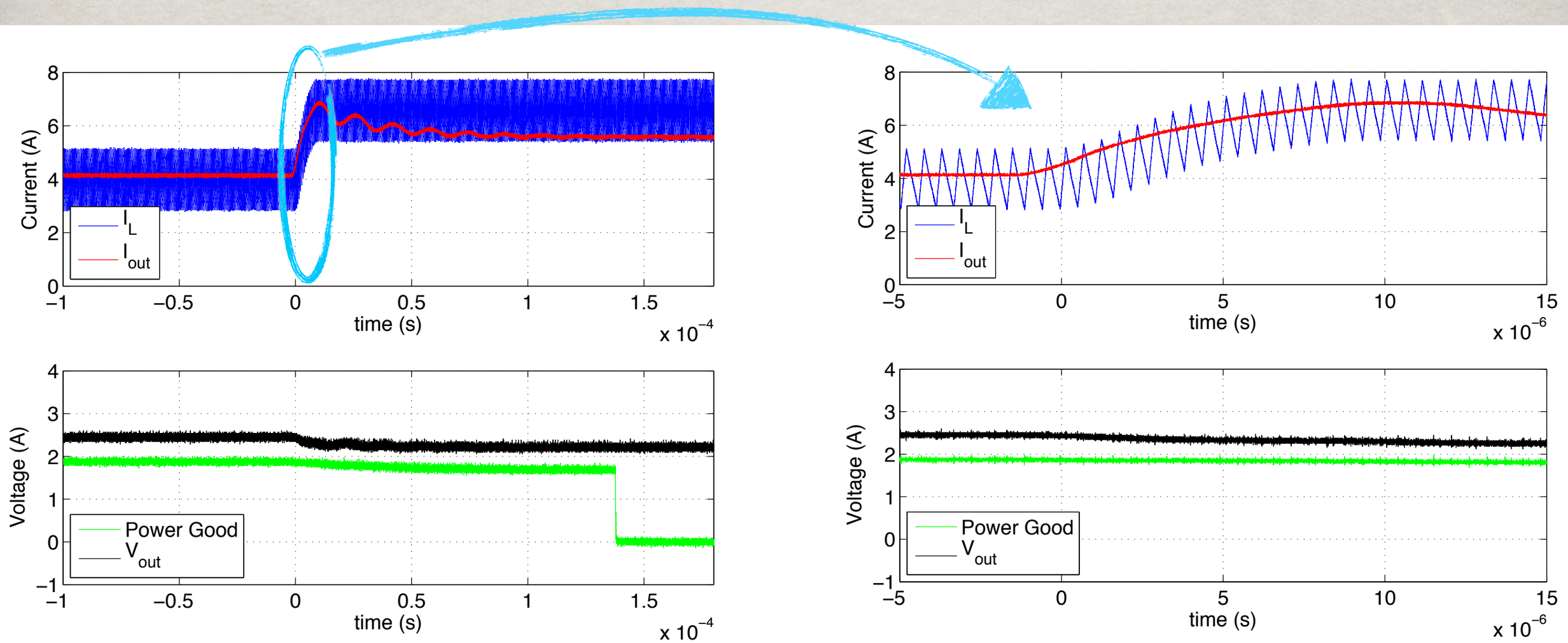


Over-Temperature



Over-current

Functionality of OCP verified in both DC and transient. The threshold is 6A and it is useful for transients, where it effectively limits the maximum current given by the converter at a cycle-by-cycle level. This has been verified with very large output current transients. In DC conditions the OTP quickly sets in.



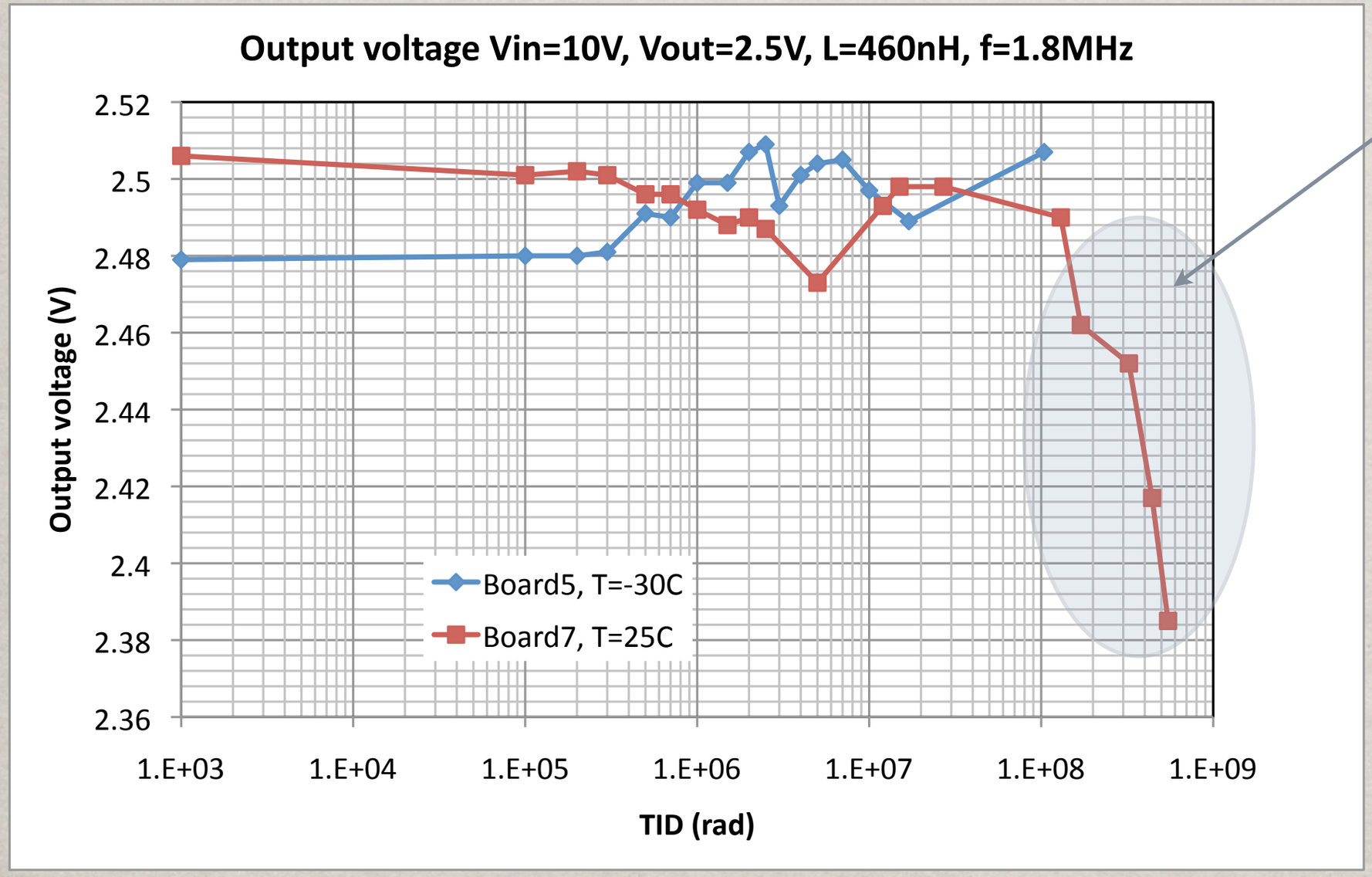
Iout transient from 4A to 7A, Vin=10V, Vout=2.5V, f=1.8MHz

Radiation test

TID test

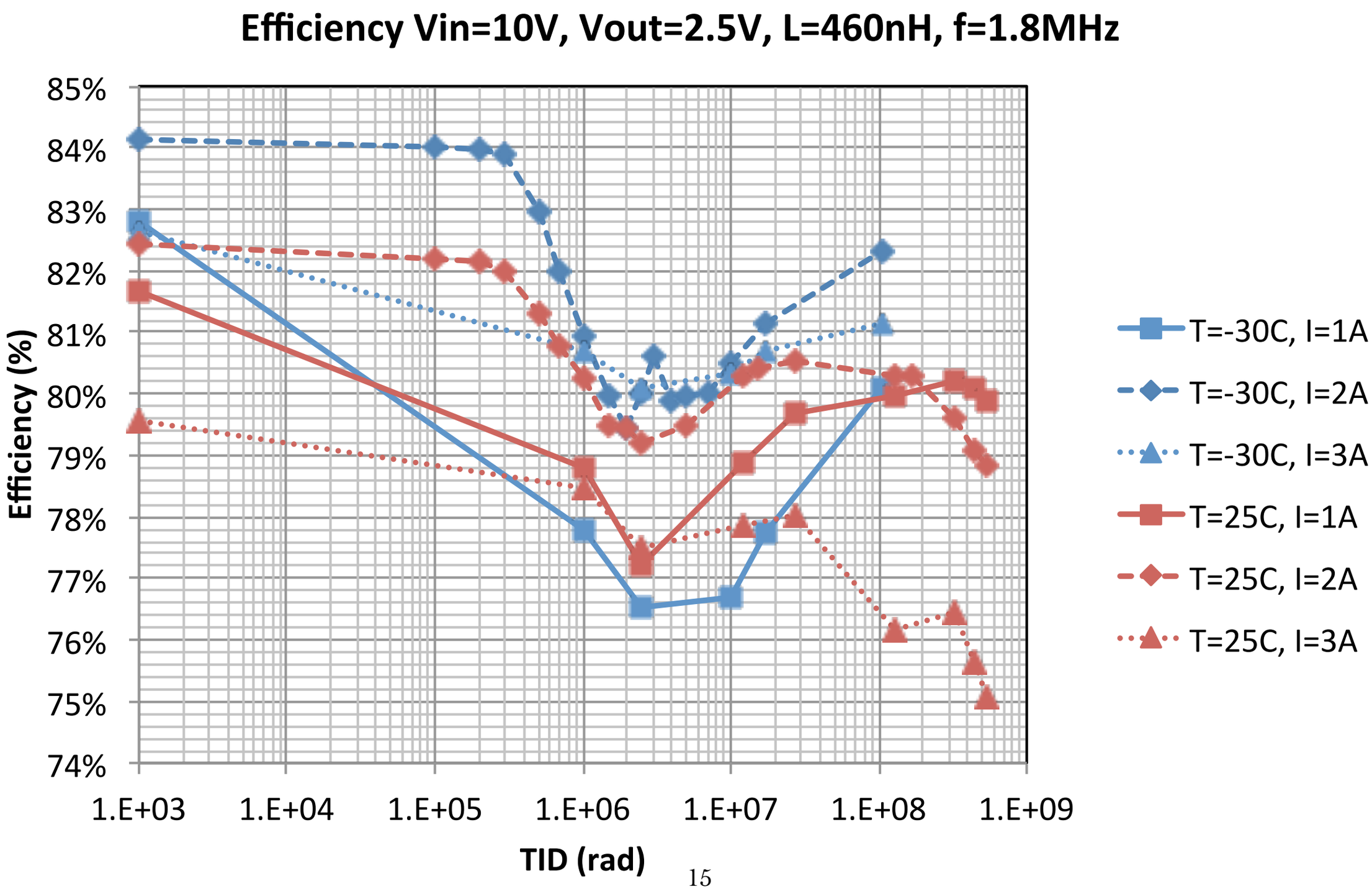
- Purpose: verify that the general TID resilience verified on AMIS5 is maintained, and that it has actually improved for a few features
- Irradiation performed at our X-ray irradiation system at controlled T (-30C, 25C) at a dose rate of 100krad/min
- Maximum TID reached: 547Mrad(SiO_2)

V_{OUT} WITH TID

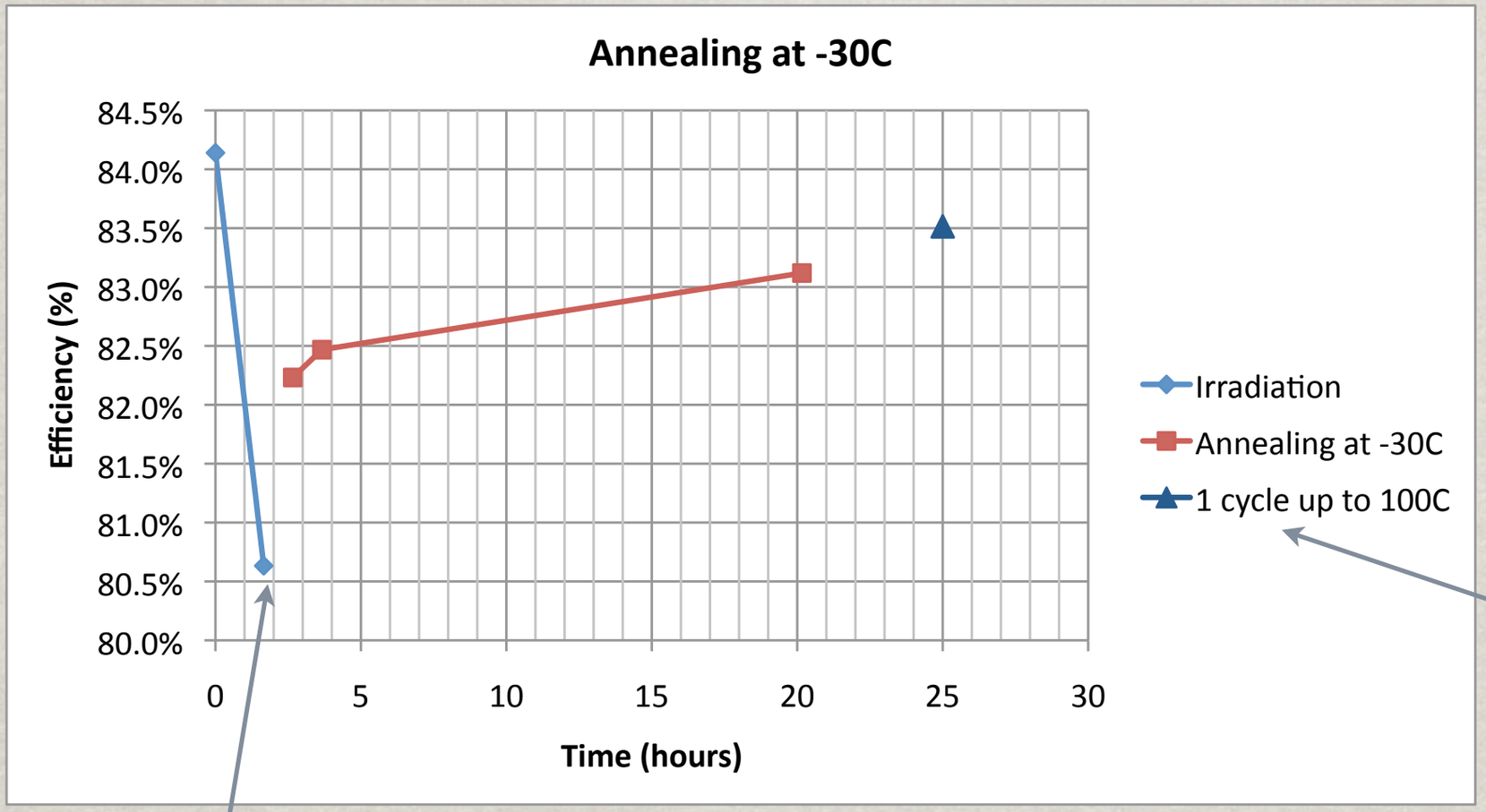


Decrease of the bandgap

Efficiency with TID



Annealing



T cycle up to 100C and down to -30C, duration about 15min

Irradiation at -30C to 10Mrad in 1h 40min

Annealing takes place quickly even at -30C!

Displacement damage tests

- Displacement damage tests have been done on AMIS5.
- AMIS5 is able to work up to 7e14 n/cm2 (1MeV Si equivalent).
- After this fluence the HV PMOS pass-transistors of the linear regulators are too degraded.
- The linear regulators present in FEAST are exactly the same of AMIS5, therefore the performances of FEAST should be comparable.
- Displacement damage test on FEAST is foreseen end 2013 - beginning 2014.

SEE test

- Measurement performed with high-penetration Heavy Ions in Louvain-la-Neuve (Be) (Cyclone accelerator at CRC-UCL)
- V_{out} and a few other nodes observed with a scope. The trigger was set as a window around nominal V_{out}
- 2 type of events observed:
  - short and low-amplitude events (less than 200mV) due to a short perturbation of the PWM. Their effect can be neglected also because the measured cross-section is low
  - 'resets' where the converter turns off and restarts (without external intervention). Overall, they last less than 1ms. In some of these events, V_{out} can start by rising above the nominal value before the converter turns completely off - it remains above nominal for some 10-15us
    - these 'resets' happen only for an LET equal or higher than $10 MeVcm^2mg^{-1}$
    - the cross-section varies with LET between 6e-7 and 7e-6 cm^2
- This indicates that the converter is potentially sensitive to SEEs in the LHC environment, and that another test has to be run to measure the cross-section in a representative radiation environment
  - an additional SEE test has been arranged at PSI (Villigen, CH), where 15 converters will be exposed to an intense beam of protons at 230MeV. Only after this test, the real sensitivity of the DCDC will be estimated

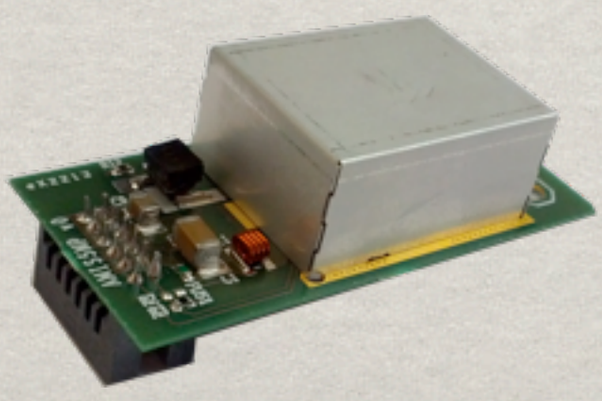
TOWARDS PRODUCTION

DC-DC modules

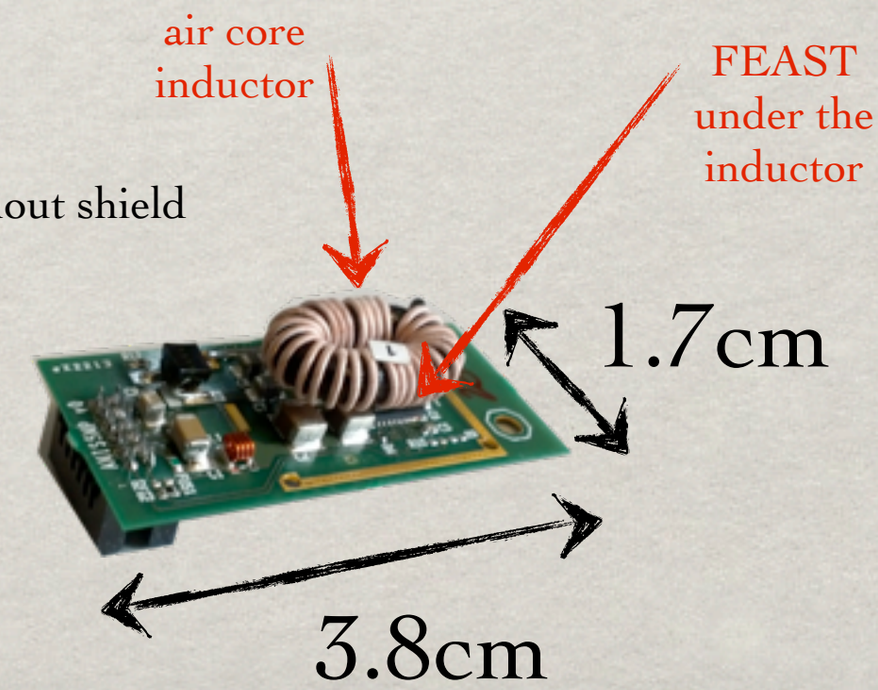
We have are going to be ready for production of ~10.000 converters in 2014.
We have defined the DCDC module layout and we are looking for passive components procurement (air core toroidal inductor).

Isaac Troyano is working on reliability test to improve the lifetime of these modules (See Isaac presentation at the power working group on Thursday 26th @ 17h00)

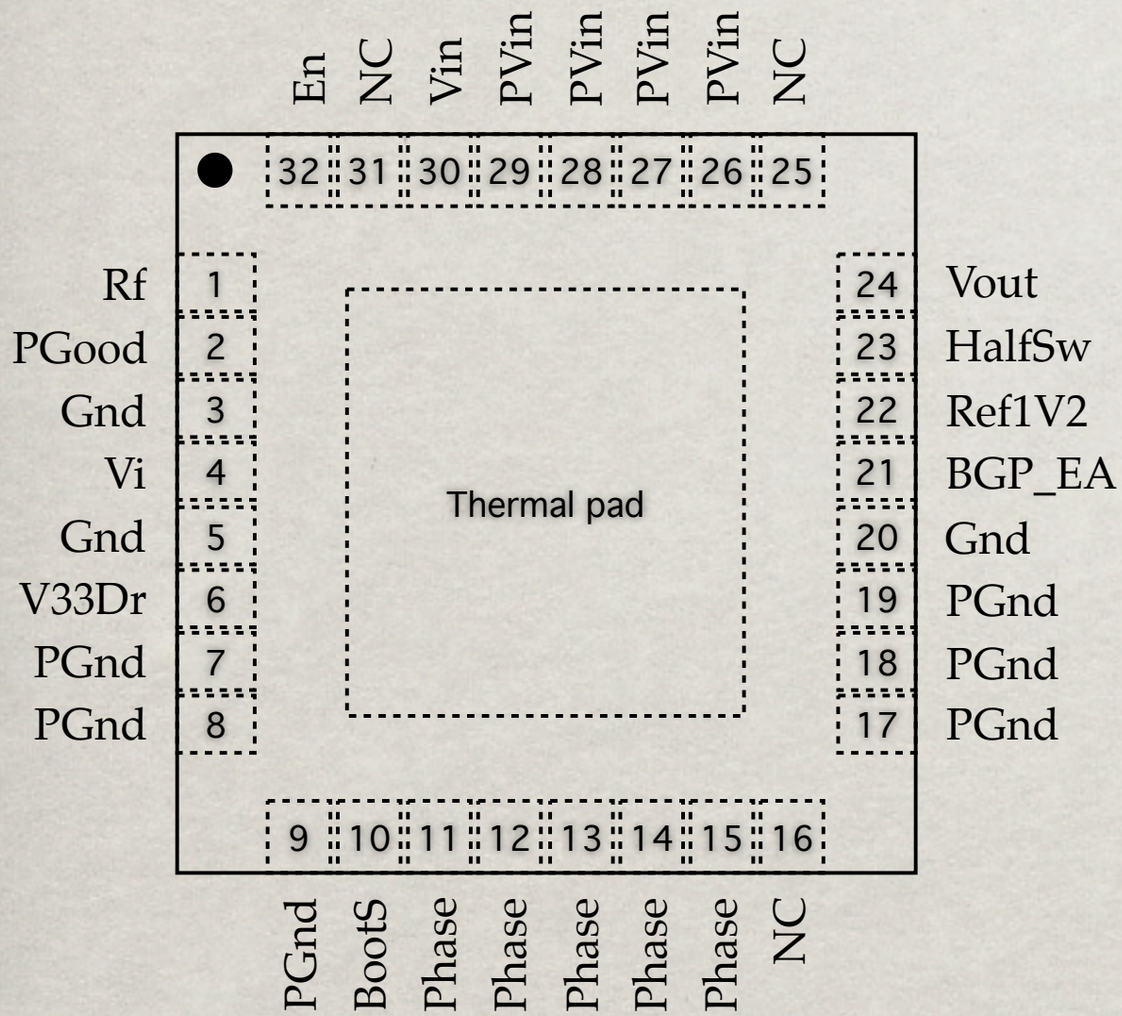
with shield

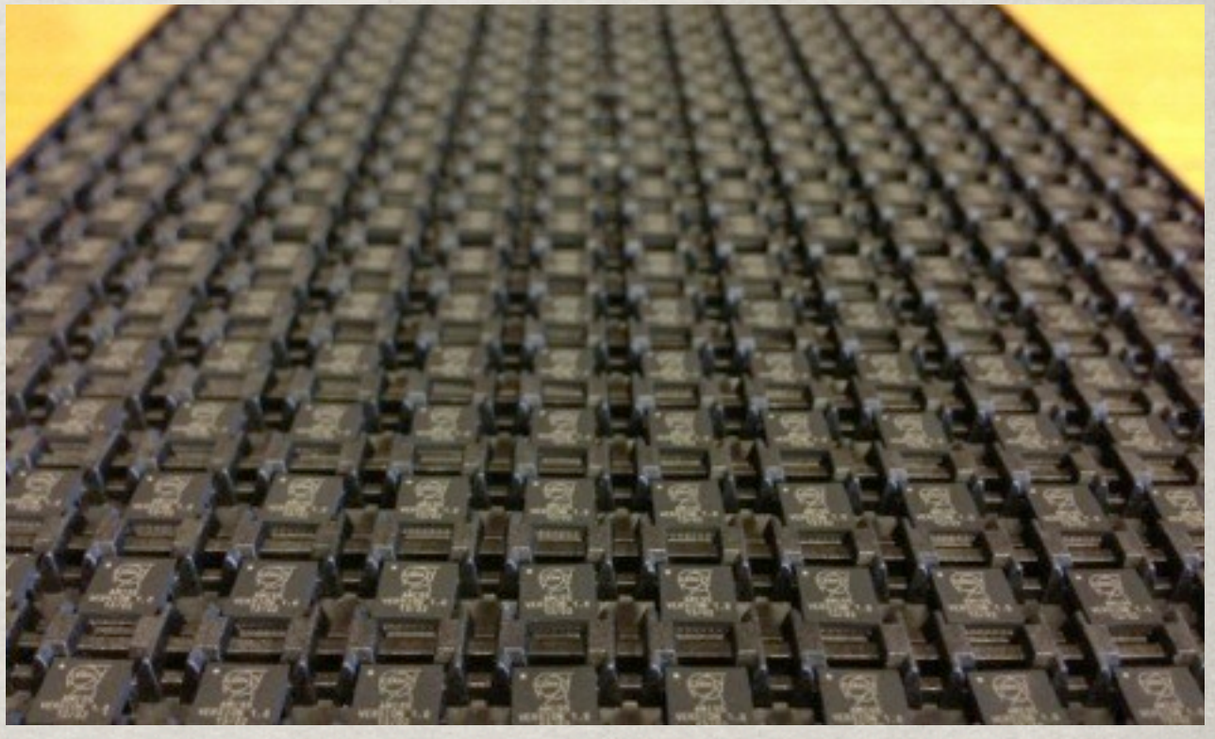


without shield



Feast Packaging

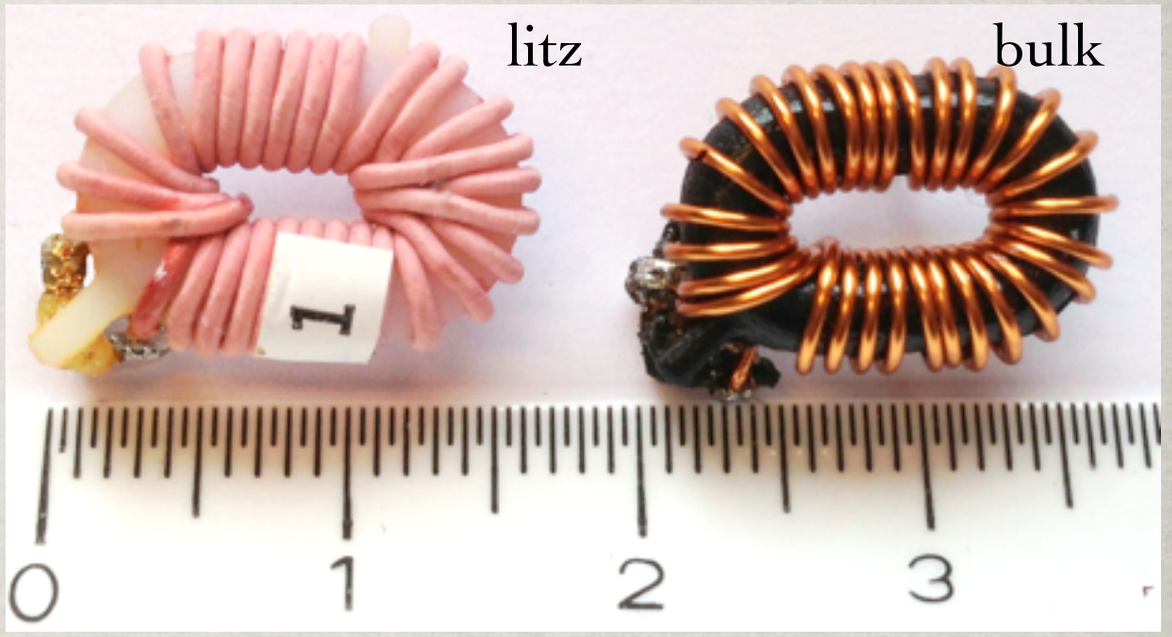


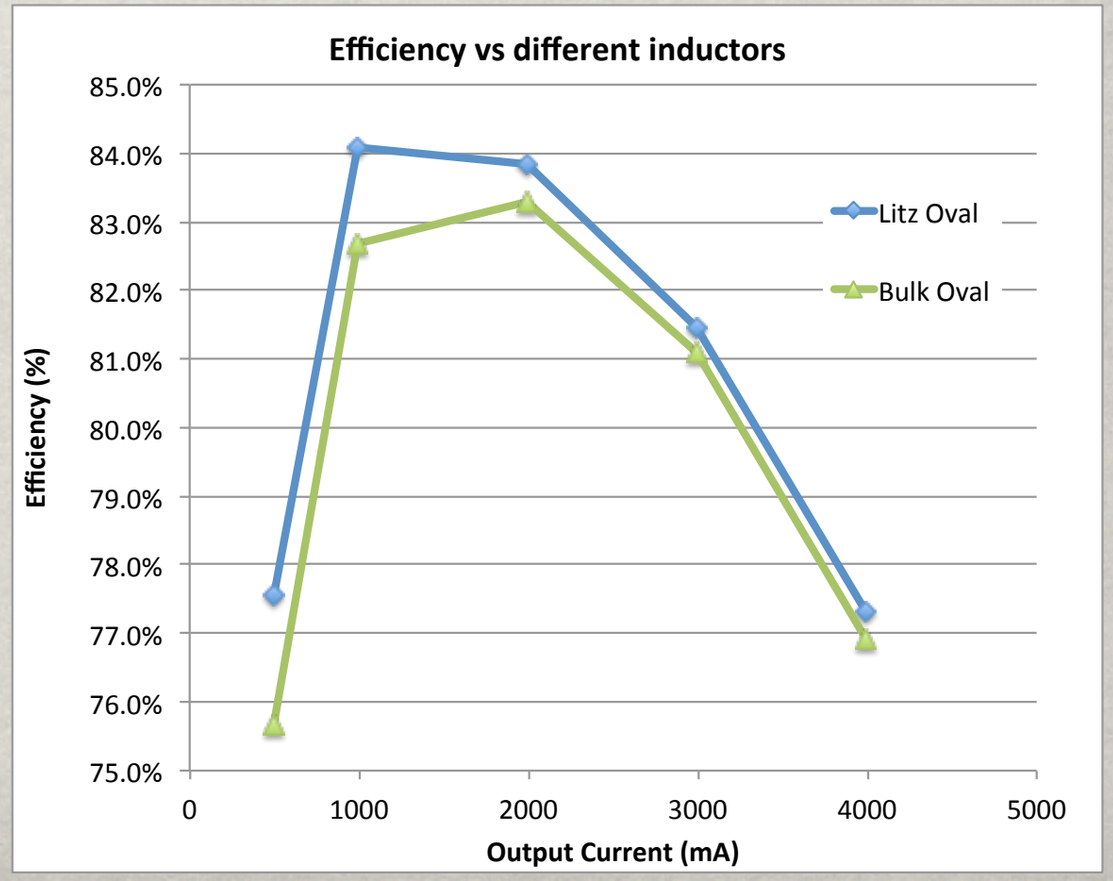


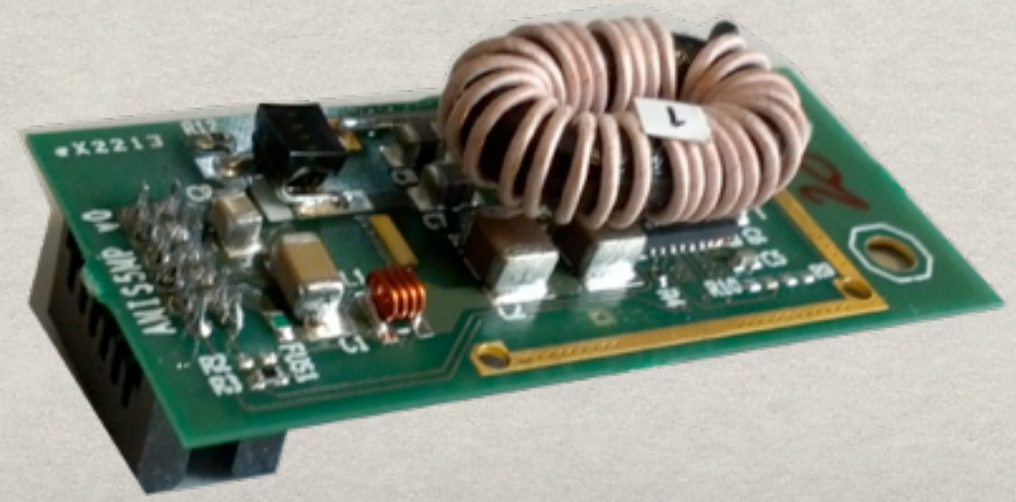
Packaging procedure started, around 4000 dies (yield not included) available in 8 weeks.

Toroidal inductor

- we are aiming to the best compromise between dimensions, cost and converter efficiency
- L=430nH as benchmark
- we are looking to the feasibility of the inductor with litz wire for mass production
- bulk=copper wire with diameter 480um
- litz=146 copper wires with diameter ~40um
- comparable DC resistance, but much lower AC resistance for the litz wire due to skin effect







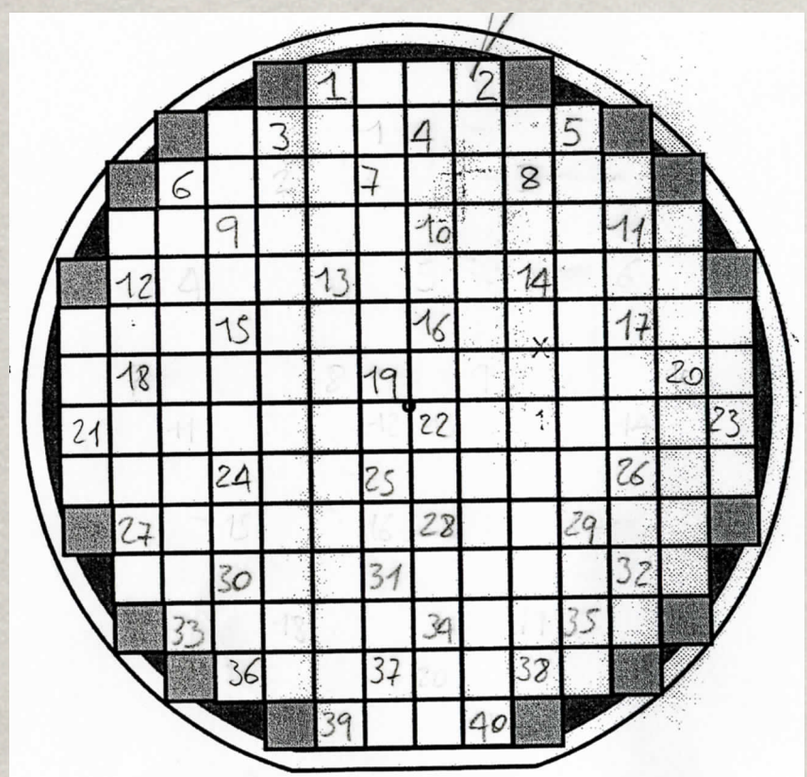
Conclusions

- FEAST ASIC is working with very good electrical performance, with efficiency higher than 80% in most of the working conditions
- All the small issues found in the previous prototype (AMIS5) have been corrected
- FEAST shows very good tolerance to TID (even up to 547Mrad)
- SEE sensitivity in LHC environment has to be determined in the proton test beam at PSI this weekend
- The DC-DC converter modules have been defined in view of production of ~10.000 sample next year
- Reliability studies and tests are on going to increase the lifetime of the modules

BACKUP SLIDES

VBG measurement

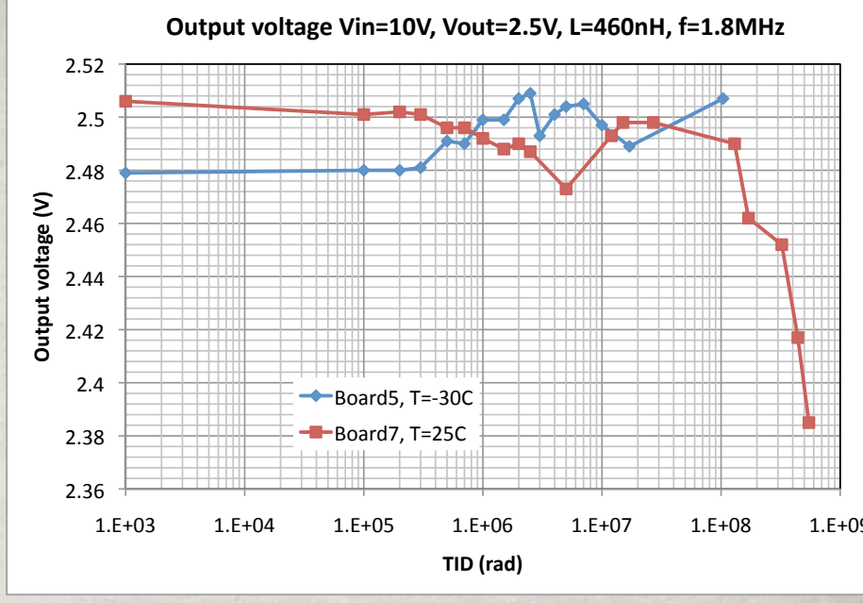
VBG has been measured on-wafer with a dedicated probe card. 40 chips have been measured in each wafer, and the average and std. deviation have been estimated.



Global average on the full lot of 6 w		
	VBGP0.6 (V)	VBGP1.2 (V)
Average	**0.597**	**1.190**
Std.Dev.	0.0044	0.0103
Minimum	0.584	1.156
Maximum	0.608	1.224

Based on these values, the resistor ratio determining the V_{out} on production-grade converter modules can be tuned to produce an average V_{out} compliant with the specification. We estimate a 6-sigma variation around the average of about ±2.5%

Line and Load regulation with TID



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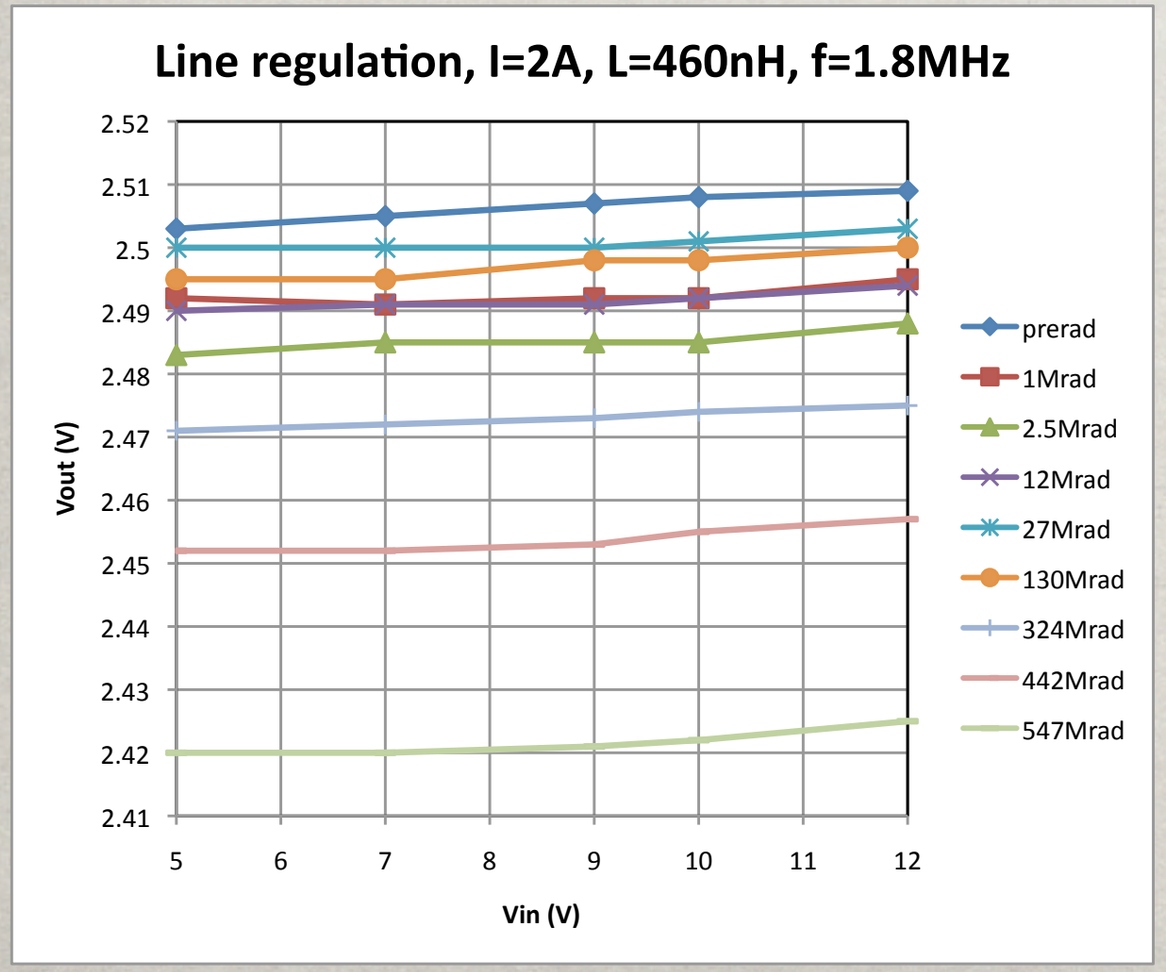

Load regulation is the capability to maintain a constant output voltage level despite changes to the output current.