A new Rad-Hard DC/DC buck converter ASIC for LHC experiment upgrades

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Power distribution with DC-DC converters

Buck Converter
Specifications
Vin<=12V
Vout=0.6-5V
Iout<=4A
frequency=1.8 MHz

Constrains:
- magnetic (2T-4T) fields
- radiation (TID>100Mrd,
  fluence < 7 \times 10^{14} \text{ n/cm}^2
  ions with LET<15\text{MeV cm}^2/\text{mg})
Some features integrated in the prototype:

- Bandgap
- 4 linear regulators: Pre-Reg, Analog, Digital and Driver
- Handling of the dead time with adaptive logic
- Improved power transistors’ design to reduce TID effects
- Possibility to enable only 2/5 of the power transistors for small Iout
- Enablers
  - Complete circuit
  - Dimension of the power transistors
- Protection
  - Over-current (OVC)
  - Over temperature (OTP)
  - Input Under Voltage Lock Out (ULVO)
- State machine for more reliable start-up procedure and handling of the signal from protection circuitry
- Power good signal if Vout is the one selected
Following the evaluation of AMIS5, circuit modifications were implemented to address all of the observed ‘problems’.

The design was completed in April tape out happened immediately. The chip has been included in an MPW in the I3T80 process where we were the only customer: all reticle available to repeat the circuit 9 times:

- Chip size: 2880 x 2800 μm²
- Number of good reticles per wafer: 148
- Total number of good chips: 1,332

Individual samples and 6 wafers (worth about 8,000 chips) delivered in mid-July.

Electrical evaluation, TID irradiation and Heavy ions SEE test performed since...
Electrical Performance
FEAST is working with very good performances.

Issues found in AMIS5 are solved:

- Vbg and frequency not affected by load
- Vout is always pulled down to gnd when chip disabled
- No problem at start-up: always a soft start
- PG appears always correct, now it is linked to Vout
- In no tested condition the converter enters an unforeseen state. It always turns off, then on again, as it should (we introduced a double threshold for Under Voltage Lock Out)
Efficiency

Conditions: cooling plate at about 18°C, L=430nH oval toroidal (bulk Cu wire), f=1.8MHz
**Regulation**

Load regulation is the capability to maintain a constant output voltage level despite changes to the output current.

Line regulation is the capability to maintain a constant output voltage level despite changes to the input voltage level.

**Conditions:** cooling plate at about 18°C, L=430nH oval toroidal (bulk Cu wire), f=1.8MHz
Protections

Input Under-Voltage lock-out

Over-Temperature

<table>
<thead>
<tr>
<th>Vin</th>
<th>t</th>
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<tbody>
<tr>
<td>3.6V</td>
<td>10</td>
</tr>
<tr>
<td>4.2V</td>
<td></td>
</tr>
<tr>
<td>4.3V</td>
<td></td>
</tr>
<tr>
<td>4.6V</td>
<td></td>
</tr>
</tbody>
</table>

FEAST
off

lin reg
on

FEAST
on

lin reg
on

FEAST
off

Temperature

<table>
<thead>
<tr>
<th>Temperature</th>
<th>t</th>
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</thead>
<tbody>
<tr>
<td>80°C</td>
<td></td>
</tr>
<tr>
<td>120°C</td>
<td></td>
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</tbody>
</table>

FEAST
on

FEAST
off

FEAST
on
Functionality of OCP verified in both DC and transient. The threshold is 6A and it is useful for transients, where it effectively limits the maximum current given by the converter at a cycle-by-cycle level. This has been verified with very large output current transients. In DC conditions the OTP quickly sets in.

I_{out} transient from 4A to 7A, V_{in}=10V, V_{out}=2.5V, f=1.8MHz
Radiation test
**TID TEST**

- **Purpose**: verify that the general TID resilience verified on AMIS5 is maintained, and that it has actually improved for a few features.

- **Irradiation performed at our X-ray irradiation system at controlled T (-30°C, 25°C) at a dose rate of 100krad/min**

- **Maximum TID reached**: 547Mrad(SiO\textsubscript{2})
Output voltage $V_{\text{Vin}}=10\,\text{V}$, $V_{\text{out}}=2.5\,\text{V}$, $L=460\,\text{nH}$, $f=1.8\,\text{MHz}$

Board 5, $T=-30\,\text{C}$

Board 7, $T=25\,\text{C}$

Decrease of the bandgap
Efficiency with TID

Efficiency $\text{Vin}=10\text{V}, \text{Vout}=2.5\text{V}, \text{L}=460\text{nH}, f=1.8\text{MHz}$

- $T=-30^\circ\text{C}, I=1\text{A}$
- $T=-30^\circ\text{C}, I=2\text{A}$
- $T=-30^\circ\text{C}, I=3\text{A}$
- $T=25^\circ\text{C}, I=1\text{A}$
- $T=25^\circ\text{C}, I=2\text{A}$
- $T=25^\circ\text{C}, I=3\text{A}$
Annealing

Annealing takes place quickly even at -30°C!

T cycle up to 100°C and down to -30°C, duration about 15 min

Irradiation at -30°C to 10 Mrad in 1h 40min
Displacement damage tests

Displacement damage tests have been done on AMIS5.

AMIS5 is able to work up to $7 \times 10^{14}$ n/cm$^2$ (1 MeV Si equivalent).

After this fluence the HV PMOS pass-transistors of the linear regulators are too degraded.

The linear regulators present in FEAST are exactly the same of AMIS5, therefore the performances of FEAST should be comparable.

Displacement damage test on FEAST is foreseen end 2013 - beginning 2014.
Measurement performed with high-penetration Heavy Ions in Louvain-la-Neuve (Be) (Cyclone accelerator at CRC-UCL)

$V_{out}$ and a few other nodes observed with a scope. The trigger was set as a window around nominal $V_{out}$

2 type of events observed:

- short and low-amplitude events (less than 200mV) due to a short perturbation of the PWM. Their effect can be neglected also because the measured cross-section is low
- ‘resets’ where the converter turns off and restarts (without external intervention). Overall, they last less than 1ms. In some of these events, $V_{out}$ can start by rising above the nominal value before the converter turns completely off - it remains above nominal for some 10-15us
  - these ‘resets’ happen only for an LET equal or higher than 10MeVcm$^2$mg$^{-1}$
  - the cross-section varies with LET between 6e-7 and 7e-6 cm$^2$

This indicates that the converter is potentially sensitive to SEEs in the LHC environment, and that another test has to be run to measure the cross-section in a representative radiation environment

an additional SEE test has been arranged at PSI (Villigen, CH), where 15 converters will be exposed to an intense beam of protons at 230MeV. Only after this test, the real sensitivity of the DCDC will be estimated
TOWARDS PRODUCTION
We have are going to be ready for production of ~10,000 converters in 2014. We have defined the DCDC module layout and we are looking for passive components procurement (air core toroidal inductor).

Isaac Troyano is working on reliability test to improve the lifetime of these modules (See Isaac presentation at the power working group on Thursday 26th @ 17h00)
Packaging procedure started, around 4000 dies (yield not included) available in 8 weeks.

![Diagram of packaging procedure](image)
we are aiming to the best compromise between dimensions, cost and converter efficiency

L=430nH as benchmark

we are looking to the feasibility of the inductor with litz wire for mass production

bulk=copper wire with diameter 480um

litz=146 copper wires with diameter ~40um

comparable DC resistance, but much lower AC resistance for the litz wire due to skin effect
Conclusions

- FEAST ASIC is working with very good electrical performance, with efficiency higher than 80% in most of the working conditions

- All the small issues found in the previous prototype (AMIS5) have been corrected

- FEAST shows very good tolerance to TID (even up to 547 Mrad)

- SEE sensitivity in LHC environment has to be determined in the proton test beam at PSI this weekend

- The DC-DC converter modules have been defined in view of production of ~10,000 sample next year

- Reliability studies and tests are ongoing to increase the lifetime of the modules
BACKUP SLIDES
Vbg measurement

VBG has been measured on-wafer with a dedicated probe card. 40 chips have been measured in each wafer, and the average and std. deviation have been estimated.

<table>
<thead>
<tr>
<th>Global average on the full lot of 6 wafers</th>
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<tbody>
<tr>
<td>VBG0.6 (V)</td>
</tr>
<tr>
<td>-------------------------------------------</td>
</tr>
<tr>
<td>Average</td>
</tr>
<tr>
<td>Std.Dev.</td>
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<tr>
<td>Minimum</td>
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<tr>
<td>Maximum</td>
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Based on these values, the resistor ratio determining the $V_{out}$ on production-grade converter modules can be tuned to produce an average $V_{out}$ compliant with the specification. We estimate a 6-sigma variation around the average of about ±2.5%
**Line and Load regulation with TID**

**Line regulation** is the capability to maintain a constant output voltage level despite changes to the input voltage level.

**Load regulation** is the capability to maintain a constant output voltage level despite changes to the output current.

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**Line regulation, V_in=10V, L=460nH, f=1.8MHz**

**Load regulation, V_in=10V, L=460nH, f=1.8MHz**