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The RCU2 - A Proposed Readout Electronics Consolidation for the ALICE TPC in Run 2

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This paper presents a proposed optimization of the ALICE TPC readout for running at full energy in the Run 2 period after 2014. During these three years an event readout rate of 400 Hz with a low dead time is envisaged for the ALICE central barrel detectors. A new component, the Readout Control Unit 2 (RCU2), is being designed to increase the present readout rate by a factor of at least 2. The immunity to radiation induced errors will also be significantly improved by the new design.

Summary

A peak luminosity of 1 to 4 x 10^{27} cm^(-2)s^(-1) for Pb-Pb collisions is expected during the Run 2 period between Long Shutdown 1 and Long Shutdown 2 of the Large Hadron Collider. To take full advantage of these running conditions, an event readout rate of 400 Hz with low dead time of the experiment has been envisaged for the ALICE central barrel detectors, assuming a typical mix of trigger conditions. The readout rate of the current readout electronics saturate for central Pb-Pb events at about 320 Hz with 100% dead time, so actions must be taken to meet the demands of Run 2. Additionally, stability problems due to radiation effects have been observed in Run 1. These are expected to be worse with the increased energy and luminosity in Run 2.

The current Time Projection Chamber (TPC) readout electronics consist of 4576 Front End Card (FECs) that are read out by 216 Readout Control Units (RCUs). One RCU connects to a maximum of 25 FECs via two branches of a wide multidrop parallel bus. The RCU consist of a motherboard that hosts two mezzanine cards, The Detector Control System (DCS) card and the Source Interface Unit (SIU). The DCS card interfaces the DCS by Ethernet and the Trigger, Timing and Control (TTC) system via an optical interface. The SIU connects optically to the Data Acquisition (DAQ) System using the Direct Data Link (DDL) protocol. The bottleneck of the current readout electronics is the multidrop parallel bus between the FECs and the RCU.

In order to meet the requirements of Run 2 a new Readout Control Unit, the RCU2, will replace the present RCU board. The RCU2 will improve the readout-scheme such that the maximum readout rate of the TPC can at least be doubled, while also decreasing the susceptibility to radiation related errors. The RCU2 will host a MicroSemi Smartfusion2 FPGA. This is a state-of-the-art flash-based System-on-Chip (SoC) FPGA that promises very high radiation tolerance. Given the tight schedule, the architecture and infrastructure surrounding the RCU2 is left untouched. This imposes strict constraints to the design. For instance, the RCU2 must be housed in the same location as the present RCU, and the connection to the DCS, TTC and DAQ must be done reusing the existing cabling. The RCU2 will connect the same number of FECs as the current RCU, but by using four branches instead of two. By utilizing the increased parallelism in the FPGA design, as well as upgrading to the 5 Gbps DDL2 protocol, early calculations show that an increase in the readout rate by a factor of approximately 2.6 can be achieved.

The first prototype of the RCU2 is estimated to be ready later this year and the goal is to have the final design ready for mass production by spring 2014. This paper will give an overview of the RCU2, and a special focus will be given to the actions taken to increase the data rate and improve the radiation tolerance of the design.

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