FPGA-based, radiation-tolerant on-detector electronics for the upgrade of the LHCb Outer Tracker Detector

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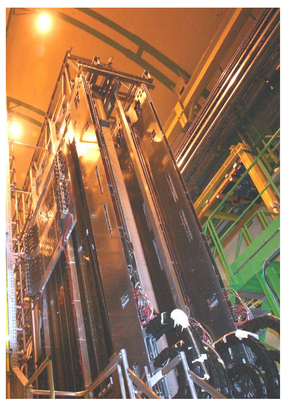
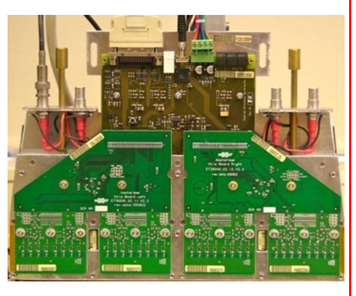
Outer Tracker Detector

An array of 54,000 straw tubes covering an area of 5x6m^2 with 12 detection layers, provides the accurate drift-time to the tracking system of the LHCb spectro meter.



Detector Module

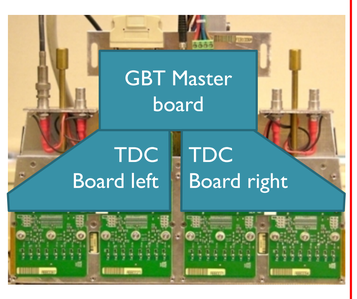
One detector module packs 128 straw tubes. The on-detector electronics is hosted in 432 Front end-Boxes. Each Front end box is a modular system consisting of 8 ASDBLR, 4 OTIS and 1 GOL boards.



Upgrade

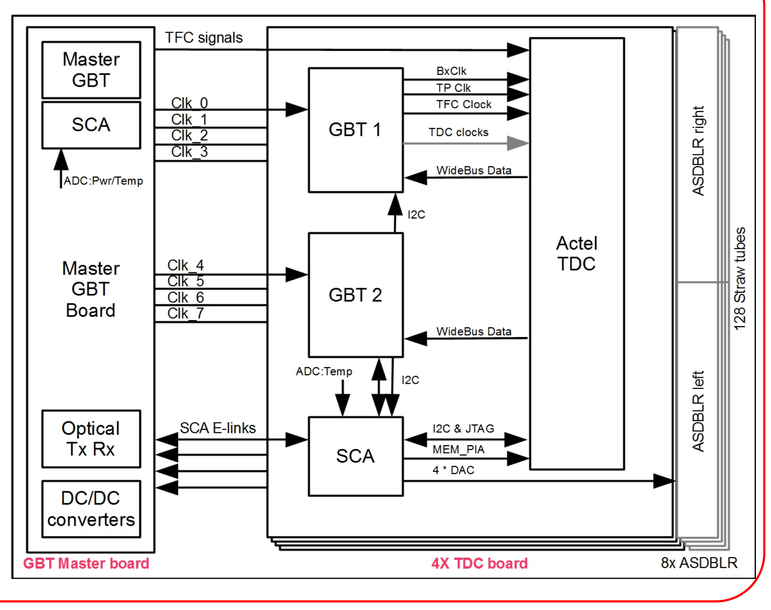
Upgrade based on FPGA's, a highly configurable on-detector solution
Two different proto-types are developed

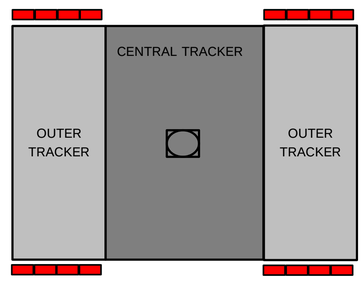
- One based on the Altera Arria GX family, including high speed serial devices
- The second based on The Actel Proasic3E family in combination with external GBT serial tranceivers(showed on this poster).



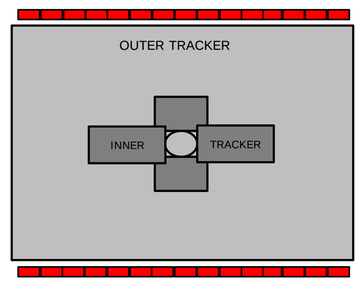
Front-End box

- One master GBT board with GBT for TFC and ECS. Power, versatile link optics, Bidir. and dual Tx or 12-way Tx.
- Four TDC boards with two wide-bus format data GBT's, SCA and Actel A3PE1500-FG484 FPGA.
- 8 ASDBLR boards, unchanged in Upgrade.





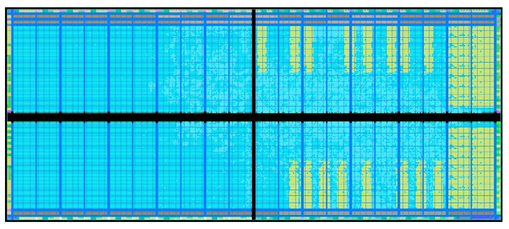
1) "Old" straw-tube modules + SciFi CT

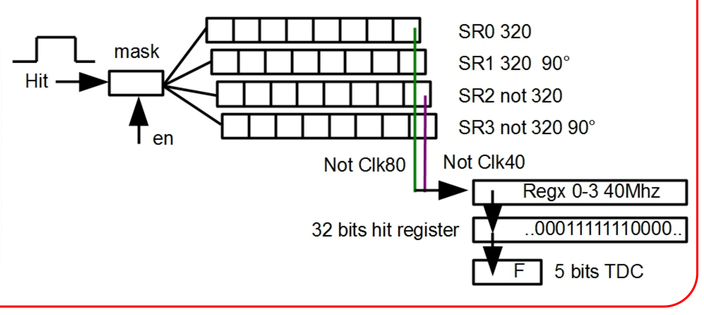


2) "Old"+"New" straw-tube modules + Si IT

FPGA based TDC

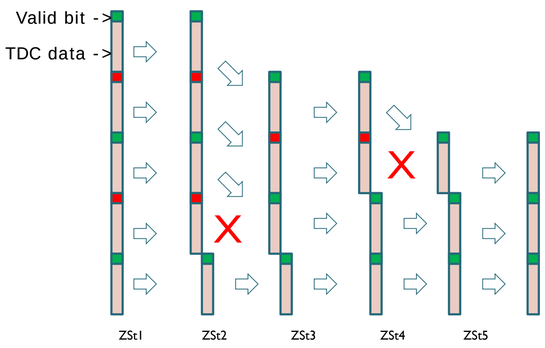
- 5 bits TDC which converts the drift time from Amplifier Discriminator Baseline Restoration asic (ASDBLR) output straw tube signal to a digital time value.
- 32 TDC channels with ~780 ps resolution.
- Three types with fixed placement used, Top right and Bottom. Usage depends on FPGA pin location. TDC registers placement are fixed to force constant delay times.





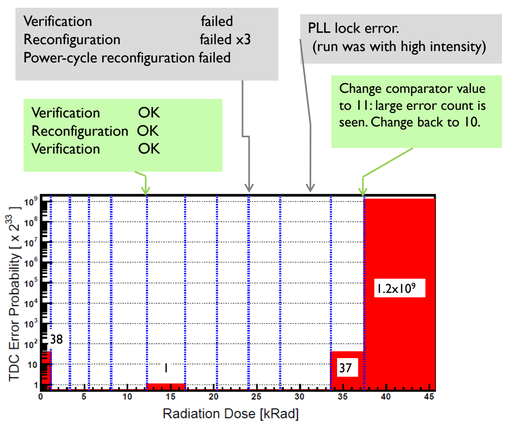
Zero suppression

- To decrease the bandwidth needs the data is zero suppressed.
- The ZS algorithm has a constant latency.
- Two variants used, 2x16 channels or 1x32 ch.
- 16/32 bits Hit pattern.



Irradiation tests

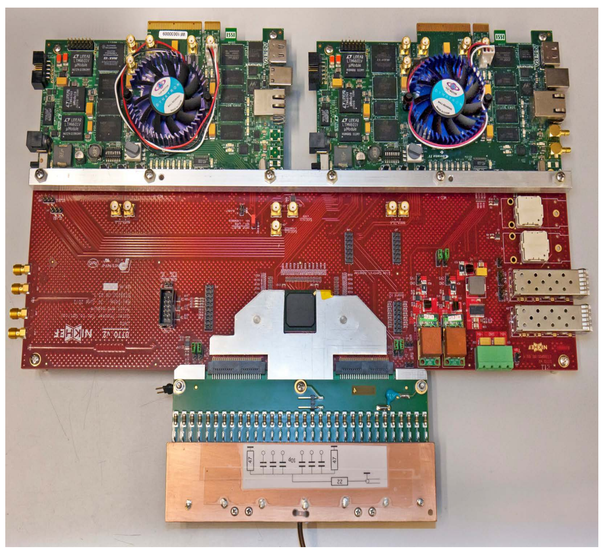
- At worst location, estimate ~7.2 krad for 50 fb^{-1} [1]
- Adopting a factor 2 safety for the simulation uncertainty and another factor 2 safety for the FE irradiation tests: ~30 krad
- Results from Actel irradiations from Syracuse group. [2]



Preliminary results of the PLL irradiation test [3,4]

- Programmable up to ~17 krad
- still functioning until ~30 krad, then high current and malfunction.
- RAM: few SEU every 3min run (few krad per run).
- After irradiation, all chips fail firmware verification and reconfiguration, but they still seem to function as TDC's
- Hardly any PLL lock lost.
- Few TDC errors up to ~30 krad, then TDC values seem to "shift".

Proto-Types

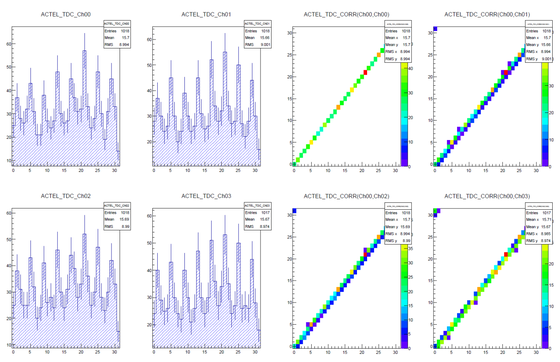


Prototype ¼ Front end box: 32 TDC Channel inputs, 2 GBT data outputs. Based on on-detector electronics

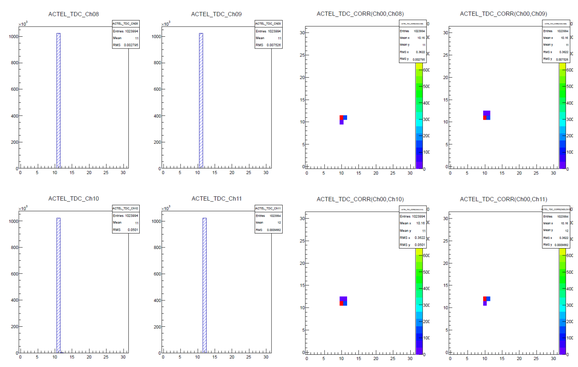
- OTTO (Outer Tracker TDC to Optical)
  - Actel 32 Channel 5 bits TDC's.
  - Various options for optical Tx/Rx.
  - Various options for control.
- Two Altera StratixIV FPGA's
  - TFC: BcntRst, Sync, CLk's.
  - Readout Actel 28 bits @ 160 MHz.
  - DDR3 buffering of Actel data.
  - DDR3 ⇒ Linux via TCP/IP.

Measurements & results

Random puls

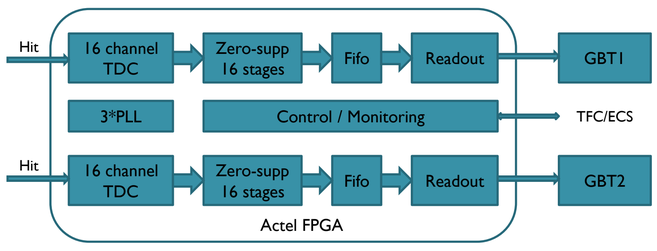


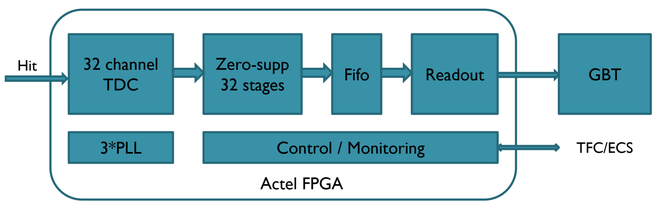
Fixed puls



Bandwidth considerations

- **100% Occupancy**
- Two data paths with each 16 channel TDC, 16 stages zero suppression double GBT's.
- **37% Occupancy**
- One data path with 32 channel TDC, 32 stages ZS on readout path to GBT serializer.





References :
[1] M. Karacson, Talk at LHCb upgrade Electronics meeting 14/Feb/2012
[2] Syracuse University: M. Artuso, E. Cowan, Bin Gui, D. Hsu, R. Mountain, JC Wang
[3] R. Mountain, Talk at LHCb electronics upgrade meeting 14/Oct/2010, 21/Jul/2011
[4] J.C. Wang, Talk at LHCb electronics upgrade meeting 14/Feb/2012