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FPGA-based, radiation-tolerant on-detector electronics for the upgrade of the LHCb Outer Tracker Detector

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The LHCb experiment studies B-decays at the LHC. The Outer Tracker straw tubes detects charged decay particles. The on-detector electronics will be upgraded to be able to digitize and transmit drift-times at every LHC crossing without the need for a hardware trigger. FPGAs have been preferred to application-specific integrated circuits to implement dead-time free TDCs, able to transmit data volumes of up to 36 Gbits/s per readout unit, including the possibility of performing zero suppression. Extensive irradiation tests have been carried out to validate the usage of field-programmable devices in the hostile environment of the LHCb tracking system.

Summary

The LHCb experiment is redesigning its readout and data-acquisition system: the on-detector electronics will no longer receive a trigger, but will instead ship all data to be buffered and selected through a full physics reconstruction. The Outer Tracker detector, an array of 54,000 straw tubes covering an area of 5x6 m2 with 12 detection layers, provides accurate drift-time to the tracking system of the LHCb spectrometer. The digitization is performed by the on-detector electronics, which then serializes and optically transmits the data. A detector module packs 128 straw tubes (2.4m long and 4.9mm diameter). In the high track-density environment of LHC, the challenge of an accurate and dead-time-free digitization of a 5-bits drift-time is combined with that of the trigger-less transmission of up to 36 Gbits/s from each on-detector readout unit.

To meet these challenges, we have developed a system combining the ability to perform time-to-digital conversion at each LHC clock cycle in a dead-time-free fashion, with that of selecting only data from channels with valid hits(zero-suppression) to reduce the data volume to the counting house. Our technological choice fell on field-programmable devices rather than ASICs; this allowed us to develop a highly-configurable on-detector electronics: one
can vary the data size and the number of channels per circuit, perform zero-suppression, data spying and histogramming, etc. Our R\&D provided two solutions: one based on the Altera Arria GX family, including high-speed serial devices, and the other on the flash-based Actel (now Microsemi)ProAsic3 family in combination with external serial transceivers from the GigaBit Transceiver (GBT) project. This contribution focuses on the Actel-based implementation. A 32-channels TDC core has been implemented in an
A3PE1500-FG484 (using roughly 40% of core resources): the 25ns period of the LHC clock is divided in 32 time bins obtained from the outputs of four 320 MHz phased-locked loops (two edges, shifted in phase by 90 degrees); data from four 8-bits shift-registers are combined into a 32-bits hit-register, then translated into a 5 bits drift-time. Zero-suppression is performed before data is stored in an output fifo, scrutinizing one channel per clock cycle and
producing a hit-pattern word. Our design has been implemented and tested in prototypes of the on-detector electronics (including an FPGA-based emulator of the GBT). Pulses resembling our detector signals have been injected to verify the TDC response and data integrity after zero-suppression. Integral and differential linearity have been measured and the dead-time-free performance verified.

We expect the hottest spot of our on-detector electronics to absorb a dose of about 1.5 Gray for each inverse femtobarn of integrated luminosity. The performance of A3PE1500 FPGAs has been studied in a series of dedicated irradiation tests, including a specific test of the PLL performance, demonstrating that our system remains operational up to about 300 Gray (30 krad). Although this is sufficient for our application, we are

also investigating the performance of the newest SmartFusion line of Microsemi FPGAs, which is expected to be considerably more radiation tolerant and is a viable alternative for our design.

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