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Power pulsing schemes for analog and digital electronics of the vertex detectors at CLIC

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The precision requirements of the vertex detector at CLIC impose strong limitations on the mass of such a detector (<0.2% of X0 per layer). To achieve such a low mass, ultra-thin hybrid pixel detectors are foreseen, while the mass for cooling and services will be reduced by implementing a power-pulsing scheme that takes advantage of the low duty cycle of the accelerator. The principal aim is to achieve significant power reduction without compromising the power integrity supplied to the front-end electronics. Voltage and current based power-pulsing schemes are proposed and their electrical features are discussed on the basis of measurements.

Summary

The vertex detector is the innermost detector at the proposed CLIC linear electron-positron collider. It is composed of several layers of pixel sensors and readout ASICs. In the central section the layers are arranged in "ladders". The precision physics requirements limit the material budget for sensors, readout, support, cooling and cabling to less than 0.2% of a radiation length (X0) per detection layer. The power consumption of the readout electronics strongly impacts the required low material budget of the detector. To reduce the cable and cooling material, the average power per unit area has to be small (<50 mW/cm2). Collision at CLIC will occur in bunch crossings every 0.5 ns during a bunch train of 156 ns. The time between consecutive trains is approximately 20 ms. The readout ASICs can then be active during a time window containing the bunch train and remain idle in the other part of the cycle, thus reducing the average power. The use of the beam duty cycle to reduce the average power is known as power pulsing.

The use of a power pulsing scheme implies that the ASIC current consumption has to change suddenly from its idle value (few hundreds of mA) to full load (more than 40 Amps for a single ladder composed of 24 ASICs) within a few microseconds, then remain constant for enough time to record and process the events (few tens of microseconds) and finally drop back to the idle current value. During the bunch train, the power consumption is at its maximum and constant, and the supplied voltage has to remain within 5% of the nominal voltage in order to allow for a correct functioning of the readout ASICs. The latter is particularly challenging, considering the big transient that takes place before the readout process.
The analog and digital components of the ASICs have different constraints and therefore will be powered separately.

A dummy load emulating the power consumption of the analog electronics of half a ladder and a power-pulsing scheme based on a voltage source to power the analog circuitry of the ladder were presented at TWEPP 2012. The scheme consisted of DCDC converters placed 30 cm away from the ladder, charging storage silicon capacitors placed in the ladder through low mass flex cables. Low dropout regulators (LDOs) in the ladder provided local voltage regulation to each readout ASIC. The proposal was validated through simulations and measurements of prototypes, with an estimated contribution to the material budget of the ladder of 0.145 % of X0.

A power-pulsing scheme based on a controlled current source made it possible to further decrease the material contribution to 0.06% of X0 and to remove the need for DCDC converters along the powering path. It consists of a controlled back-end current source that charges the silicon capacitors in the ladder with low current during the idle time. In this way, the charging current is dramatically reduced to less than 100 mA for a whole ladder. A prototype of this back-end current source was implemented using an FPGA. A dummy load

emulating the power consumption of the digital components is currently being implemented. It will be used to compare the performance of both power-pulsing topologies.

The talk will introduce the requirements and the proposed powering schemes and present simulations and prototype measurement results of the performance for both the digital and analog components.

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