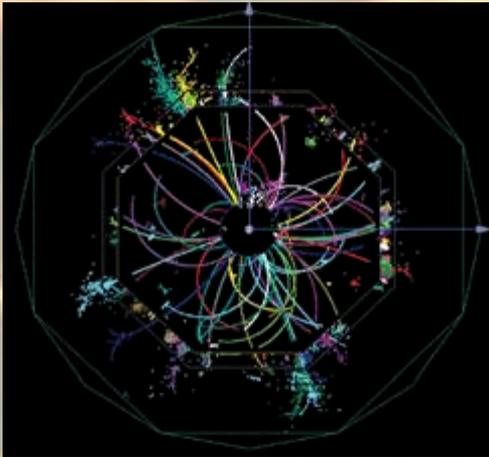


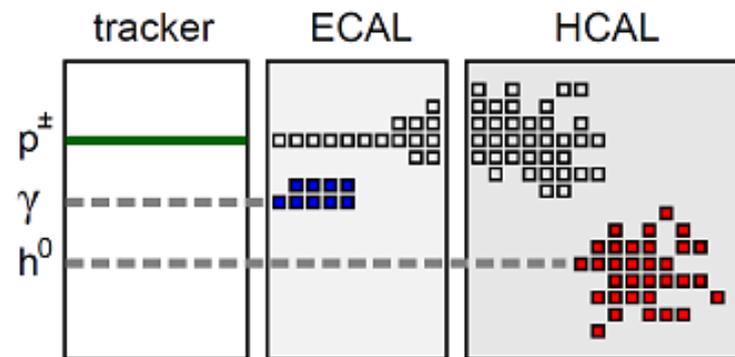
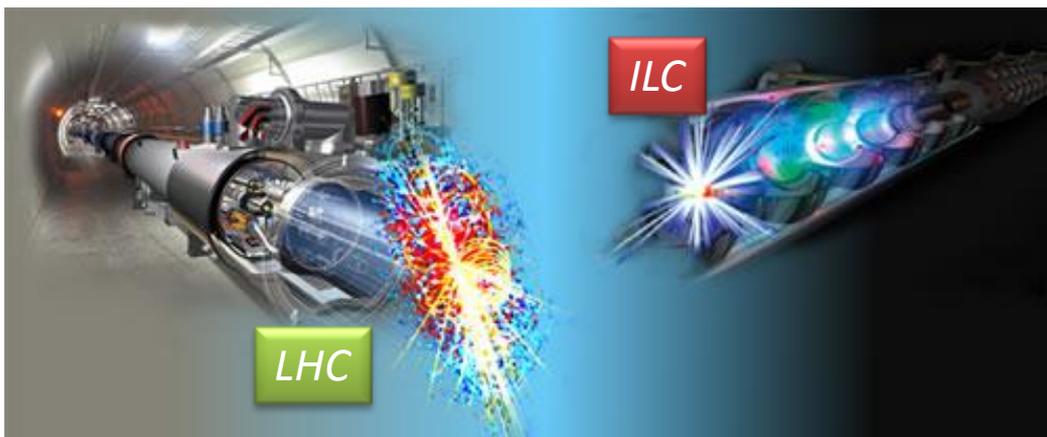
ROC chips for imaging calorimetry at the International Linear Collider



PERUGIA, TWEPP 2013

Nathalie Seguin-Moreau on behalf of OMEGA microelectronics group

IN2P3-CNRS, Ecole Polytechnique, Palaiseau (France)

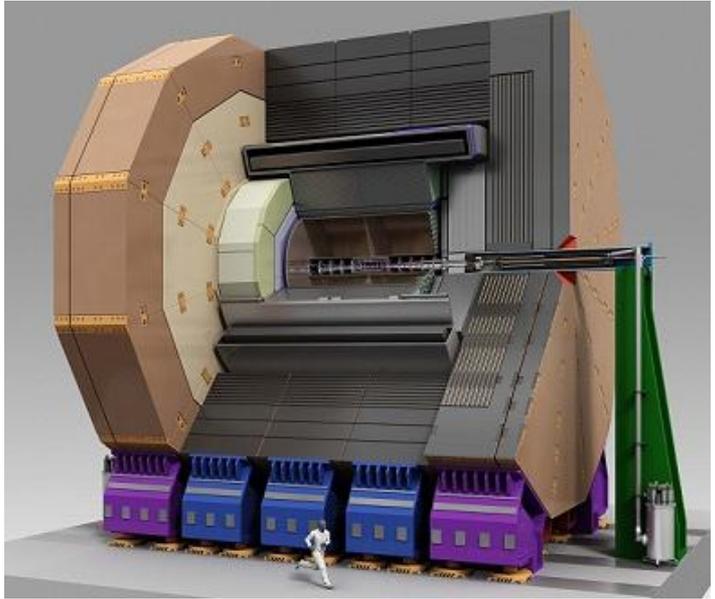


Imaging calorimetry at the International Linear Collider

- ⇒ New detectors with one hundred million channels, “calorimetry grade”
- ⇒ Readout electronics: must be highly integrated (System On Chip) and ultra low power to be embedded inside the detectors
- ⇒ Readout ASICs: HARDROC, MICROROC, SPIROC and SKIROC in SiGe 350 nm technology (AMS) by OMEGA group (CNRS-Ecole Polytechnique)



ASICs for ILC prototypes

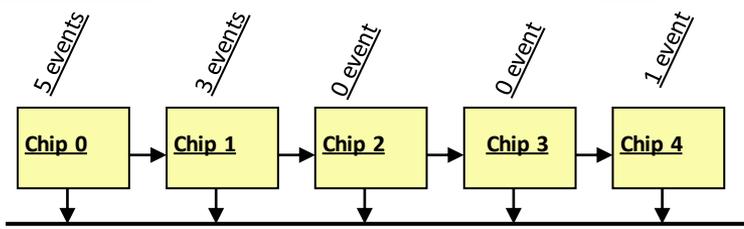


❑ 1st generation ASICs: FLC-PHY3 and FLC_SiPM (2003) for **physics prototypes**

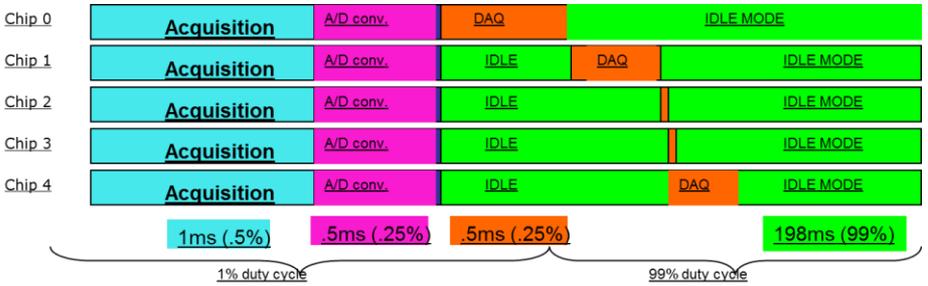
❑ 2nd generation ASICs: ROC chips for **technological prototypes**



- ✓ Address integration issues
- ✓ Auto-trigger, analog storage, internal digitization, power pulsing
- ✓ Readout architecture **common to all calorimeters** and **minimization of data lines & power**
 - ✓ **Daisy chain** using token ring mode
 - ✓ Open collector, low voltage signals
 - ✓ Low capacitance lines



Data bus



❑ 3rd generation ASICs (AIDA funded)

- ✓ **Independent channels to perform Zero suppress**



SKIROC2 for ECAL readout

- ❑ « Imaging » calorimetry for « particle flow algorithm » => 30%/√E jet resolution

- ✓ **High granularity and segmentation of the calorimeters**



- ❑ **Si W Calorimeter**

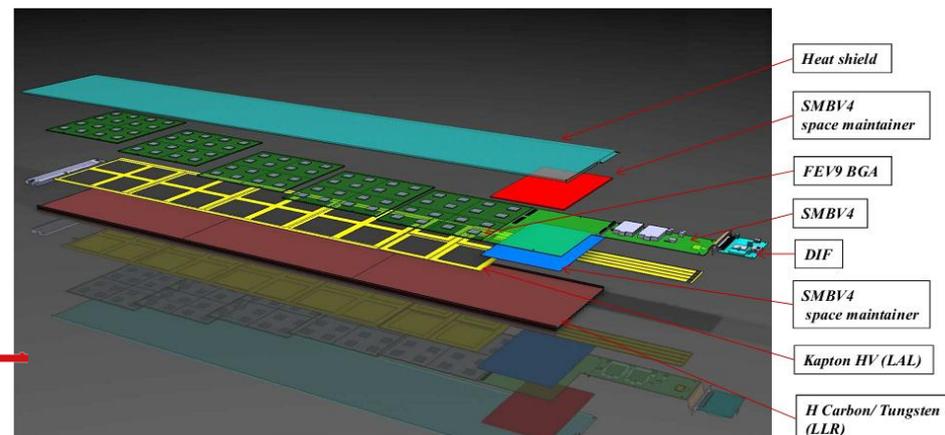
- ✓ **Active medium: SILICON SENSORS (WAFERS)**

- ✓ 325μm thick Silicon Wafers => 25000e⁻/MIP ie 1MIP=4 fC

- ✓ High granularity : 5x5 mm²

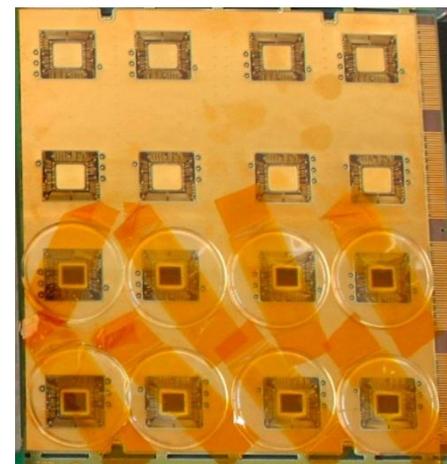
Agence Nationale de la Recherche
ANR
CALIIMAX-HEP

- ✓ High segmentation: **45 000 cells with embedded electronics for the technological prototype**



LAL
LABORATOIRE
DE L'ACCÉLÉRATEUR
LINÉAIRE

 **AIDA**



- ❑ Final ECAL: 30 layers, **100 M channels**

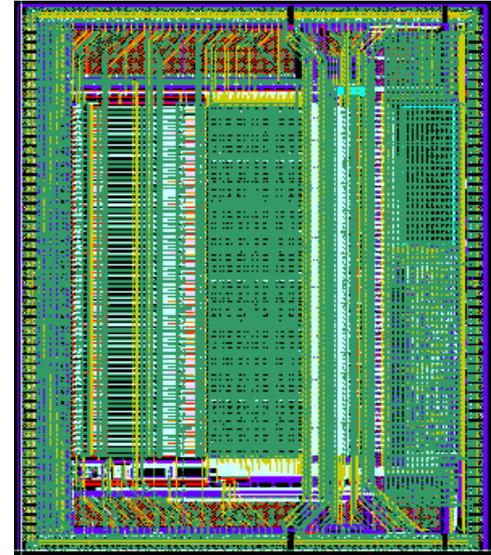
- ✓ **SKIROC2 embedded** inside the detector, **No (few) external components**

- ✓ **Front End boards: crucial element**

- ❑ Stitchable motherboards (Active Sensor Units)
- ❑ Minimize connections between boards

SKIROC 2 main features

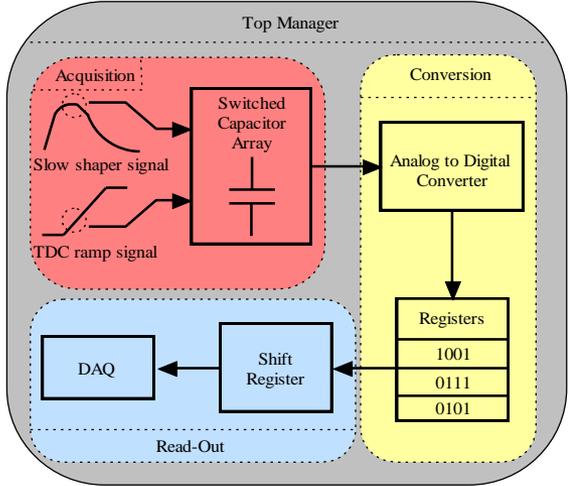
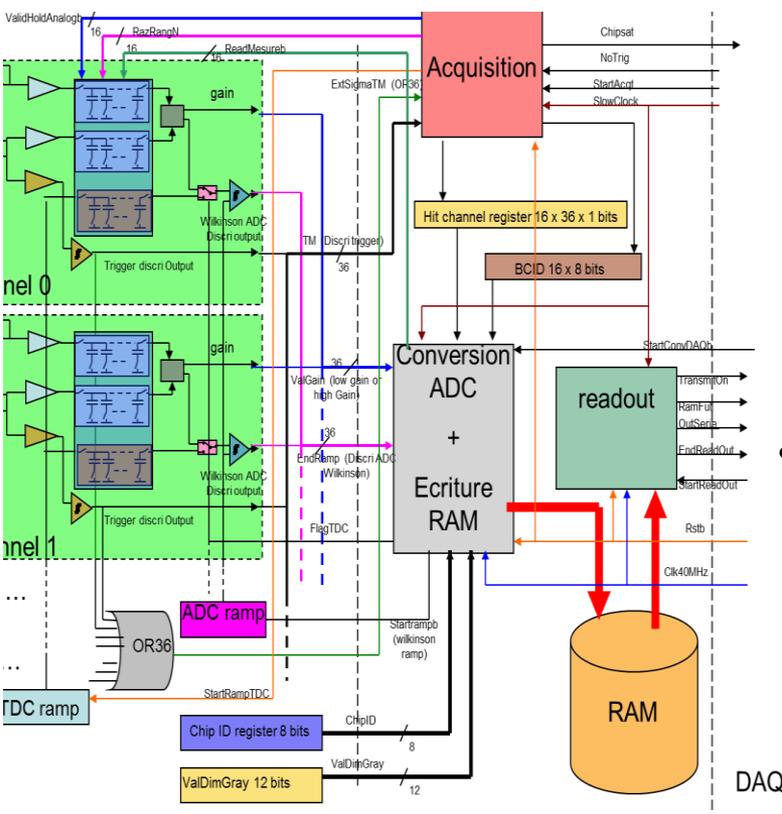
- Energy measurement : 14 bits
 - 2 gains (1-10) + 12 bit ADC: **1 Mip (4fC) → 2500 Mip (10pC)**
 - Variable shaping time from 50ns to 100ns
 - Mip/noise ratio > 10
- Auto-trigger on 1/2 MIP (2 fC)
 - MIP/noise ratio on trigger channel >10
 - Fast shaper : ~30 ns
 - Auto-Trigger on ½ MIP
- Time measurement :
 - 12-bit Bunch Crossing ID + 12 bit TAC step~100 ps
- Analog memory for time and charge measurement : depth = 15
- 12 bit-ADC, 4k internal memory
- Daisy chain readout
- Low consumption : ~25 μ W per channel (in power pulsing mode)



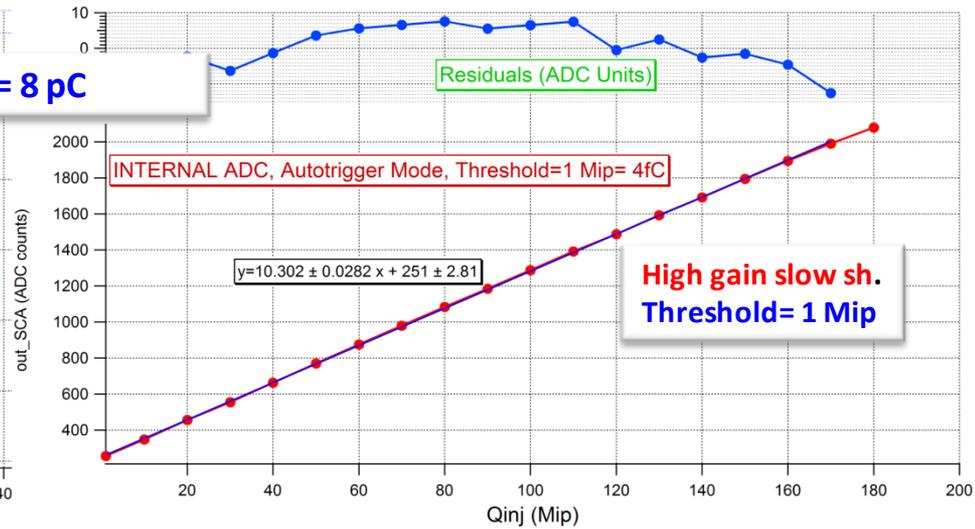
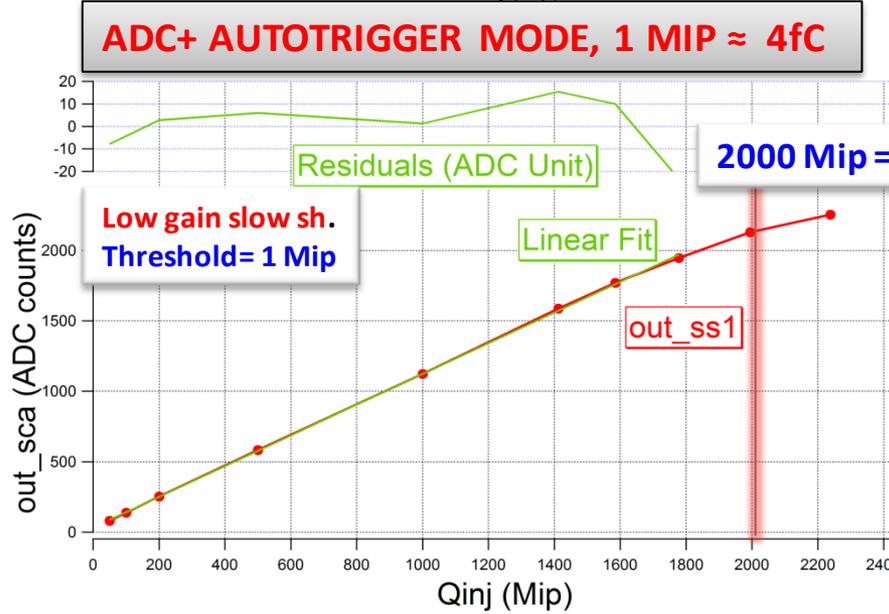
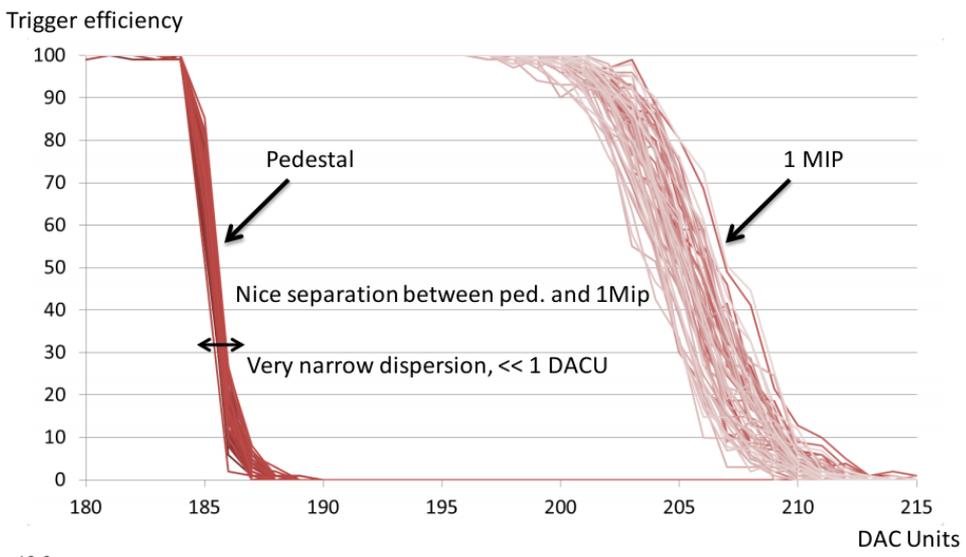
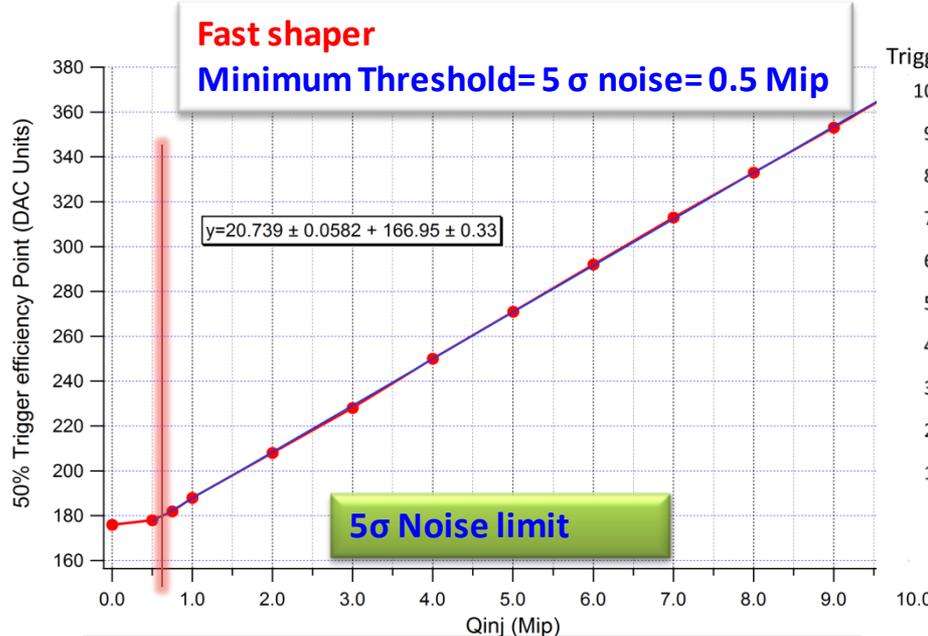
SKIROC2 digital features

- Common features with Hardroc & Spiroc (compatibility with any CALICE DAQ system)
 - Open Collector token-ring ReadOut
 - Multiplexed Slow Control & Probe
 - Redundancy on Data Out & Transmit On signal lines
 - 2 switchable StartReadOut Inputs & EndReadOut Outputs :
 - to prevent chip failure

- Very Complex Digital Part (~10% of the Die)
 - Manage Acquisition, Conversion, 15 SCA control, RAM, I/Os...



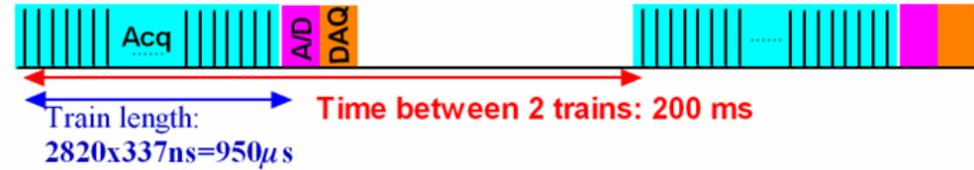
SKIROC2 PERFORMANCE



POWER PULSING

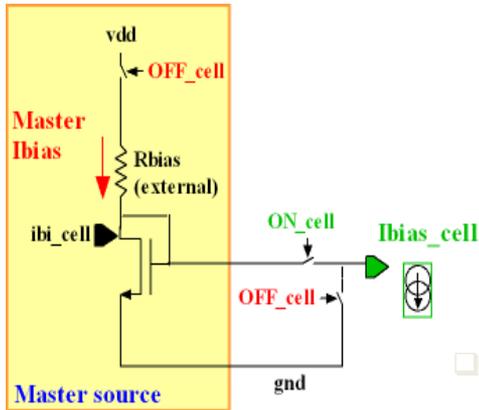
Time between 2 bunch crossings:

337 ns



Requirement:

- 25 $\mu\text{W}/\text{ch}$ with 0.5% duty cycle
- 500 μA for the entire chip



Power pulsing:

- Bandgap + ref Voltages + master I: switched ON/OFF
- Shut down bias currents with vdd always ON

SK2 power consumption measurement:

- $123 \text{ mA} \times 3.3\text{V} \approx 400 \text{ mW} \Rightarrow 6 \text{ mW}/\text{ch}$

- 4 Power pulsing lines : analog, conversion, dac, digital
- Each chip can be forced **on/off by slow control**

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MEASUREMENTS

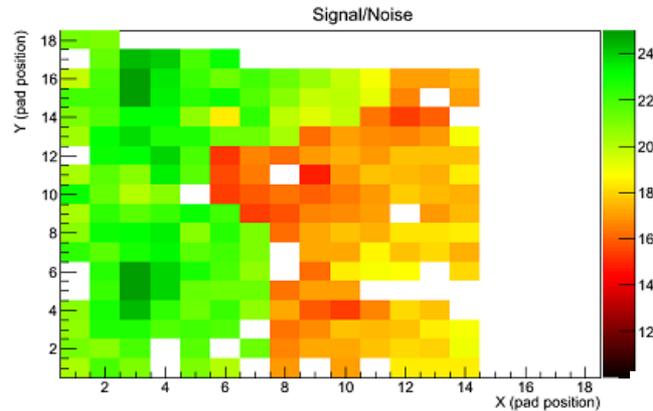
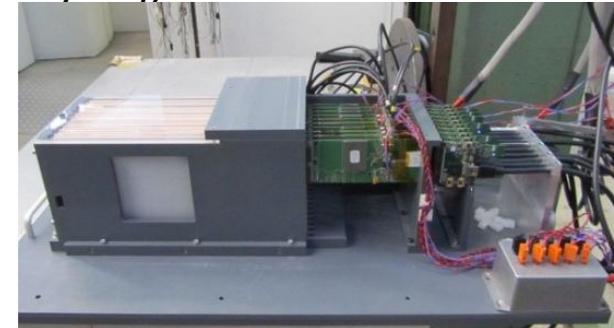
Acquisition	88 mA , 290 mW	Duty Cycle =0.5%, 1.45 mW
Conversion	27.3 mA, 90 mW	Duty Cycle =0.25%, 0.225 mW
Readout	8.0 mA, 26.4 mW	Duty Cycle =0.25%, 0.066 mW

Skiroc2 power consumption with Power pulsing: 1.7 mW ie 27 $\mu\text{W}/\text{ch}$

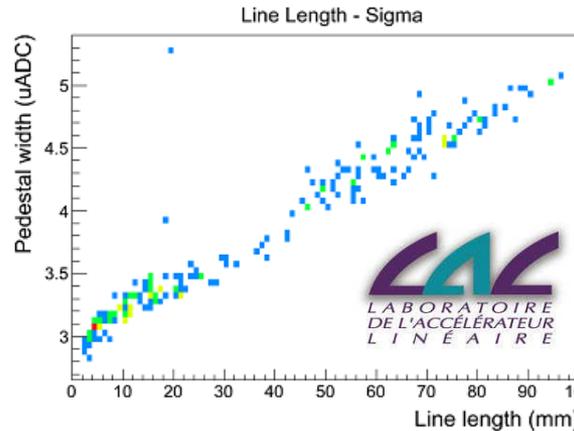
TESTBEAMs with SKIROC2

Successful test beams @ DESY in 2012 (1 to 6 layers) and 2013 (8 layers), power pulsing mode, autotrigger mode, e- (1 to 5GeV)

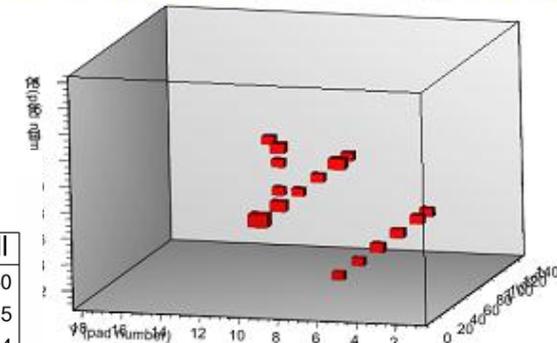
- ✓ 4 packaged skiroc2/slab
- ✓ Nice event displays



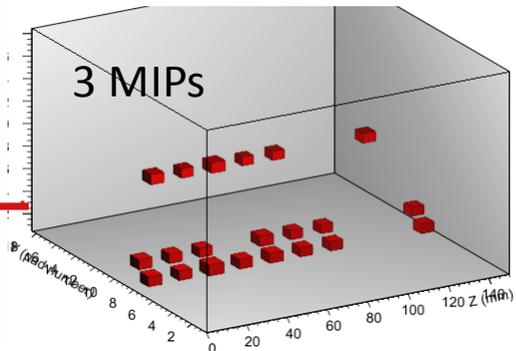
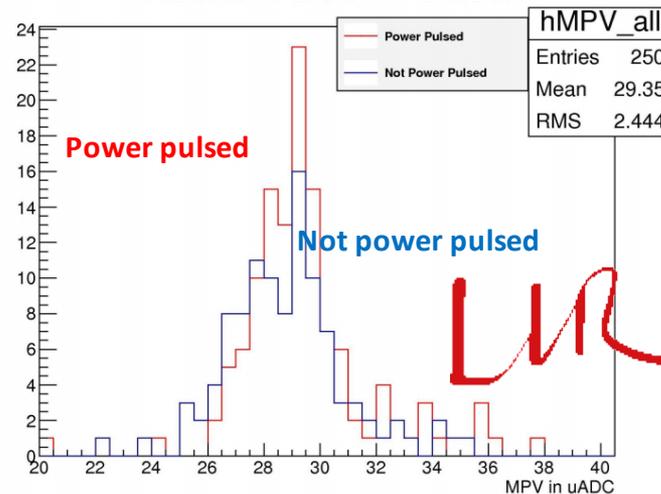
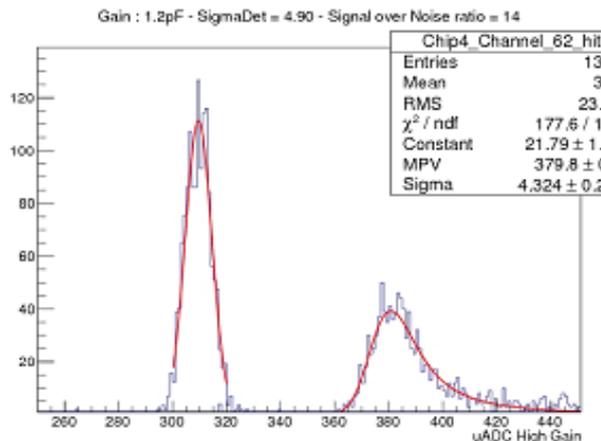
S/N > 10



2 e- (3 GeV, no tungsten)



Beam is in the center of the detector
Distribution of all the MPV of the dif 2

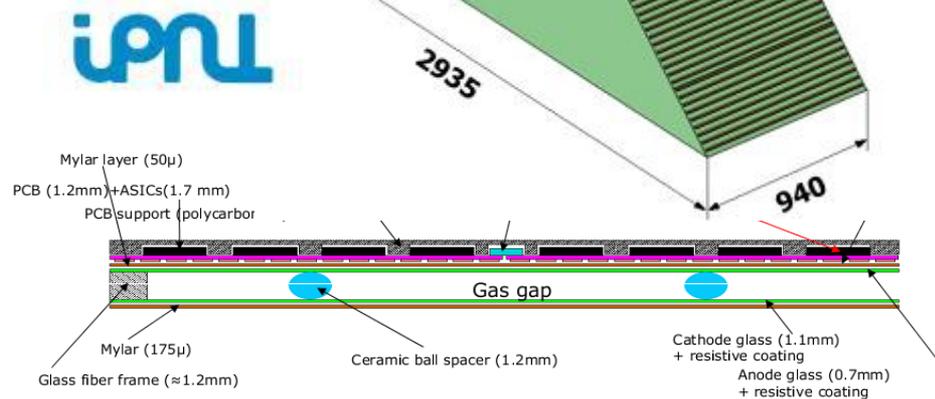
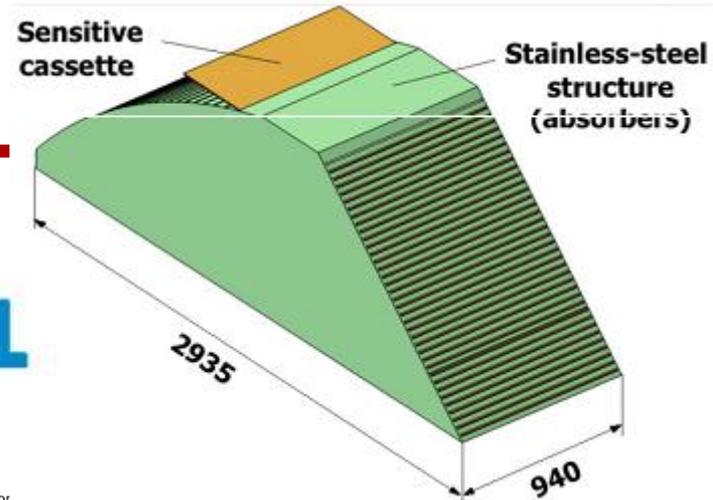
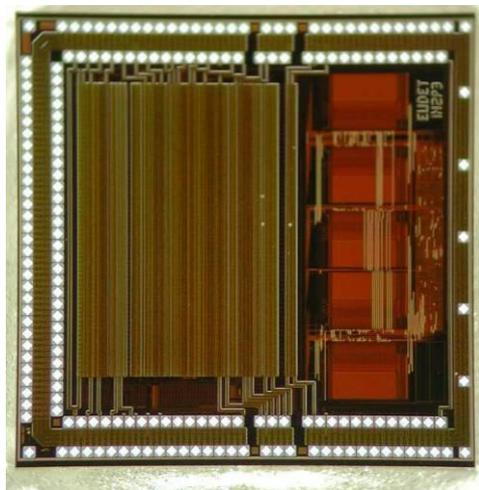
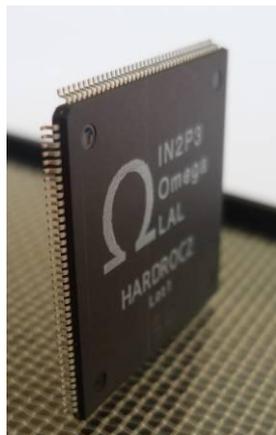


HARDROC for SDHCAL readout

Semi Digital HCAL: RPC layers

Hadronic Rpc Detector Read Out Chip

- 64 channels
- semi digital readout to reduce the number of data with 3 thresholds
 - preamp + shaper+ 3 discris + memory
- Auto trigger on 10fC up to 20 pC
- Full power pulsing



1m² RPC [IPNL]

HARDROC SCHEMATICS

64 inputs

Current preamp with **8 bits gain correct**: G=0 to 255 (analog G=0 to 2)

3 shapers, variable Rf, Cf and gains:

- ❑ Fsb1, G= 1/2, 1/4, 1/8, 1/16
- ❑ Fsb2, G= 1/8, 1/16, 1/32, 1/64

3 discriminators

- ❑ 3 10 bit-DACs to set the thresholds (100fC, 1pC, 10pC)
- ❑ Encoded in 2 bits

Auto-trigger down to 10fC up to 10pC

All channels and BCID stored for every hit in a **127 bit deep digital memory**

- ❑ Data format : 127 (depth)*[2bit*64ch+24bit(BCID)+8bit(Header)] = 20 320 bits

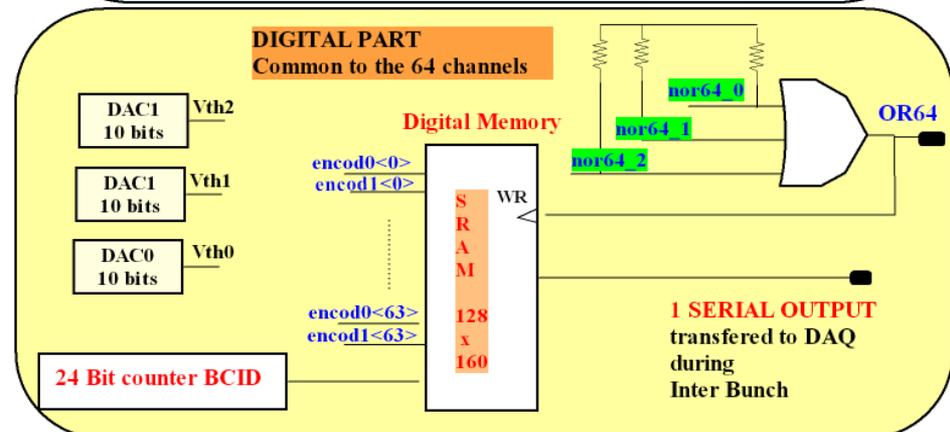
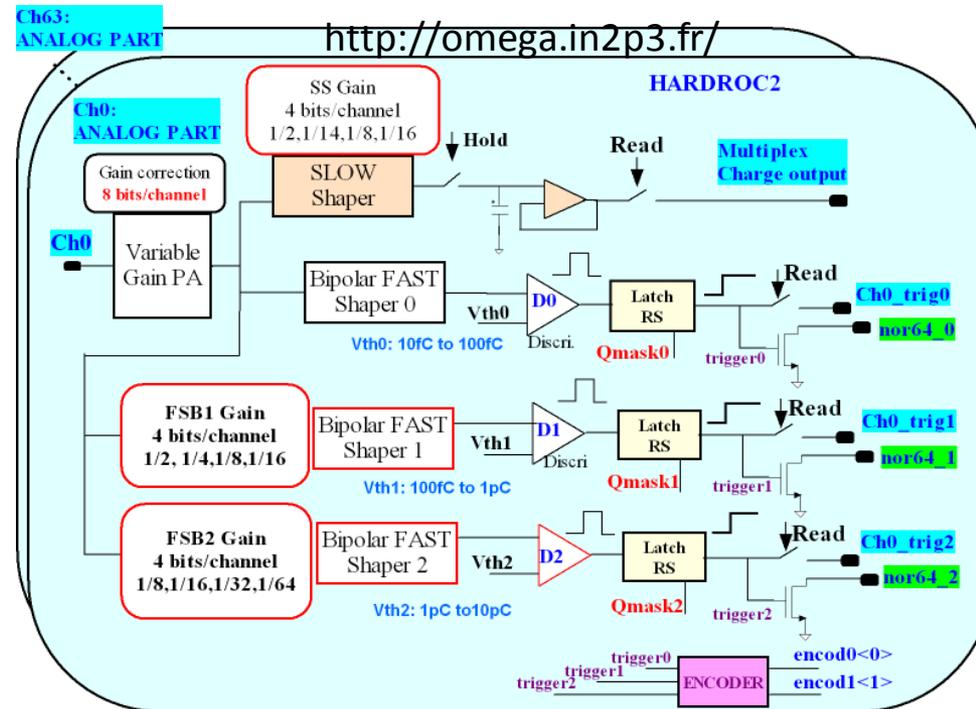
872 SC registers, default config

- ❑ Mask of bad channels

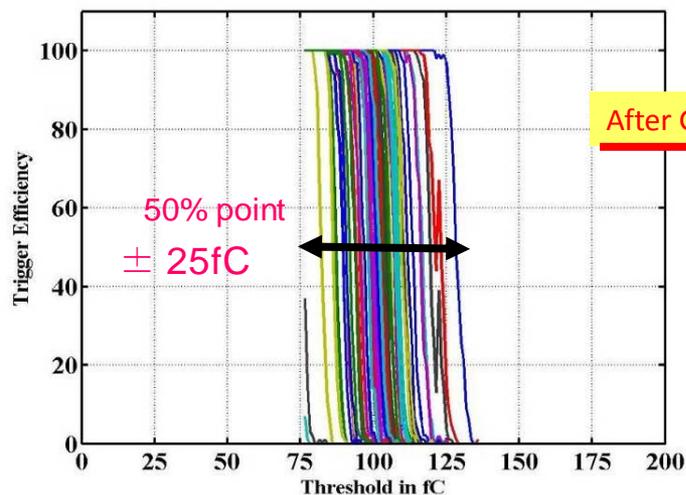
Full power pulsing: < 10μW/ch

HARDROC2

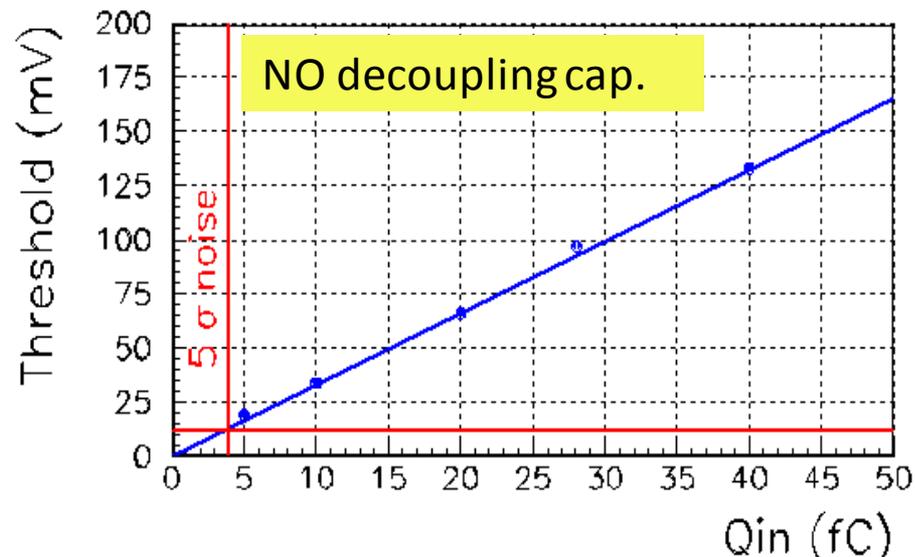
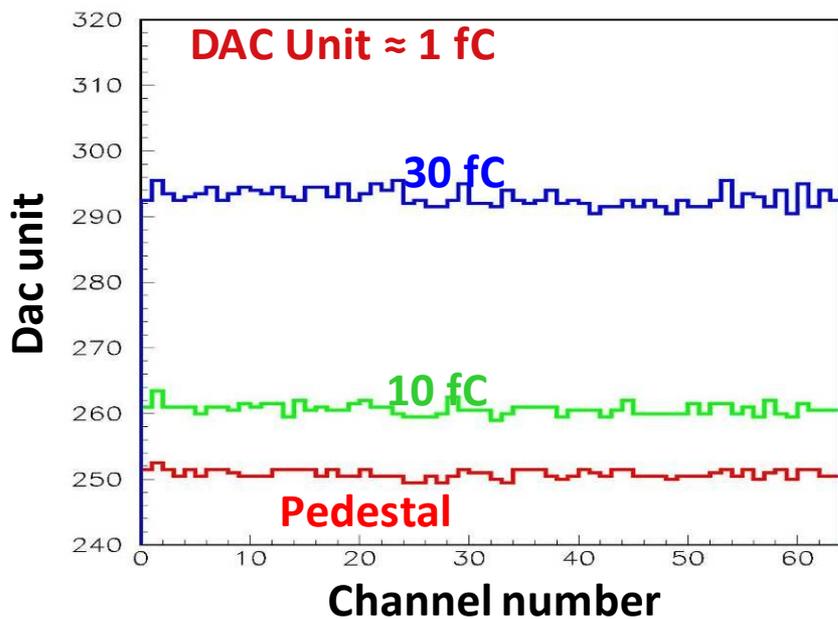
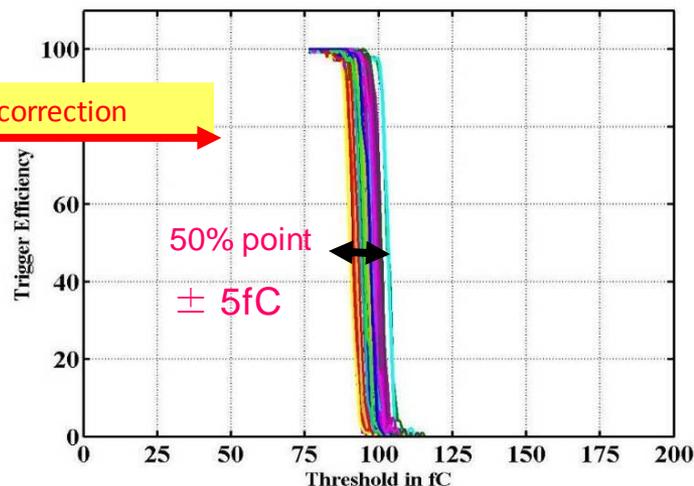
<http://omega.in2p3.fr/>



HARDROC performance



After Gain correction



HARDROC in Testbeam

1 m³ RPC detector, 40 layers
370 000 channels

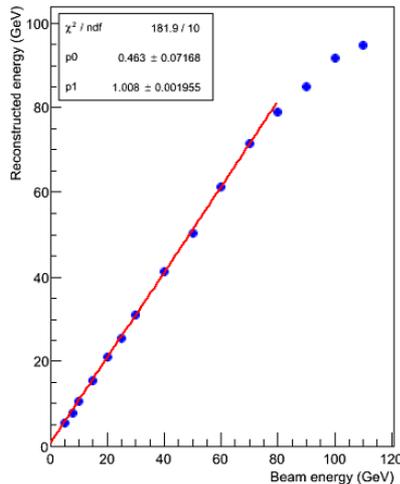
- SDHCAL technological proto with up to 50 layers (7200 HR2 chips) built in 2010-2011.
- Scalable readout scheme successfully tested
- Complete system in TB with **460 000 channels**, **AUTOTRIGGER** mode and **power pulsing (5%)**



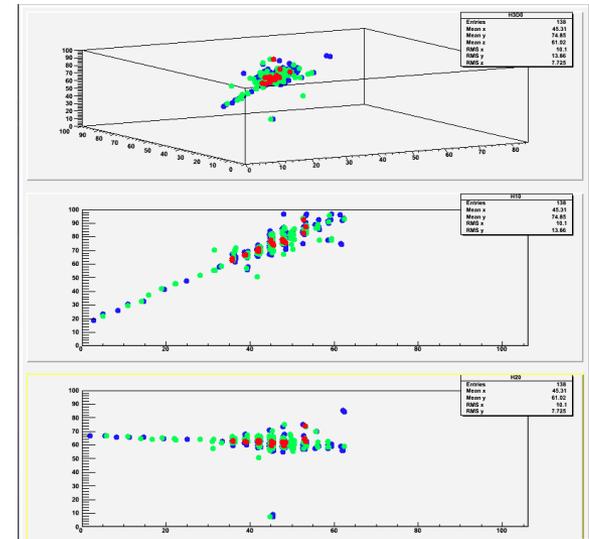
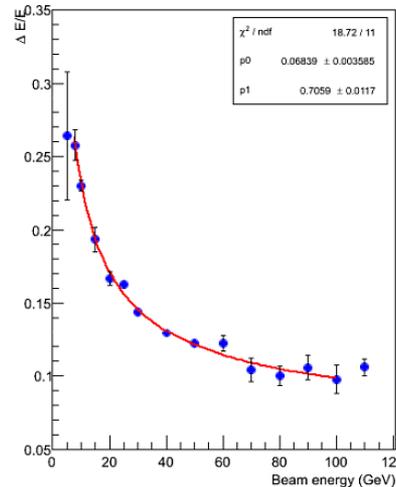
@IPNL Lyon

Vth0 Vth1 Vth2

SDHCAL mode: Reconstructed energy vs Beam Energy



SDHCAL mode: Relative resolution vs Beam Energy



POWER PULSING

- Power dissipation
 - 1.5 mW/ch continuous
 - 25 μ s awake time
 - 7.5 μ W/ch with 0.5% duty cycle
- 10 μ W/ch = 24h operation of full slab with 2 AAA batteries !



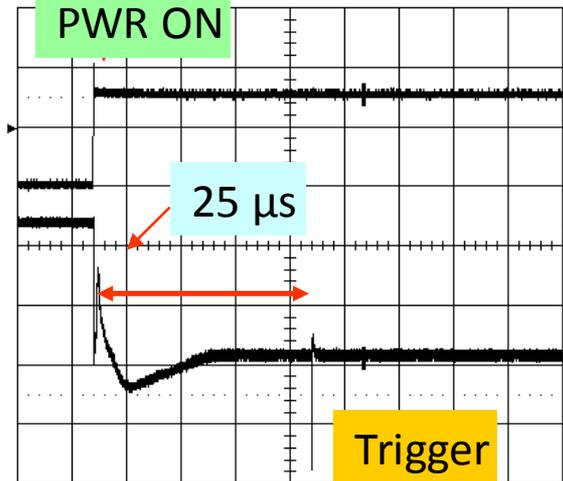
16-Jan-09

15:06:58

2

5 μ s

2.00 V



5 μ s

1.5 V AC

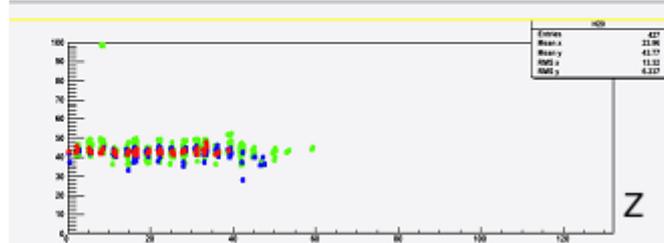
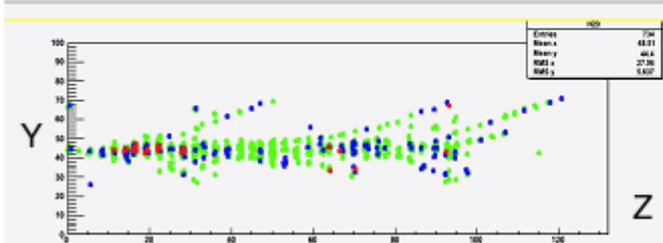
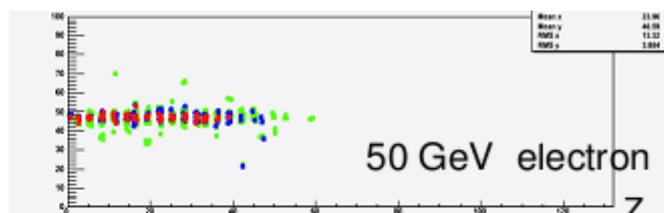
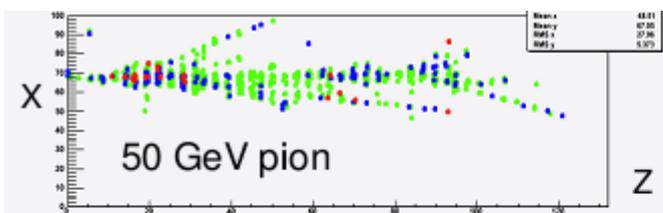
Time

24.7095 μ s

2 2 V DC

2 DC 1.88 V

Testbeam: 370 000 channels power pulsed (5% duty cycle)

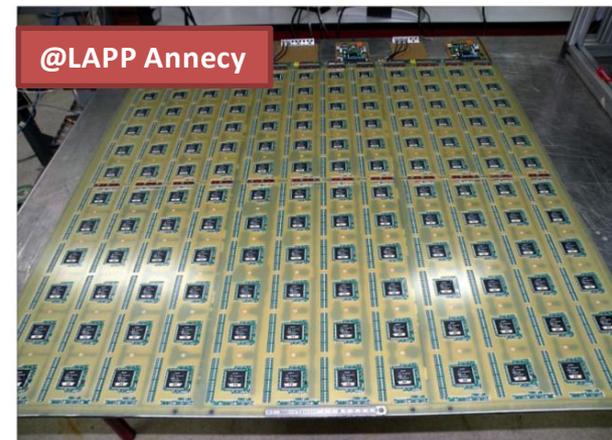


Colours correspond to the three thresholds: Green (114 fC), Blue (5 pC), Red (15 pC)

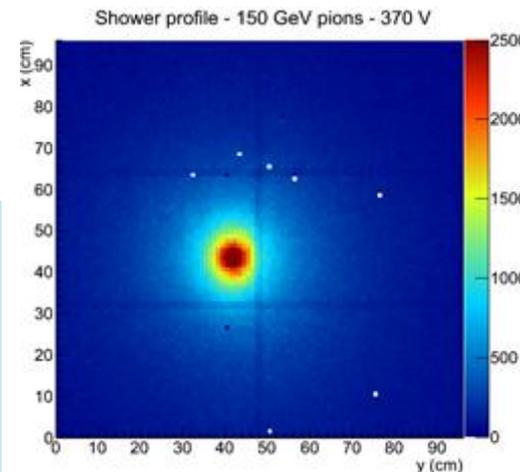
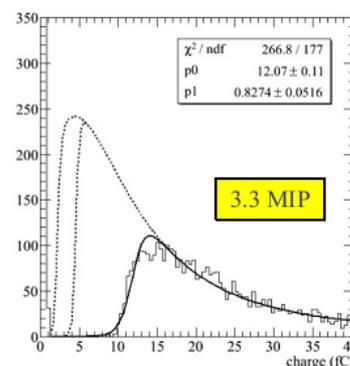
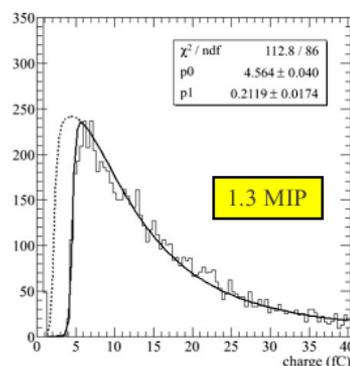
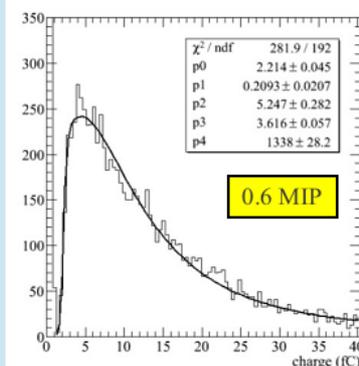
MICROROC (variant of HARDROC)

64 channels to readout a DHCAL equipped with MICROMEAS

- ❑ Very similar to HARDROC except for the input preamp (@LAPP) and shapers (100-150 ns)
- ❑ **Noise: 0.2fC** (Cd=80 pF). Auto trigger on 1fC up to 500fC
- ❑ Pulsed power: **10 μ W/ch** (0.5 % duty cycle)
- ❑ 4 Micromegas prototypes of 1x1 m² were constructed in 2011-2012 and tested in particle beams inside the DHCAL steel structure in 2012
- ❑ **Very good performance of the electronics and detector in autotrigger mode and with threshold set to 1fC**



Landau distribution with cuts on the passed thresholds



❑ 3rd generation chip for ILD

❑ Independent channels (zero suppress):

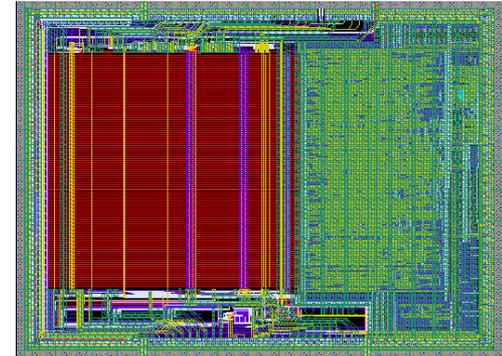
Each of the hundred millions of channels:

will sense that it gets a signal,

will measure its charge on 16 bits and its time to a fraction of ns

and will send its zero-suppressed digital information to the

reconstruction farms. This scheme is **extremely challenging for such large detectors**



❑ I2C link (@IPNL) for Slow Control parameters and **triple voting**

❑ HARDROC3: 1st of the 3rd generation chip to be submitted

– No major change in the analog part

– PLL: integrated to generate clocks internally,

– Submitted in Feb 2013 (SiGe 0.35 μ m), funded by AIDA, received end of June 2013

– Die size ~ 30 mm² (6.3 x 4.7 mm²)

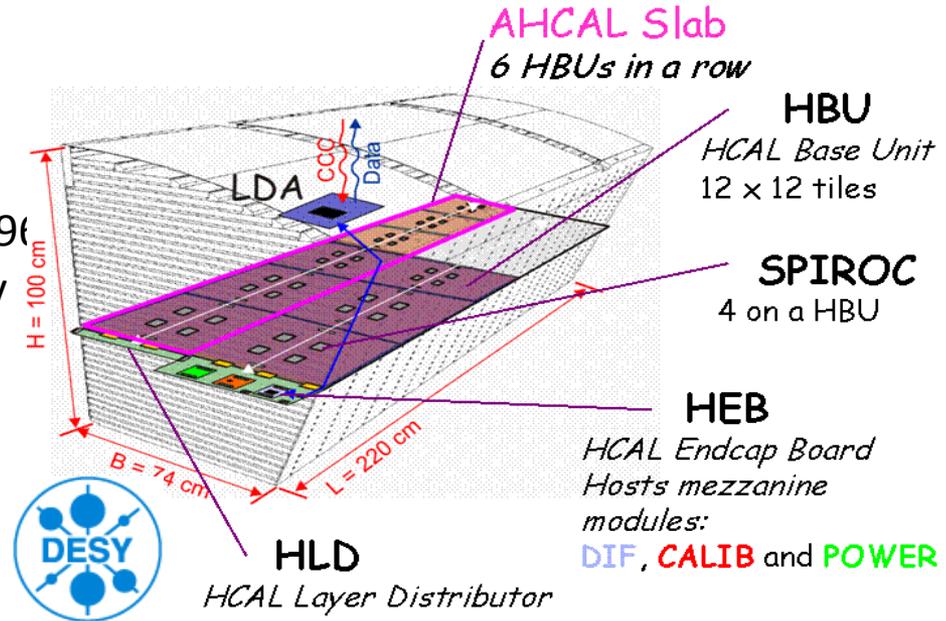
– To be packaged in a TQFP208, will equip 2-3m RPC chambers

– **2013: dedicated to the test of HR3 before submitting other chips**

SPIROC for AHCAL readout

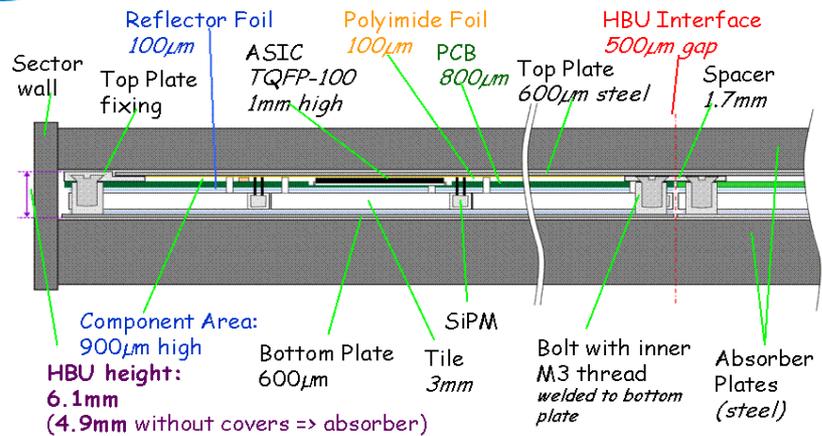
❑ Analog HCAL:

- ✓ 40 layers of 1.5 m² 2 cm thick steel plates interleaved with cassettes of 29 scintillating tiles (3x3 cm²) readout by SiPMs

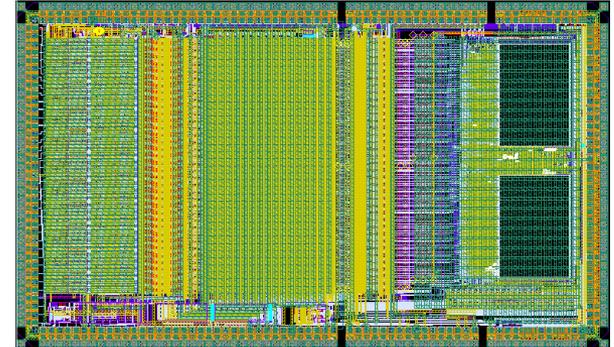


❑ FE Chip embedded inside the detector

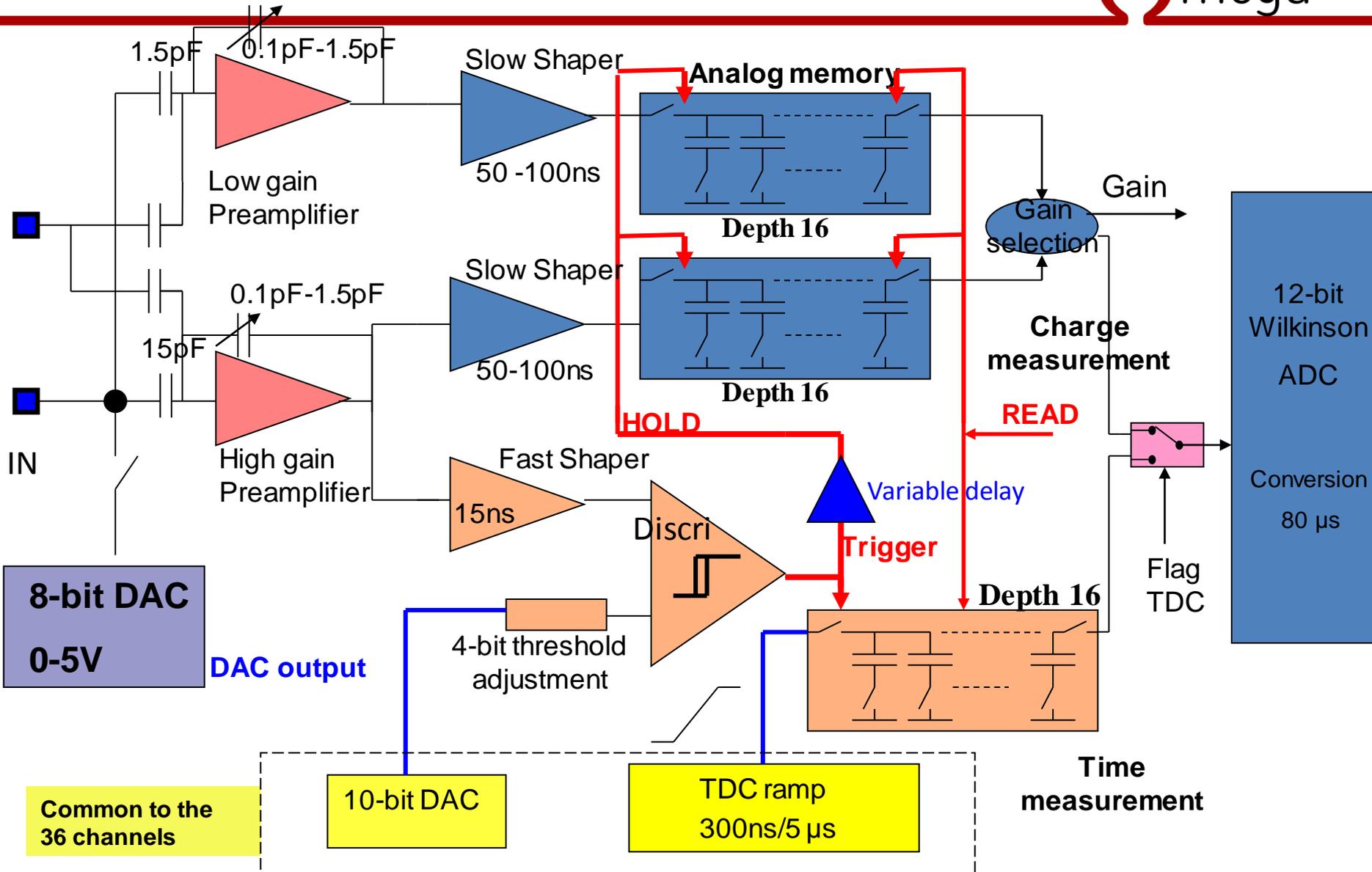
- ✓ Thickness: critical issue, mother boards (HBU) are sandwiched between 2 absorber plates



- Internal input 8-bit DAC (0-5V) for individual SiPM gain adjustment
- Energy measurement : 14 bits
 - 2 gains (1-10) + 12 bit ADC: 1 pe \rightarrow 2000 pe
 - Variable shaping time from 50ns to 100ns
 - pe/noise ratio : 11
- Auto-trigger on 1/3 pe (50 fC)
 - pe/noise ratio on trigger channel : 24
 - Fast shaper : \sim 10 ns
 - Auto-Trigger on $\frac{1}{2}$ pe
- Time measurement :
 - 12-bit Bunch Crossing ID
 - 12 bit TDC step \sim 100 ps
- Analog memory for time and charge measurement : depth = 16
- 4k internal memory and Daisy chain readout
- Low consumption : \sim 25 μ W per channel (in power pulsing mode)
- Individually addressable calibration injection capacitance
- Embedded bandgap for voltage references
- Embedded 10 bit DAC for trigger threshold and gain selection
- Multiplexed analog output for physics prototype DAQ



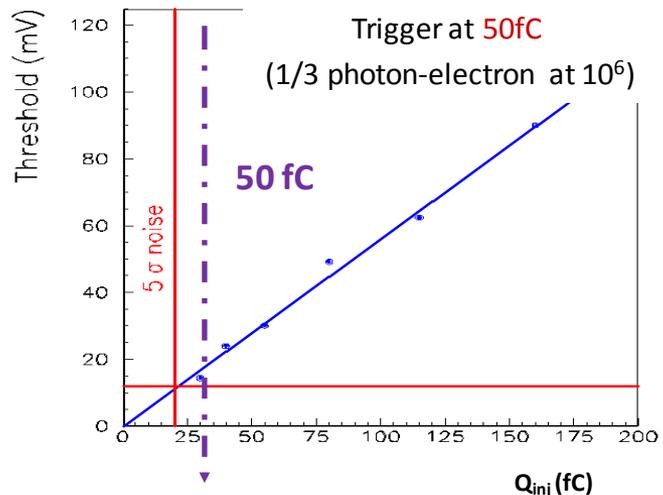
SPIROC: one channel schematics



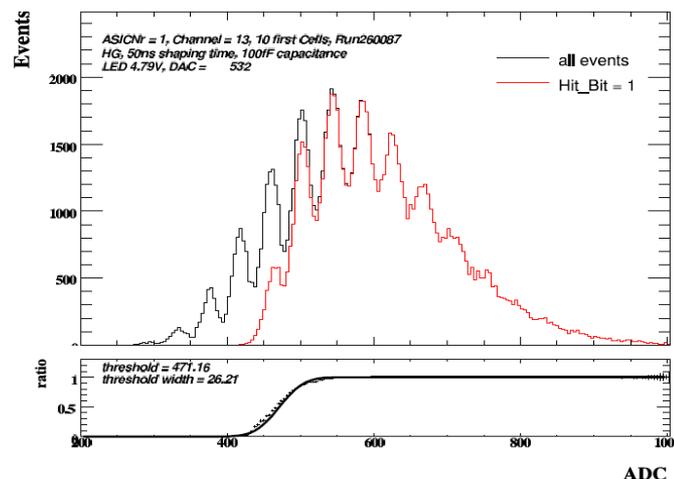
SPIROC2 performance



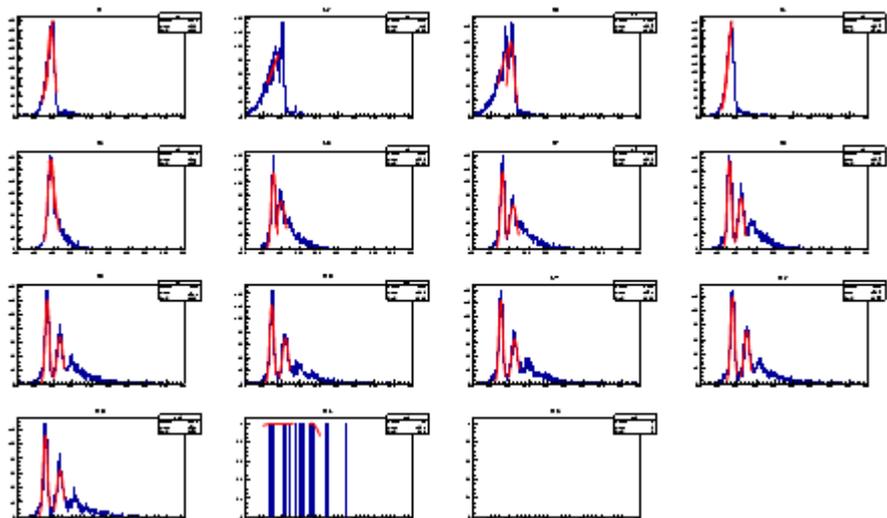
50 % Trigger efficiency point vs Q_{inj}



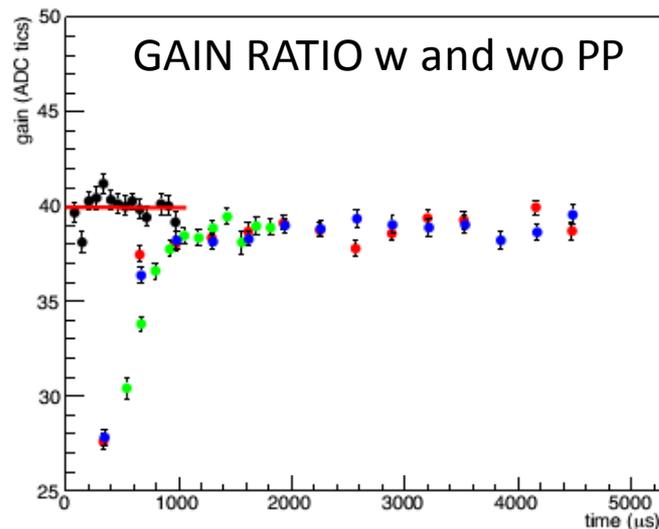
SiPM SPECTRUM with Autotrigger



Power pulsing measurements on testbench (DESY) (Monitoring of the gain vs wake up time)

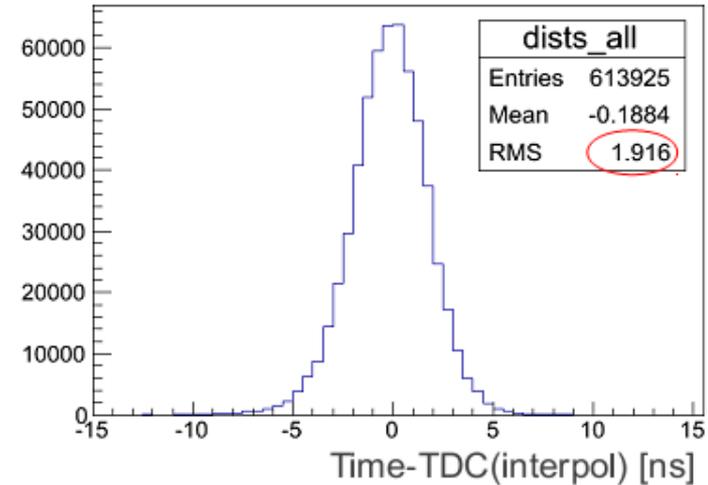


Gain



TESTBEAMS WITH SPIROC2

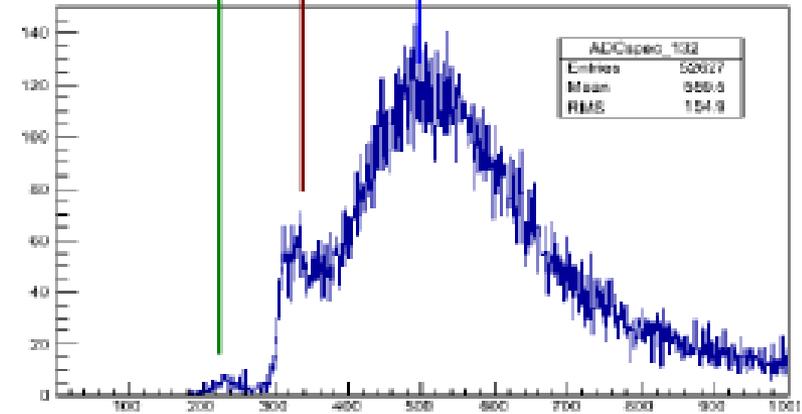
- ❑ 576 channel AHCAL layer prototype **successfully tested at CERN and at DESY** in 2012
- ❑ TDC: First tests of TDC ramps in SPIROC2b show promising results
 - ✓ Several corrections needed: memory cell and channel wise offsets correction, chip wise ramp corrections
 - ✓ Electronics resolution ~ 2 ns, allows neutrons identification
- ❑ Multi layer prototype in TB at DESY in June 2013



@DESY, HBU

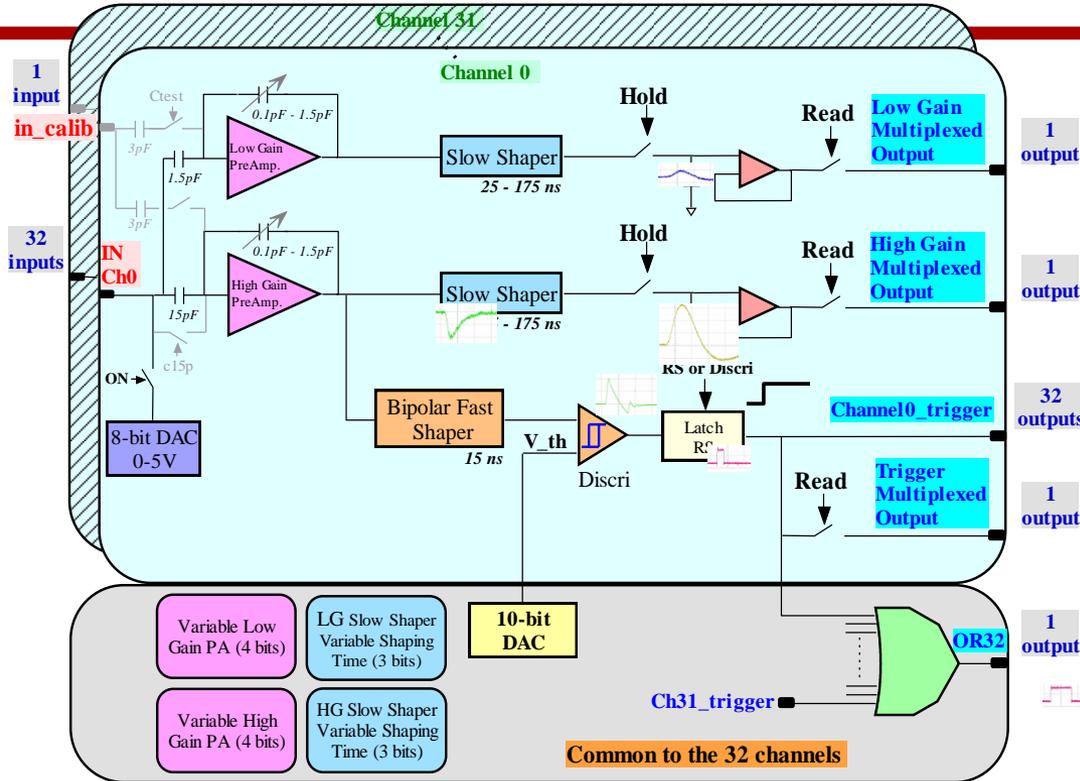


pedestal
threshold
MIP
ADC Spectrum ASIC 132



Plots: Katja Krüger

EASIROC: SIMPLER VERSION



- 32-channel front-end readout (analogue part of SPIROC)
 - 2 multiplexed analog outputs (high gain, low gain) [tri state outputs]
- Trigger output
 - 32 Trigger outputs
 - OR32 output
 - Trigger multiplexed output (latch included) [Tri state output]
- Low power : **4.84 mW/channel**, 155 mW/chip

SipMed, IMNC, LAL, OMEGA

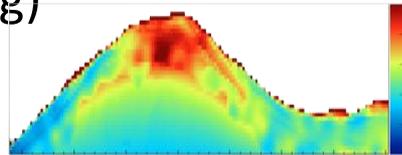
Many applications:

- Astrophysics (CTA Palermo),
- Nuclear physics (KEK, Tohoku),
- PET (Roma, Pisa, Valencia),
- Vulcanology (Napoli, IPN Lyon)

JPARC



- ❑ Imaging calorimetry possible thanks to ROC chips, also used for many other applications (astrophysics, vulcanology, medical imaging)



*γ ray camera
readout with Hardroc*

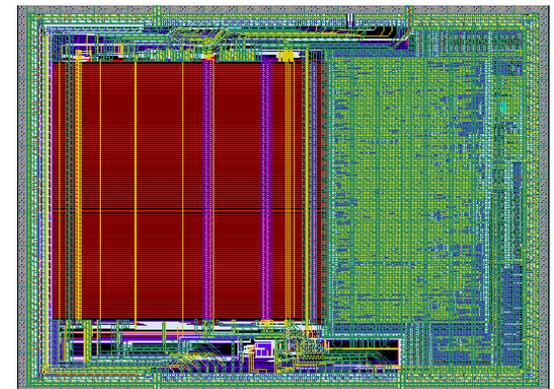
- ❑ Integration issues successfully addressed with the 2nd generation chips

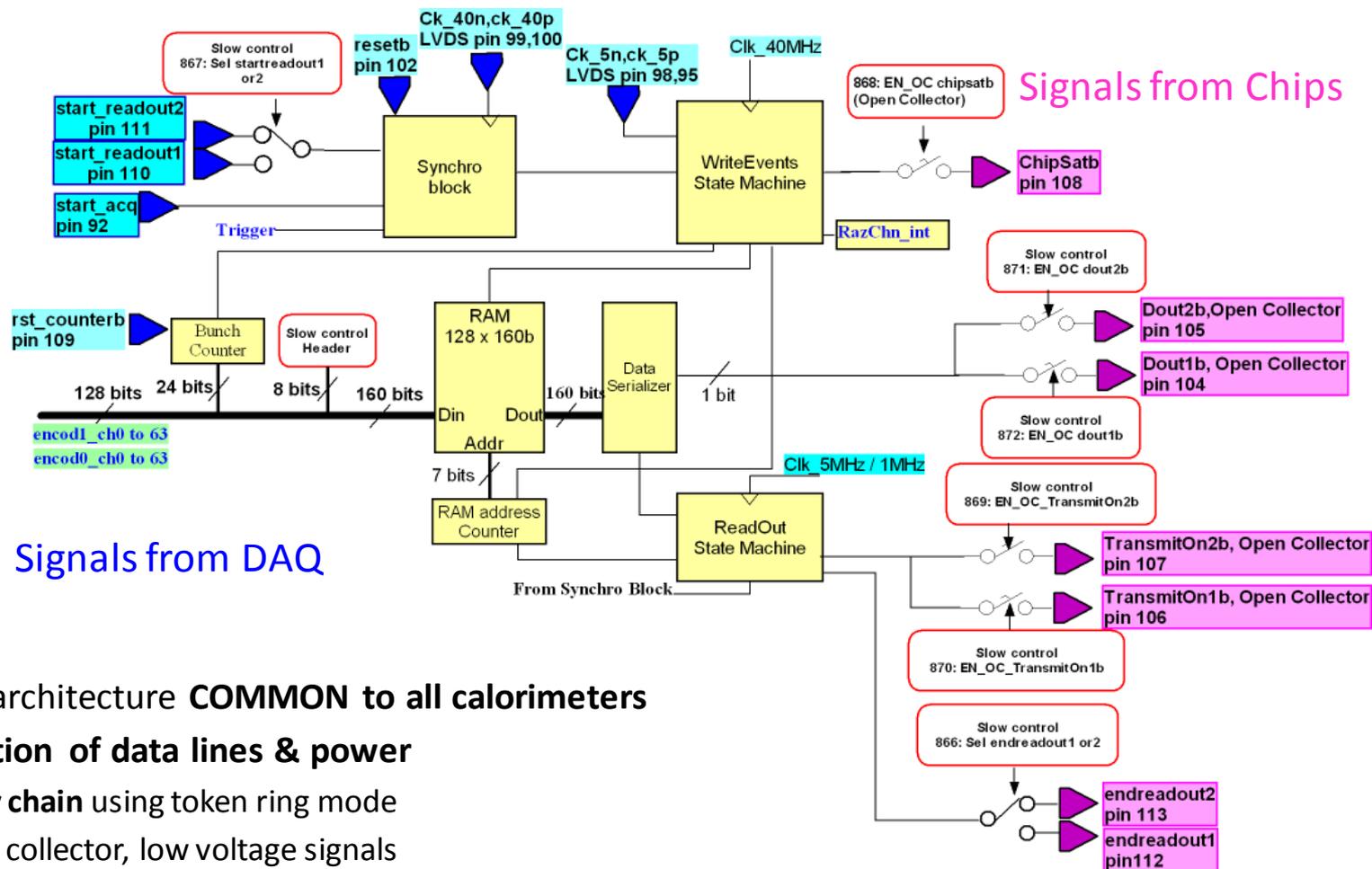
- ❑ **Complete systems with up to 400k channels run at system level in auto trigger mode and with power pulsing**

- ❑ **3rd** and last **generation** of chips (= completely independent channels, triggerless) underway

⇒ Intelligence brought inside the chips

⇒ Major change for the next generation of detectors





- Readout architecture **COMMON** to all calorimeters
- **Minimization of data lines & power**
 - **Daisy chain** using token ring mode
 - Open collector, low voltage signals
 - Low capacitance lines

MAIN SIGNALS OF THE DAISY CHAIN



COMMON to all the ROC chips

StartAcq

- Start acquisition, generated by DAQ

ChipSat (Open Collector signal):

- Generated by chip, « 1 »: digital memory is full or acq is finished

StartReadout:

- Generated by DAQ, start of the readout

EndReadout

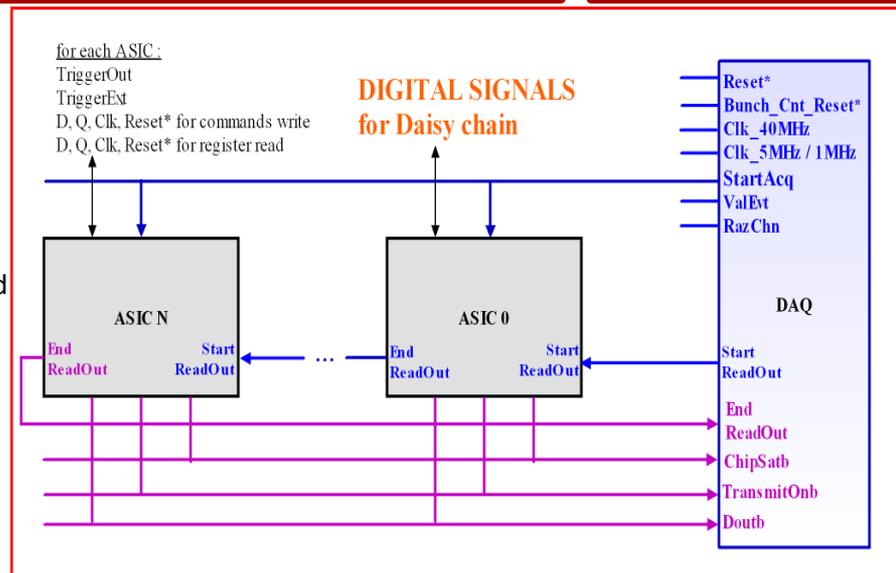
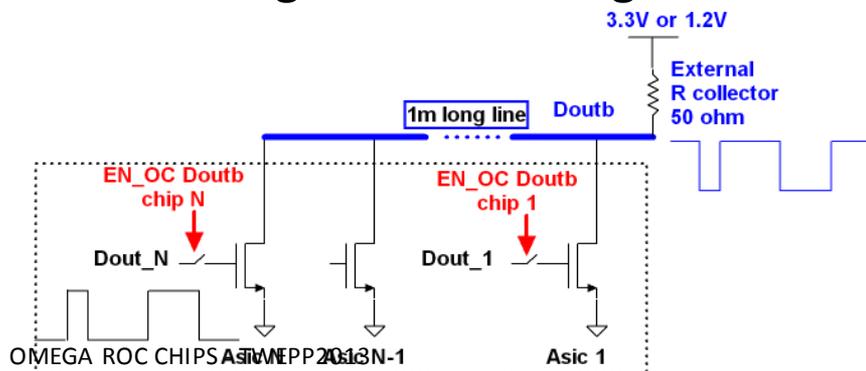
- Generated by chip, End of the readout

Dout: data out (OC signal)

TransmitOn (OC signal)

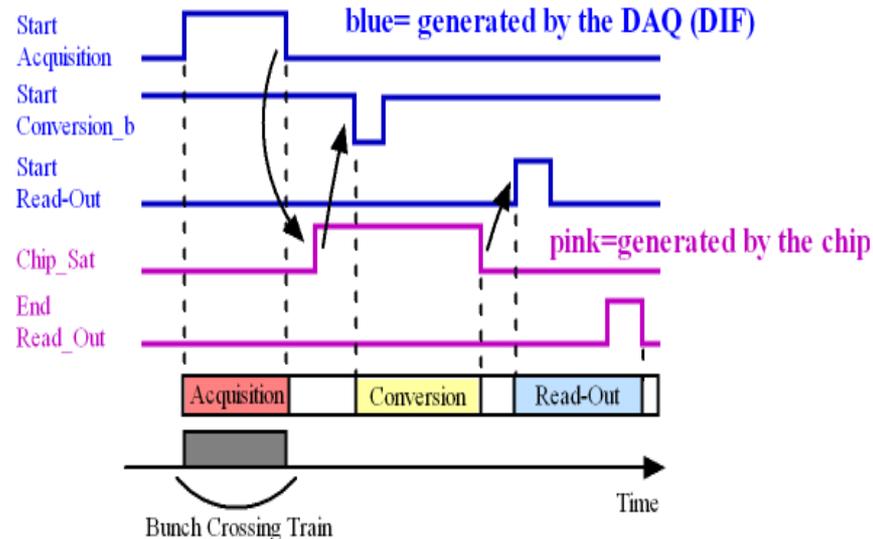
- Generated by chip, Data out are transmitted

Buffers integrated for OC signals

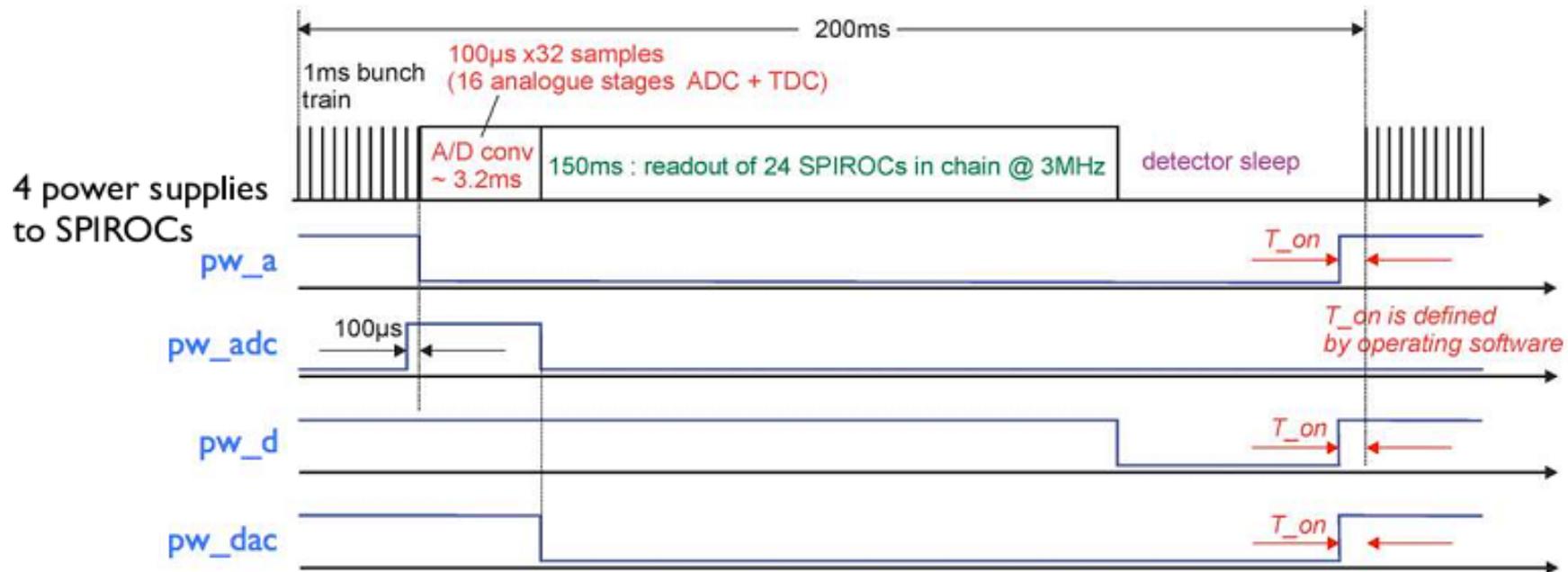


ILC

No conversion in Hardroc



POWER PULSING LINES



(B. Hermberg, M. Reinecke, M. Terwort (2012))