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ROC chips for imaging calorimetry at the International Linear Collider

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Imaging calorimetry at the International Linear Collider requires highly granular and innovative detectors. Technological prototypes have been built and tested under the CALICE collaboration framework and FP6 EUDET, FP7 AIDA EU programs. These prototypes are readout by multi-channel chips named SKIROC2, SPIROC2 and HARDROC2, designed in SiGe 350 nm technology by the IN2P3 OMEGA group.
In this presentation, the ASIC architectures and test results on test bench and at system level will be described as well as first results of test bench measurements performed on HARDROC3, which is the first of the "3rd generation"chip to be submitted and where the 64 channels are handled independently to perform zero suppress on chip.

Summary

Imaging calorimetry at the International Linear Collider requires new detectors with one hundred million channels that will be read-out with calorimetric performance, that is percent accuracy over 16-bit dynamic range. The readout electronics must be highly integrated and ultra-low power (μW per channel compared to W at LHC) to be embedded inside the detectors.
To tackle these challenges, R&D started in 2000 under the CALICE collaboration framework and FP6 EUDET, FP7 AIDA EU programs. Several detector technologies have been proposed and tested: Tungsten/Silicon for the Electromagnetic Calorimeter (ECAL), scintillating tiles SiPM readout for an Analog Hadronic Calorimeter (AHCAL) and RPC/Micromegas/GEM for a Semi Digital Hadronic Calorimeter (SDHCAL).
Detector prototypes have been built and readout by "ROC"chips (Read Out Chips) named SKIROC, SPIROC and HARDROC and designed in SiGe 350 nm technology by the IN2P3 OMEGA group. They have similar requirements in terms of low noise, low power and radiation hardness and thus similar design: a low noise input stage for amplification, a slow channel for charge measurement, a trigger channel, a conversion stage for internal time and charge digitization and a complex digital part to manage the acquisition, the conversion and the read out.
Different front-end architectures have been integrated for the various sensors and, to optimize the commonalities between the various detector proposals, the chips share a common backend and readout scheme. In order to address the numerous challenges, three generations of chips have been foreseen. The first generation consisted in analog readout ASICs that allowed characterizing the detector concepts in test beam, referred to as CALICE physics prototypes. The second generation addresses the integration issues with embedded electronics and performs analog amplification, shaping, internal triggering, digitization and local storage of the data in memory. Thousands were produced in 2010 to equip CALICE technological prototypes and are being tested by IN2P3, DESY, CERN, and KEK groups for their detectors.
Zero suppression must be added in the 3rd generation chips, which is a major modification as it increases the complexity of the digital part. HARDROC3 was submitted in March 2013. It is the first of the 3rd generation chip to be submitted. It integrates 64 channels which are handled independently to perform zero suppress on chip and reduce the data volume. Other features such as triple voting to ensure SEU hardness, a I2C link to load slow control configurations and a Phase Lock Loop to generate the clocks internally are also integrated. First testbench results are expected this summer.
The architecture and the performance of these chips on test bench and at the system level will be detailed in this presentation.

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