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The proposed trigger-less TBit/s readout for the Mu3e experiment

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The Mu3e experiment searches for charged lepton flavor violation in the rare decay $\mu \rightarrow eee$ with a projected sensitivity of 10^{-16} . Precise measurement of the decay product momentum, decay vertex and time is necessary for background suppression at rates of 10^9 muons/s. This can be achieved by combining an ultra-lightweight pixel tracker based on HV-MAPS with two timing systems. The trigger-less readout of the detector with three stages of FPGA-boards over multi GBit/s optical links into a GPU filter farm will be presented. In this scheme data from all sub-detectors is merged and distributed in time slices to the filter farm.

Summary

The Mu3e experiment searches for charged lepton flavor violation in the rare decay $\mu \rightarrow eee$. Since the decay $\mu \rightarrow eee$ is extremely suppressed in the standard model with a $BR < 10^{-50}$ any observation would be a clear sign of new physics. In order to measure or exclude this decay with a sensitivity of 10^{-16} , more than 10^9 muons/s have to be observed for one full year. The background for this measurements is either combinatorial or stems from the radiative decay $\mu \rightarrow eee\nu$. Precise measurement of the decay product momentum, decay vertex and time is necessary for background suppression. The low momentum of the decay electrons leads to large multiple scattering and demands detectors of extremely low radiation length in the active volume of the experiment. The high vertex and momentum resolution is achieved with the help of a tracking system based on high voltage monolithic active pixel sensors (HV-MAPS) thinned to 50 μm . These sensors not only have on-chip analog electronics but also digital zero suppression and fast serializers. The necessary high time resolution is obtained by a scintillating fiber tracker and a scintillating tile hodoscope, both equipped with SiPMs.

The high and continuous muon decay rate of $10^9/\text{s}$ and the event size of 1kBit per decay lead to a considerable amount of data of 1 TBit/s. The data of the full detector has to be merged and time slices of this data must be distributed to the individual nodes of the event filter farm online. The trigger-less TBit/s readout of the detector is based on three stages of FPGA driven readout boards. The first stage is located near the sensors and receives serial zero-suppressed data from the HV-MAPS at 800 MBit/s per link. The corresponding front-end boards for the SiPM based detectors either utilize the DRS5 chip developed at PSI or the STiC TDC developed at the KIP in Heidelberg. In all cases the data is reformatted and send over optical multi GBit/s links to off-detector read-out boards. There is one off-detector readout board per sub-detector partition and PC sub-farm. The first part of the data distribution can be accomplished by connecting the eight optical outputs of one detector front-end board to four different off-detector readout boards belonging to one PC sub-farm each.

The off-detector readout boards distribute the data within one PC sub-farm over optical links. The optically transmitted data is received by one PCIe-board inside each of the twelve PCs of one sub-farm. These PCIe boards build blocks of events from the full detector with the help of powerful FPGAs and transmit large data sets at high speed via PCIe to the graphical processing units (GPUs). Preferably the communication between these FPGAs and the GPUs is realized using direct memory access (DMA). Tracking and event reconstruction runs on the GPUs with the purpose of reducing the background events by a factor > 1000 . The remaining up to 100 Mbytes/s of data are written to a storage system via Gigabit Ethernet.

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