A GLIB-based uTCA demonstration system for HEP experiments

Hands-on the new link for LHC upgrades

PH-ESE-BE

Manoel Barros Marin [on behalf of the GLIB team]

TWEPP-13 Perugia (24/09/2013)

A GLIB-based uTCA demonstration system for HEP experiments

Outline:

- Introduction
- Demonstration system overview
- Summary & Outlook
- Acknowledgements & References

PH-ESE-BE

Hands-on the new link for LHC upgrades

A GLIB-based uTCA demonstration system for HEP experiments

Outline:

- Introduction
- Demonstration system overview
- Summary & Outlook
- Acknowledgements & References

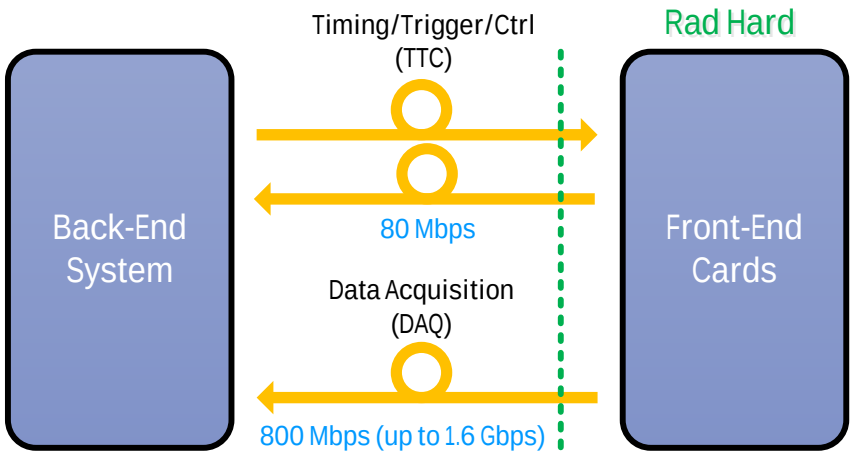
PH-ESE-BE

Hands-on the new link for LHC upgrades

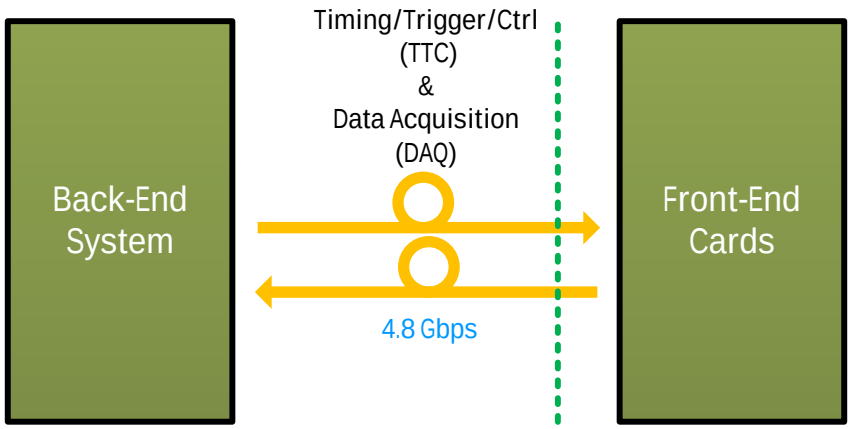
Introduction (1 of 2)

Links for LHC experiments

- **Current generation:**
  - Separated links for TTC & DAQ.
  - Direct clock forwarding to Front-End.

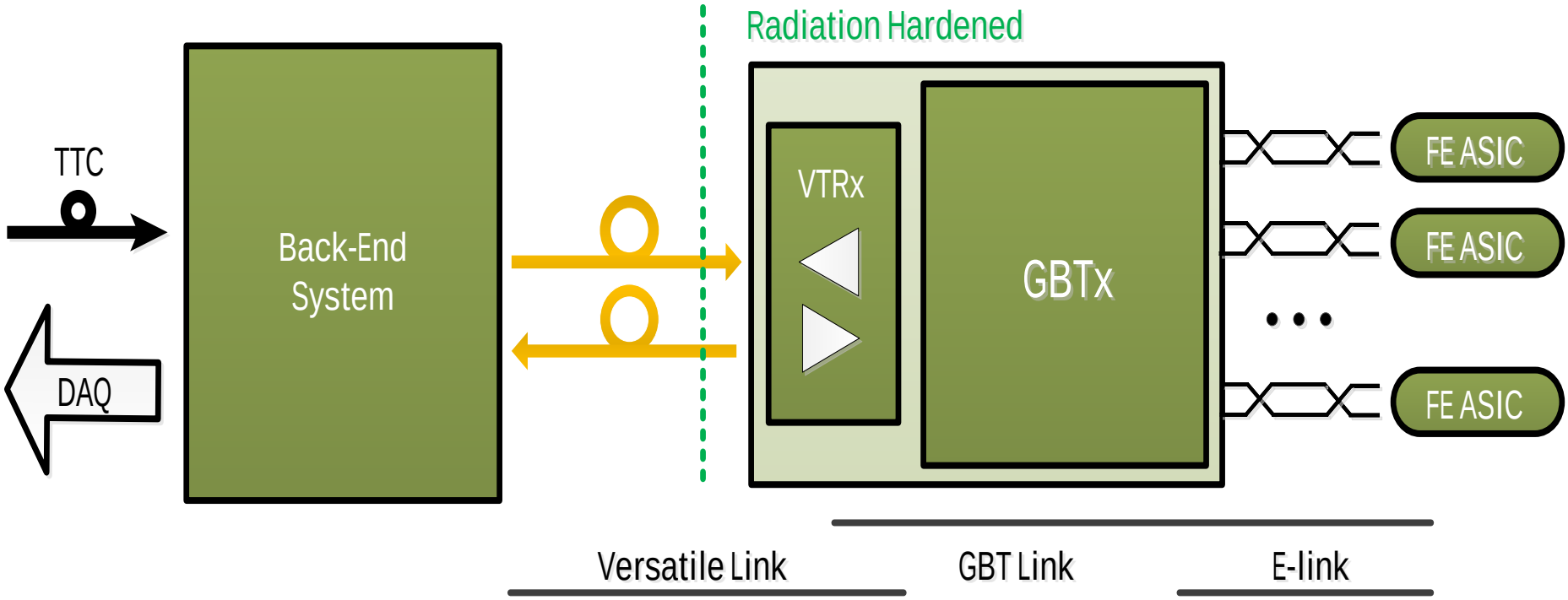


- **New generation:**
  - Unified link for TTC & DAQ.
  - Much faster DAQ.
  - Clock recovered from data stream.



Introduction (2 of 2)

The new link



A GLIB-based uTCA demonstration system for HEP experiments

Outline:

- Introduction
- Demonstration system overview
- Summary & Outlook
- Acknowledgements & References

PH-ESE-BE

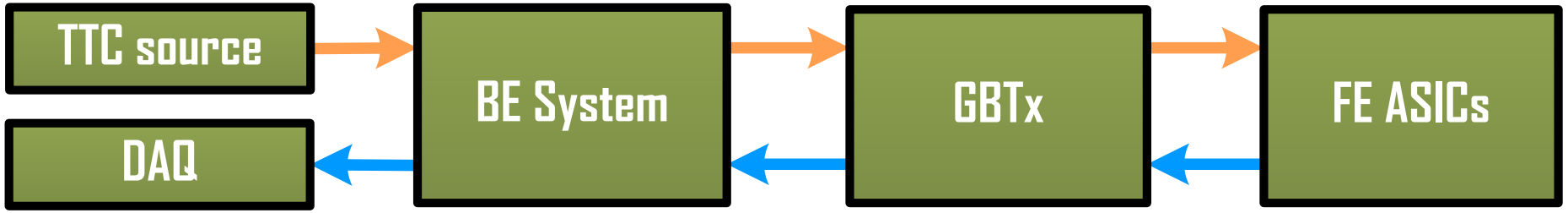
Hands-on the new link for LHC upgrades

Demonstration system overview (1 of 16)

Motivation

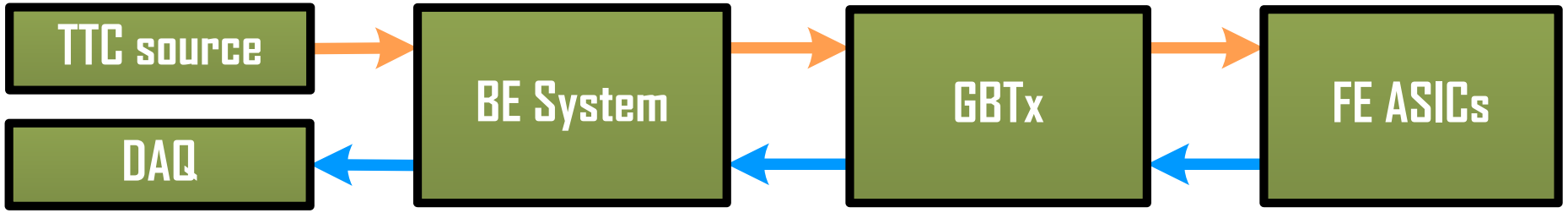
Demonstration system overview (1 of 16)

Motivation



Demonstration system overview (1 of 16)

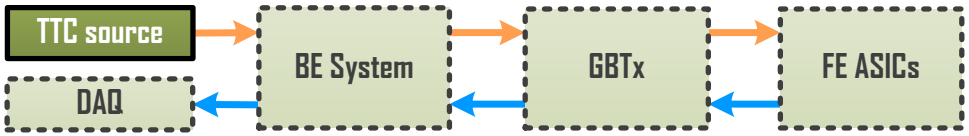
Motivation



To demonstrate the feasibility of the new link for LHC upgrades in an early state of development using realistic resources

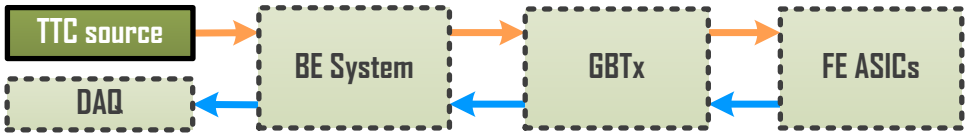
Demonstration system overview (2 of 16)

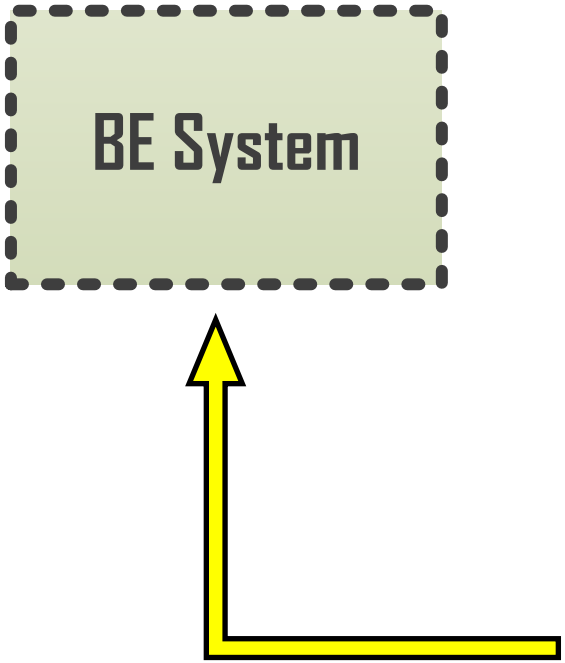
TTC source



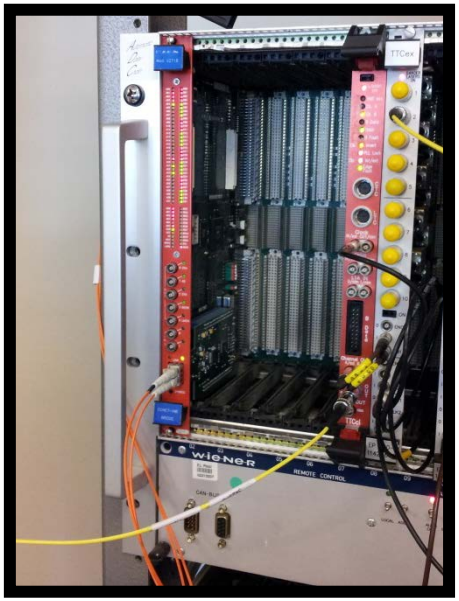
Demonstration system overview (2 of 16)

TTC source



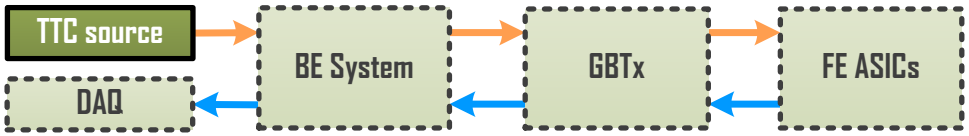


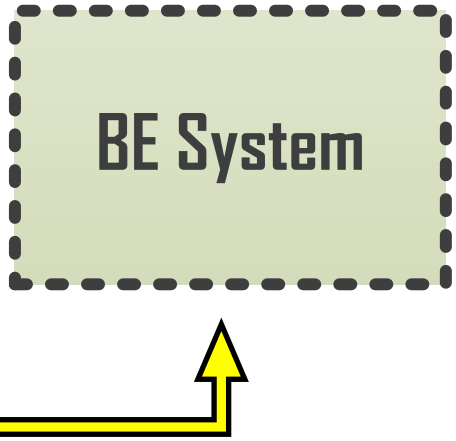
Standard TTC system



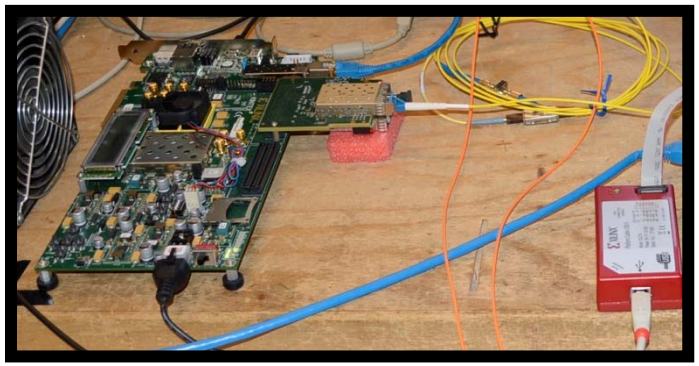
Demonstration system overview (2 of 16)

TTC source



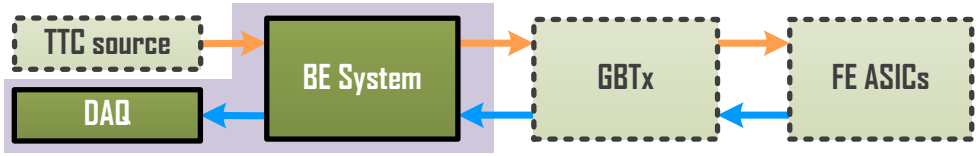


FPGA-based devkit



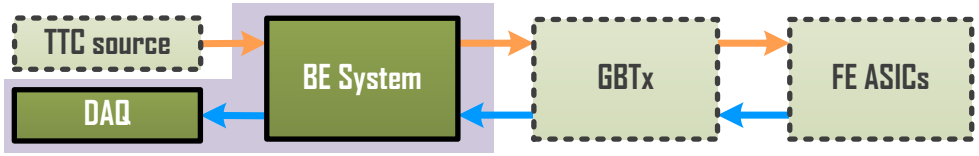
Demonstration system overview (3 of 16)

Back-End System & DAQ



Demonstration system overview (3 of 16)

Back-End System & DAQ



BE System

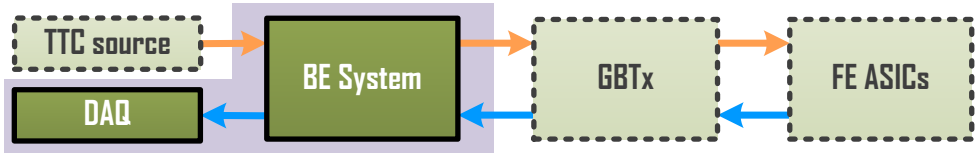
TTC FMC

GLIB AMC

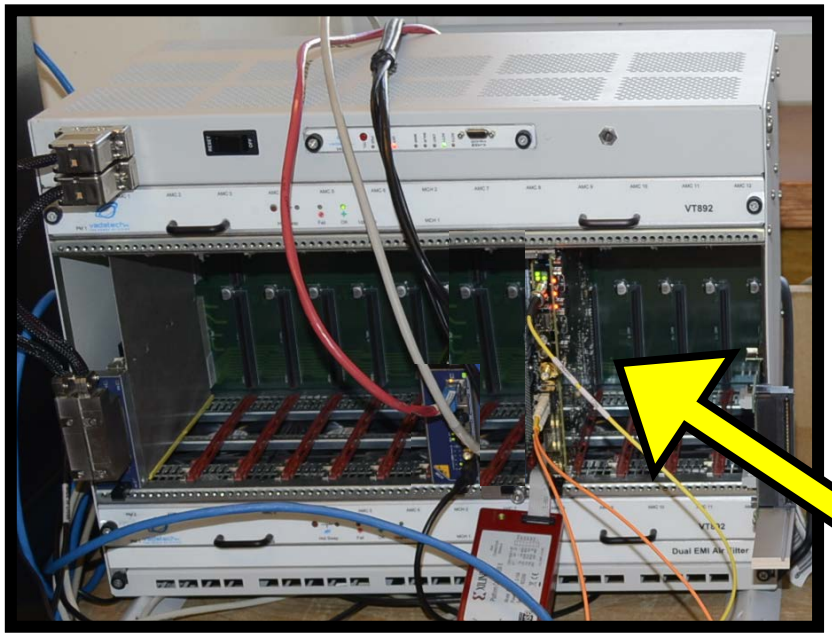
SFP+

Demonstration system overview (3 of 16)

Back-End System & DAQ



uTCA shelf



BE System

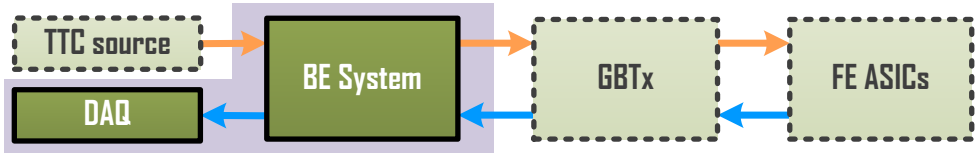
TTC FMC

GLIB AMC

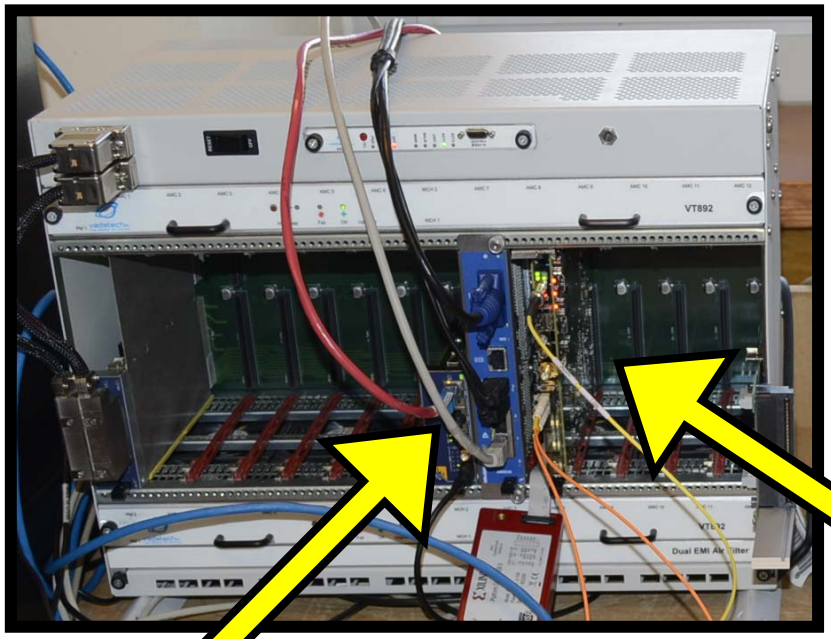
SFP+

Demonstration system overview (3 of 16)

Back-End System & DAQ



uTCA shelf



BE System

TTC FMC

GLIB AMC

DAQ

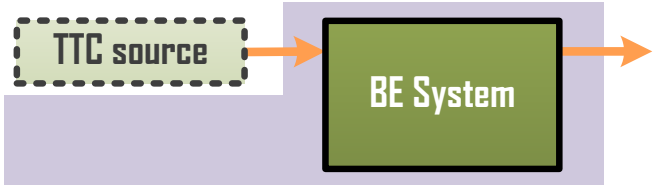
AMC Processor

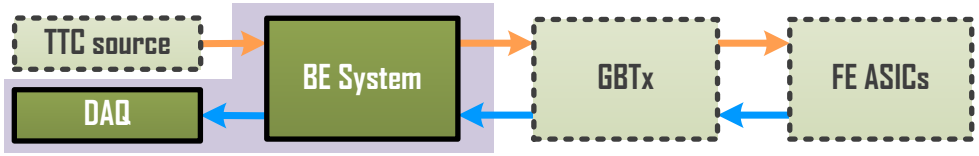
SFP+

Demonstration system overview (4 of 16)

Back-End System & DAQ

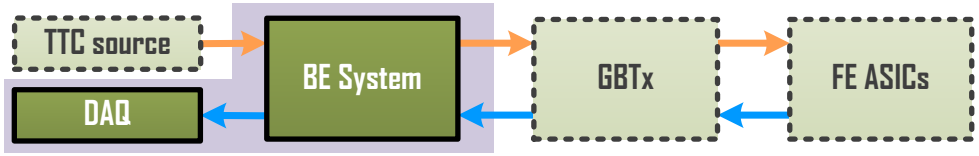
- TTC (downstream):



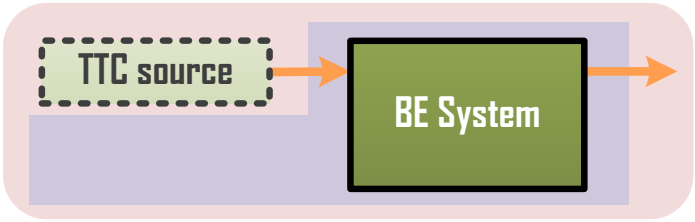


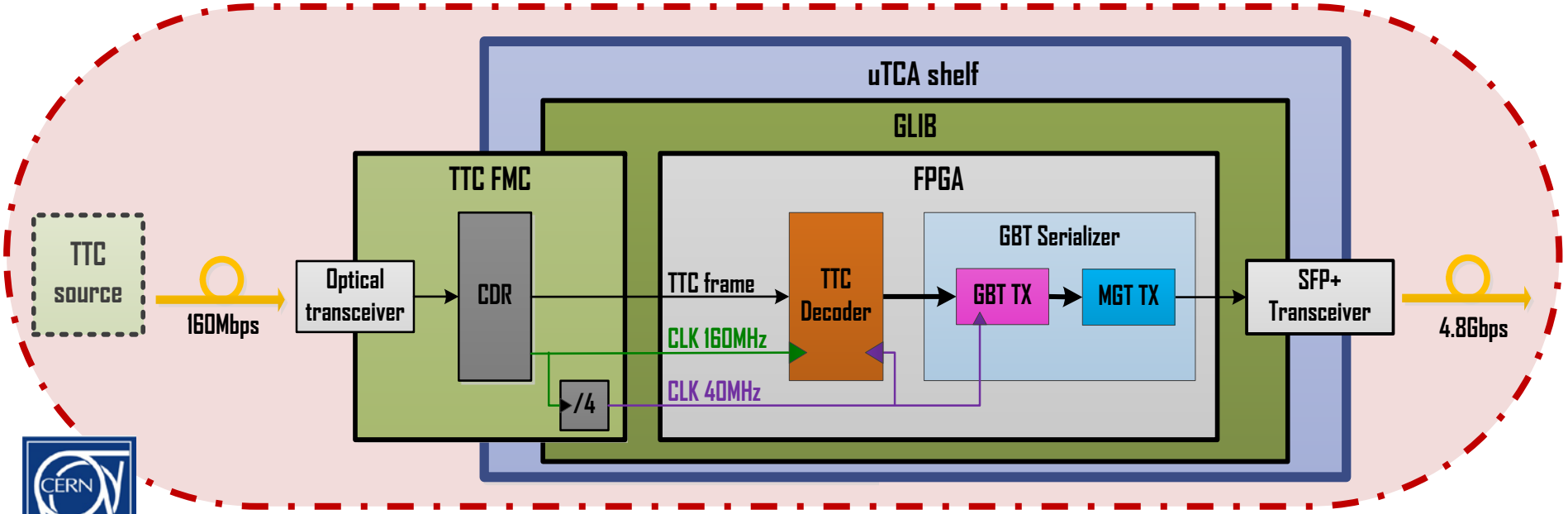
Demonstration system overview (4 of 16)

Back-End System & DAQ



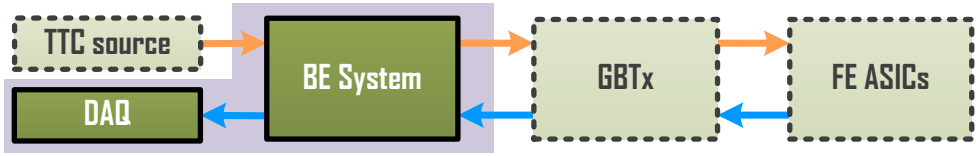
- TTC (downstream):



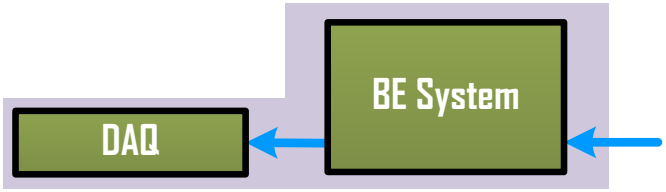


Demonstration system overview (5 of 16)

Back-End System & DAQ

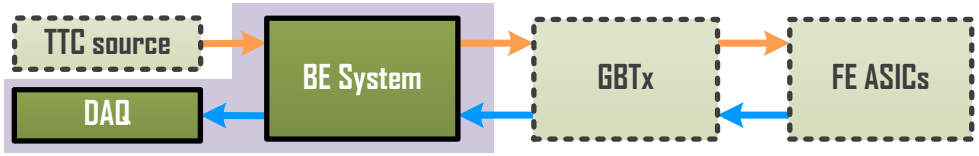


- DAQ (upstream):

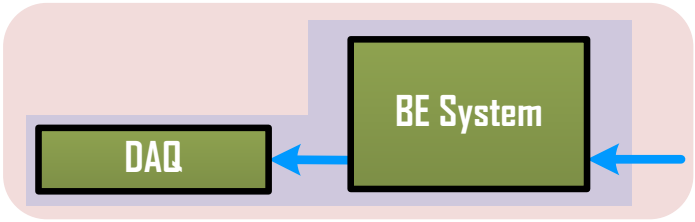


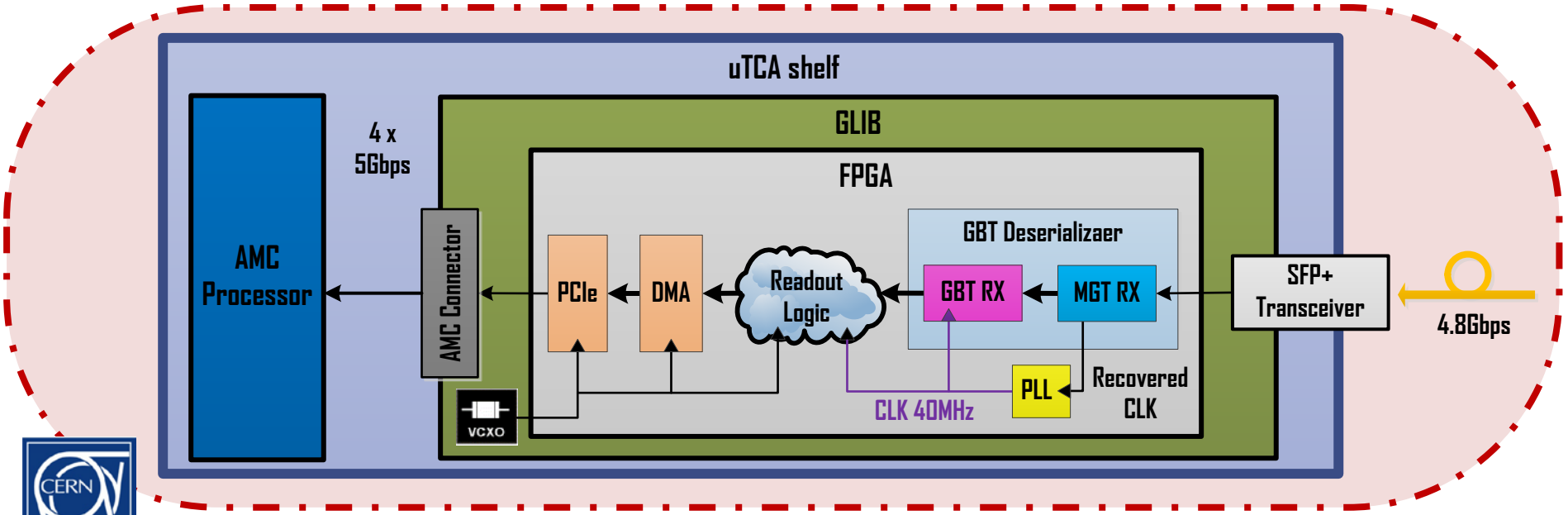
Demonstration system overview (5 of 16)

Back-End System & DAQ



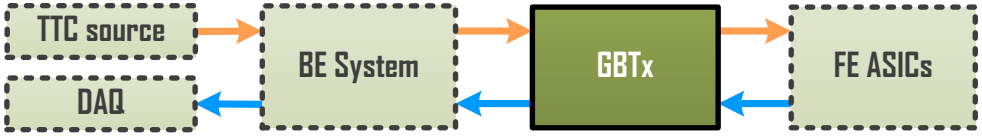
- DAQ (upstream):





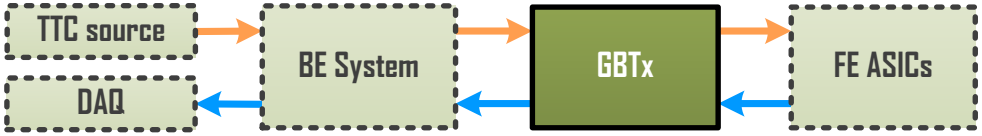
Demonstration system overview (6 of 16)

GBTx

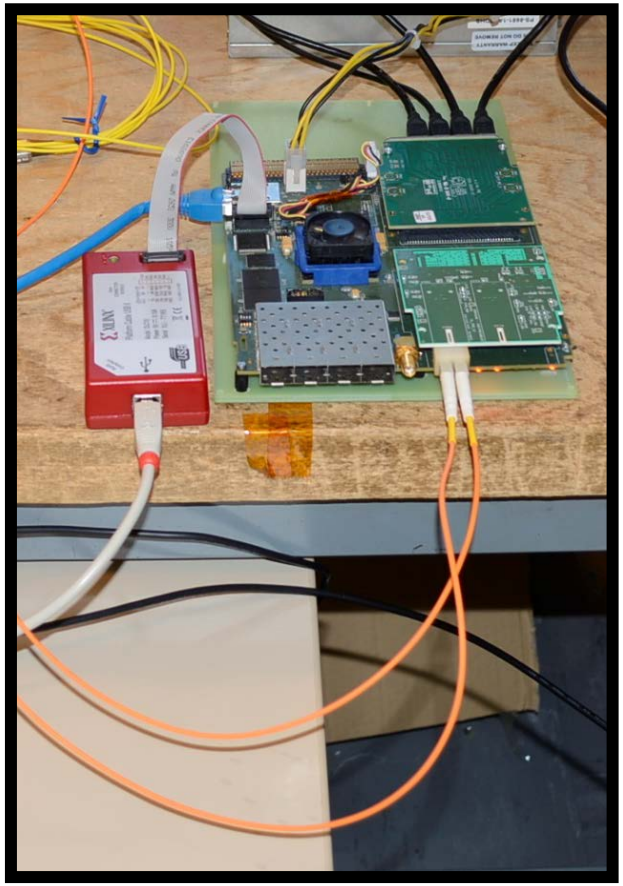


Demonstration system overview (6 of 16)

GBTx

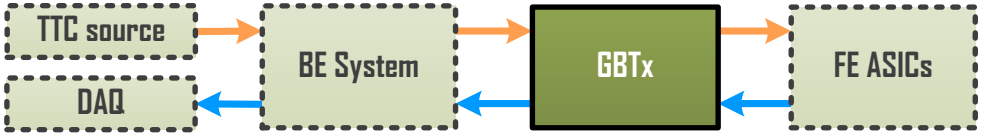


- Emulation:

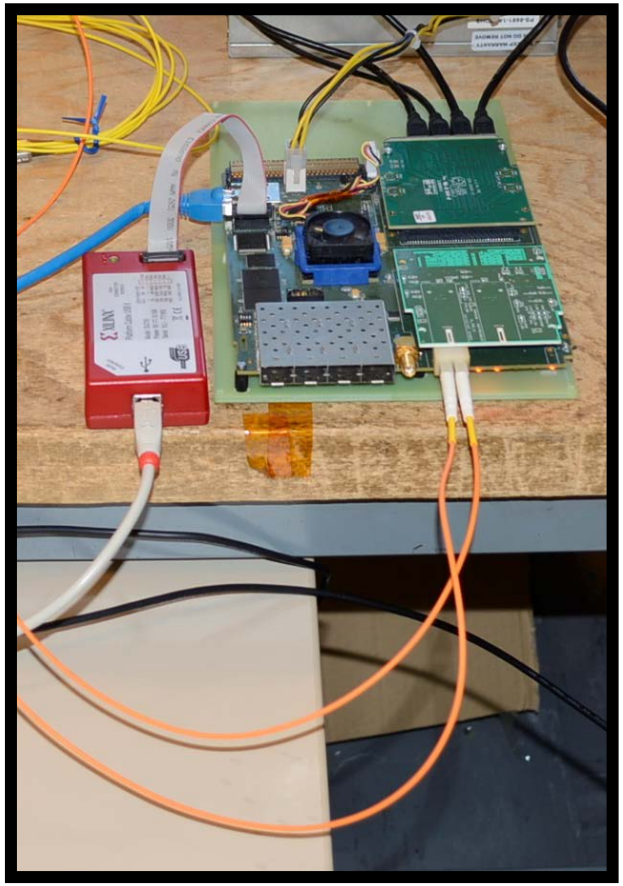


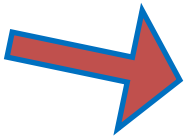
Demonstration system overview (6 of 16)

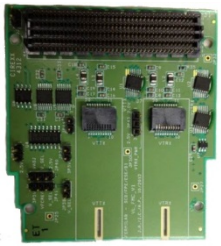
GBTx



- Emulation:



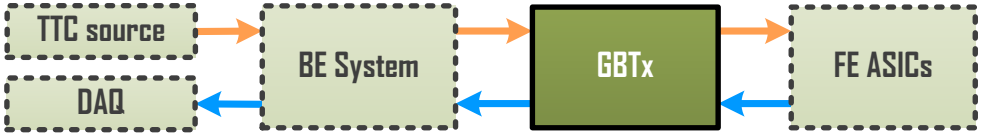




Demonstration system overview (7 of 16)

GBTx

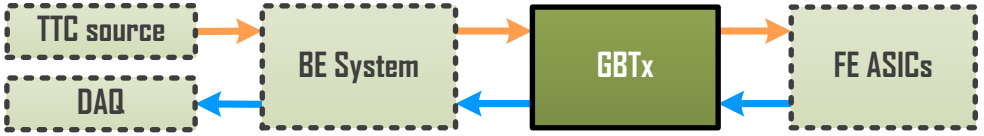
- Emulation:

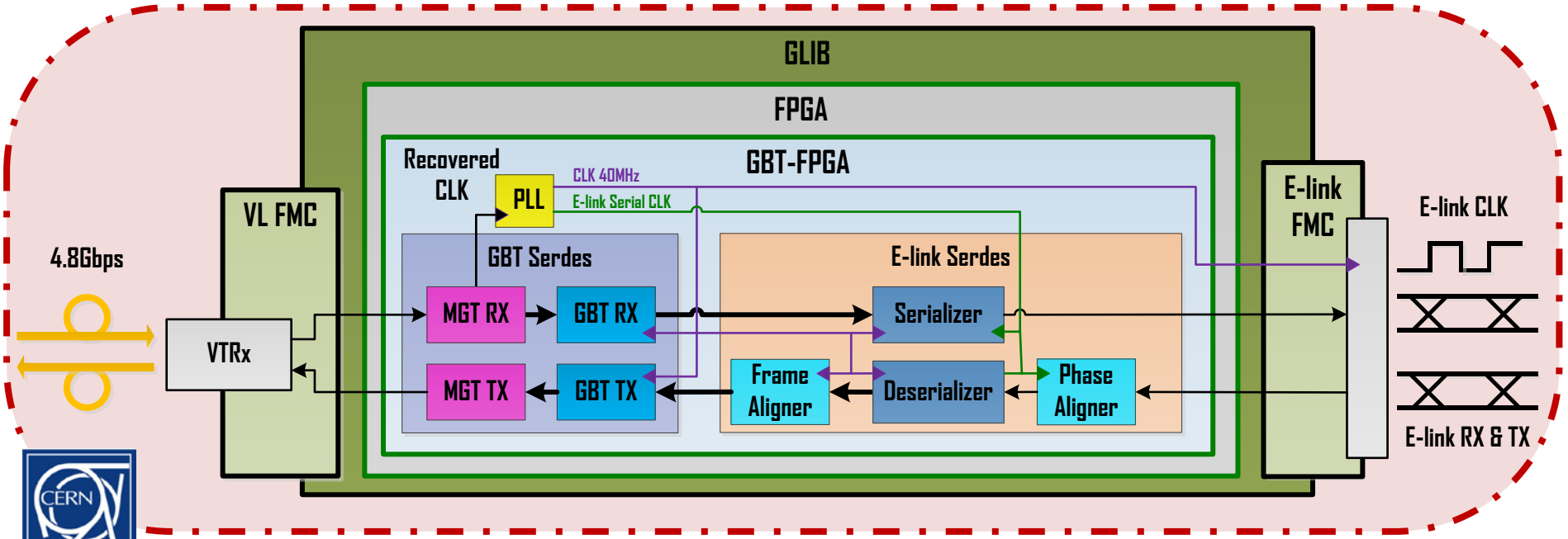


Demonstration system overview (7 of 16)

GBTx

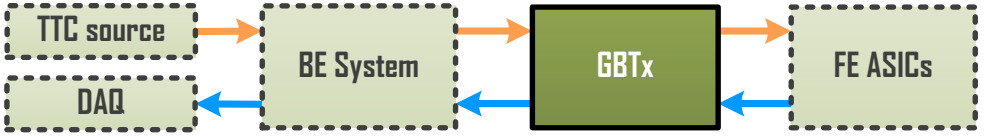
- Emulation:





Demonstration system overview (8 of 16)

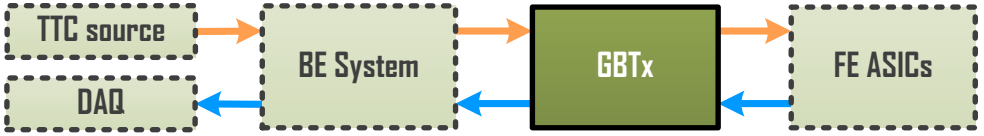
GBTx



SURPRISE !!

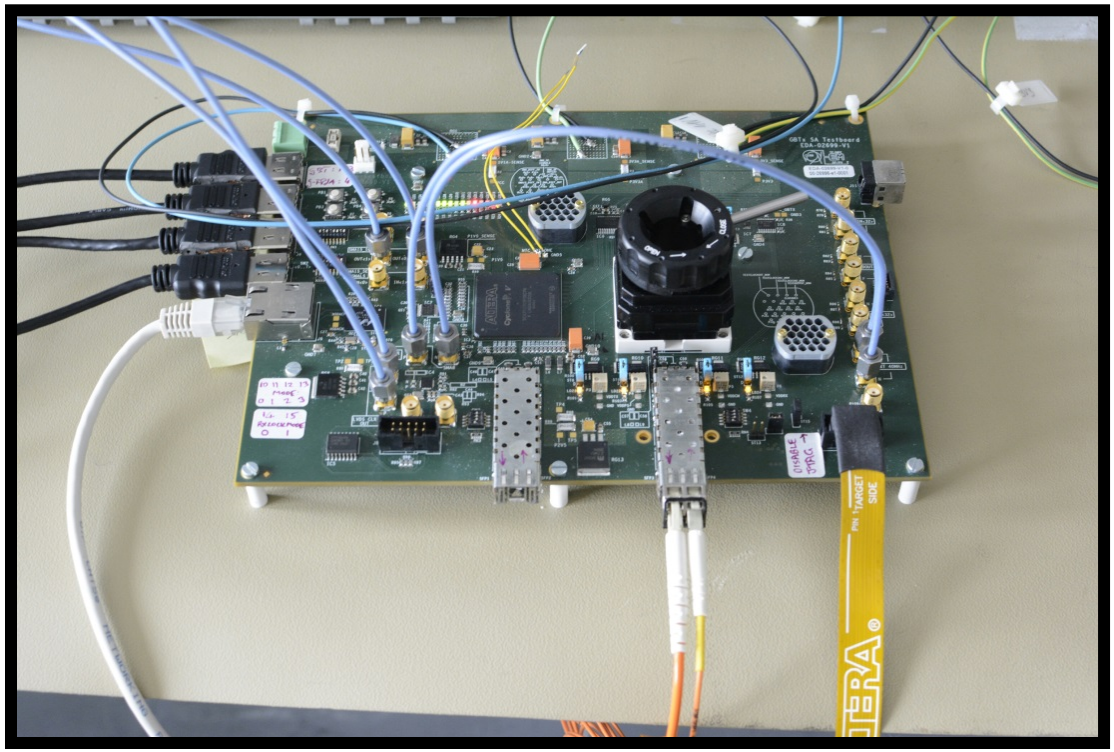
Demonstration system overview (9 of 16)

GBTx



- Use of GBTx ASIC:

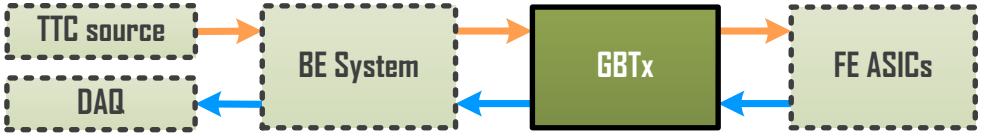
Stand Alone Test (SAT) board



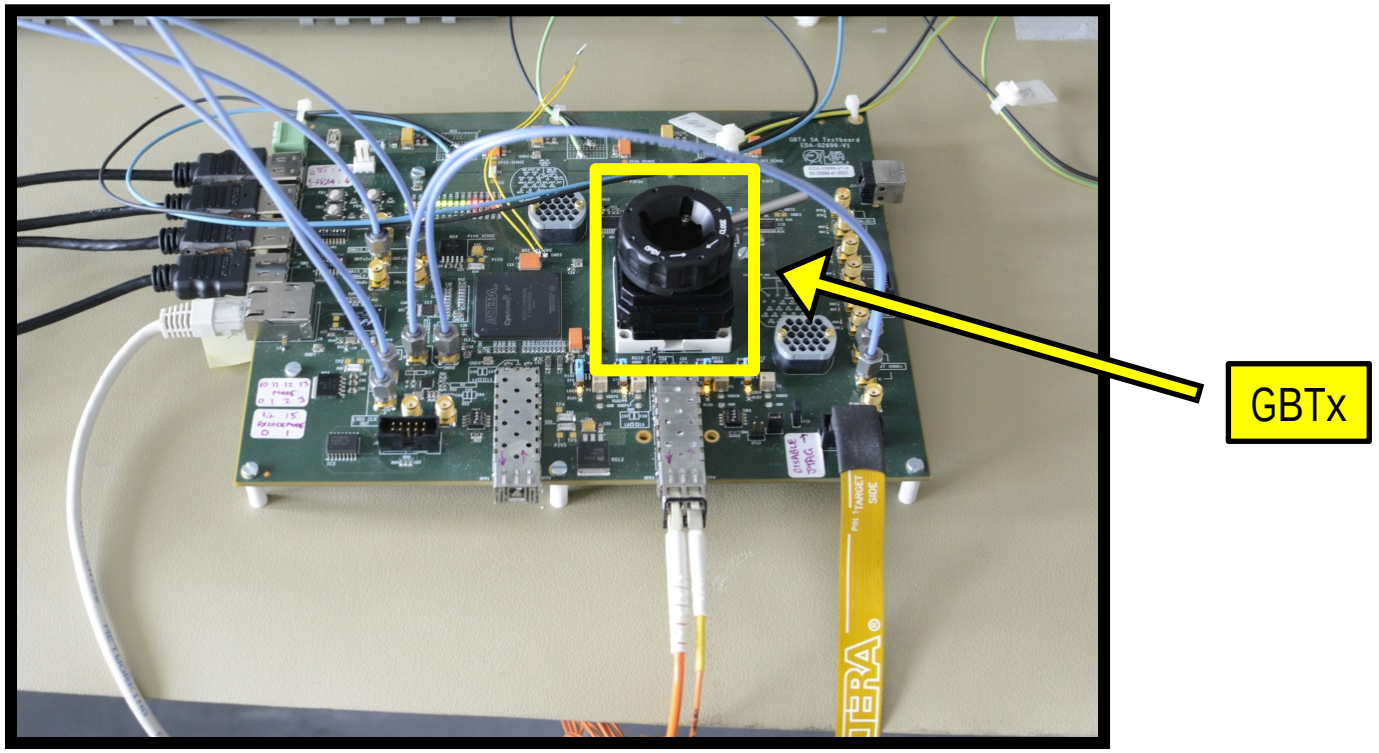
Demonstration system overview (9 of 16)

GBTx

- Use of GBTx ASIC:



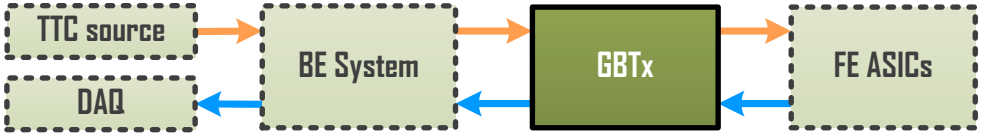
Stand Alone Test (SAT) board



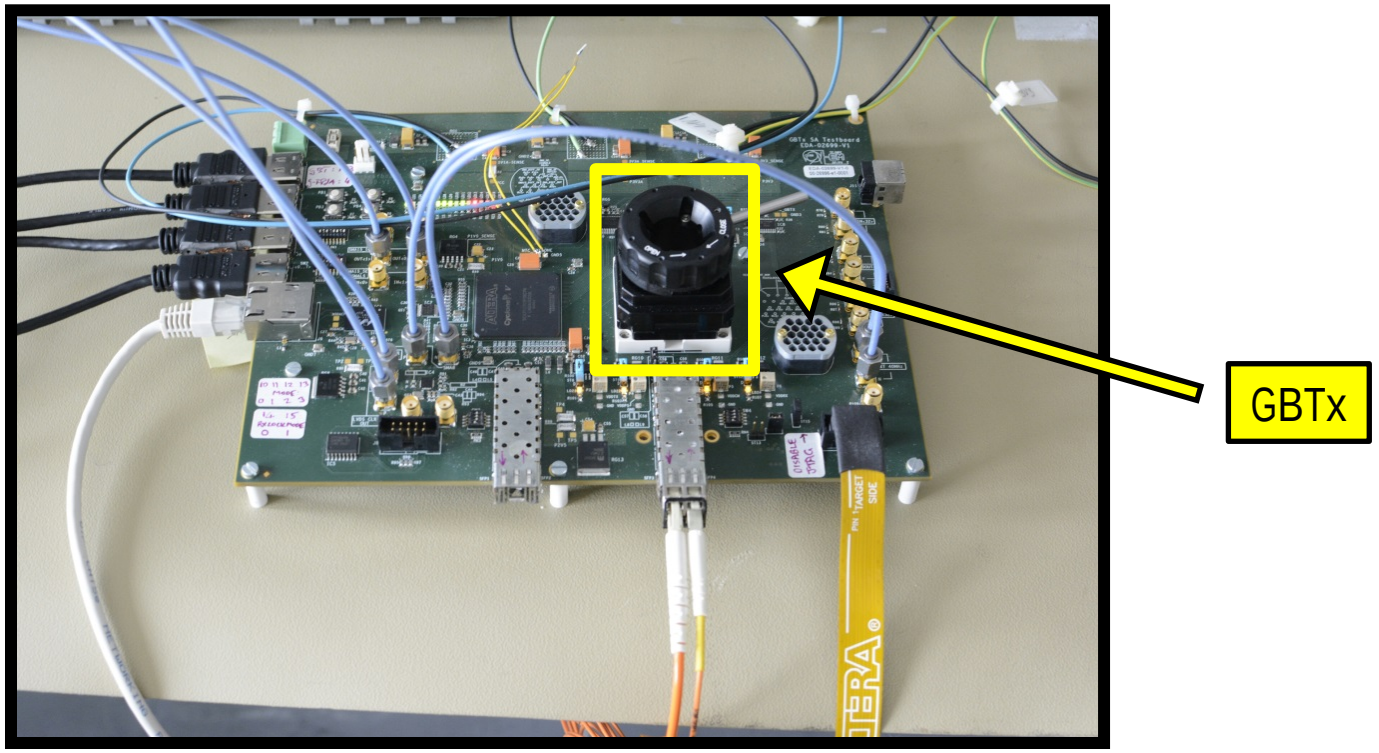
Demonstration system overview (9 of 16)

GBTx

- Use of GBTx ASIC:



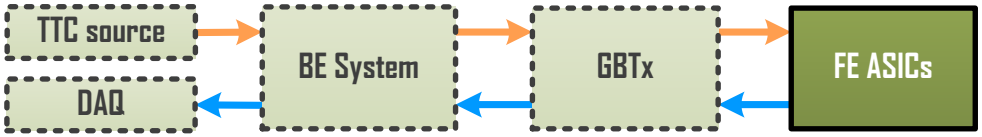
Stand Alone Test (SAT) board



First full system using a GBTx ASIC

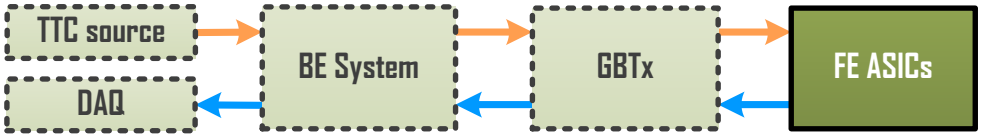
Demonstration system overview (10 of 16)

Front-End ASIC



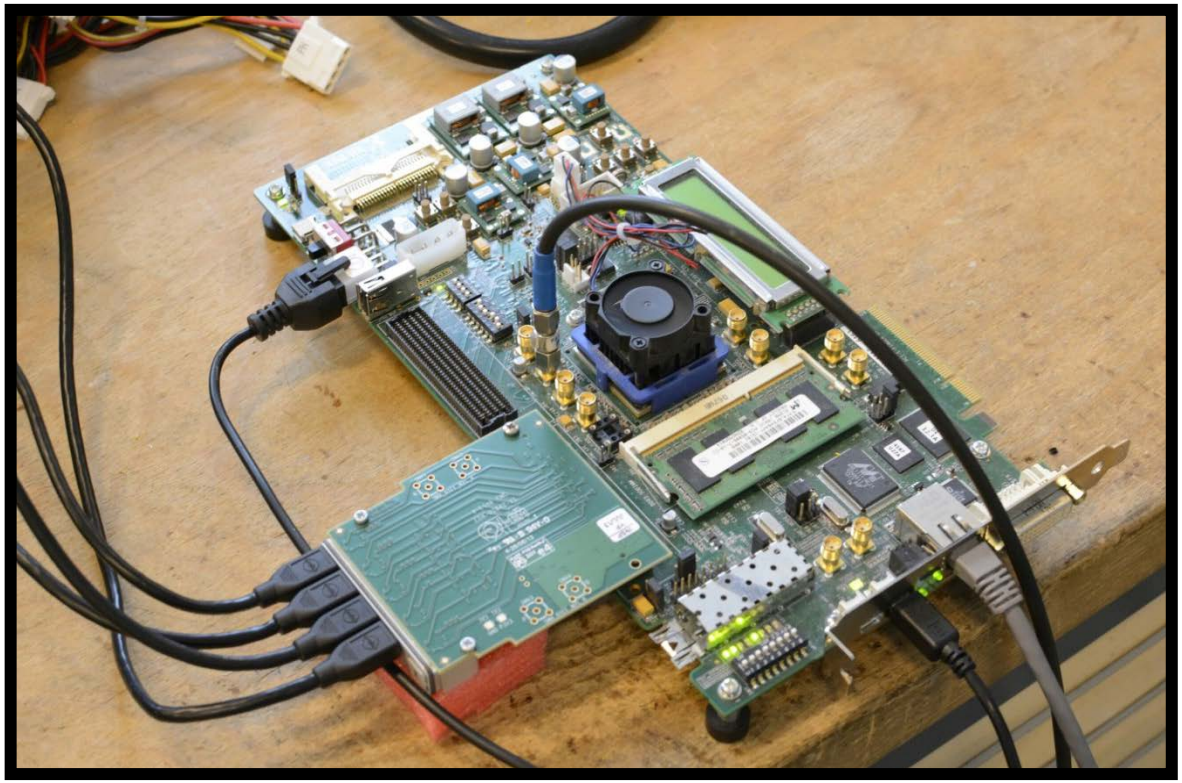
Demonstration system overview (10 of 16)

Front-End ASIC



- **Emulation:**

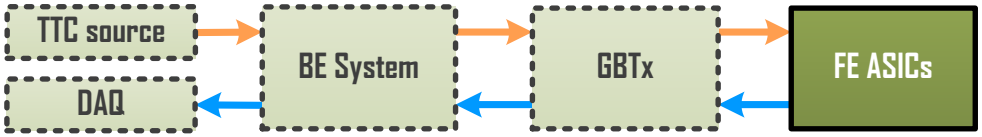
FPGA-based devkit



Demonstration system overview (11 of 16)

Front-End ASIC

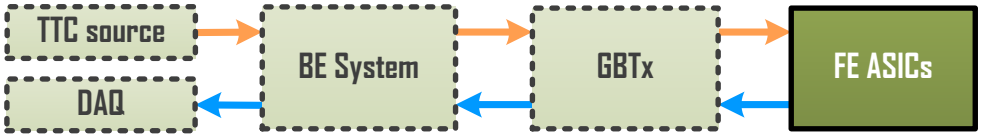
- Emulation:



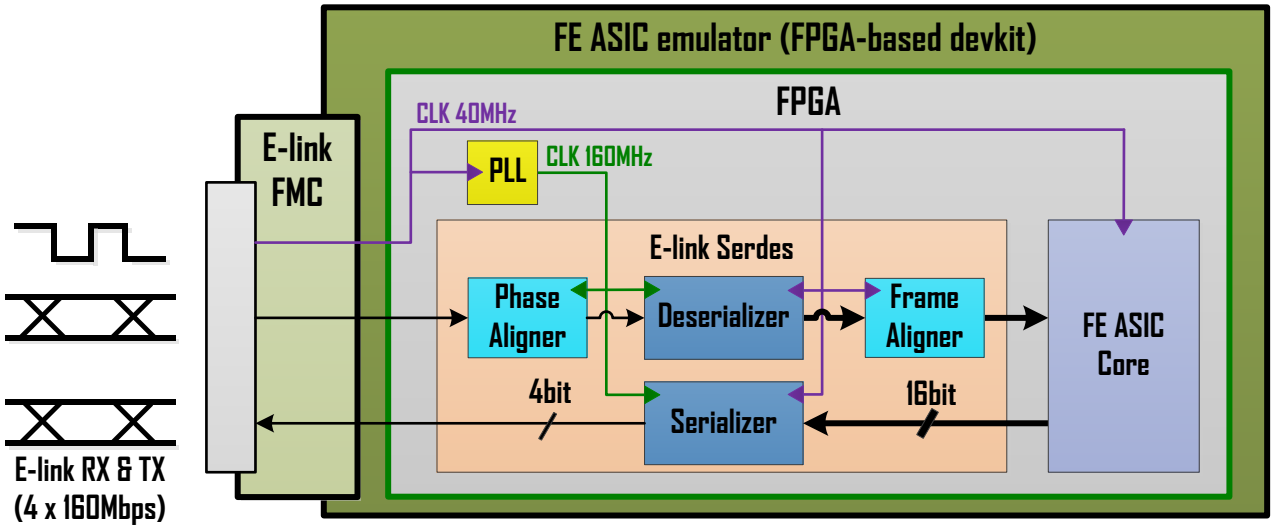
ASIC SPECS	
Line rate	640Mbps
Event size	512Byte
E-links	4@160Mbps

Demonstration system overview (11 of 16)

Front-End ASIC



- Emulation:

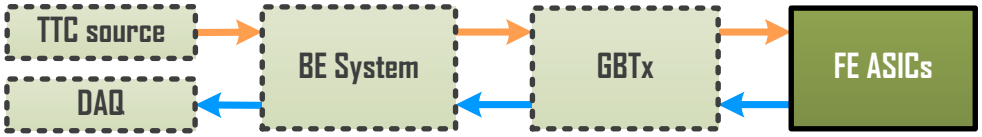


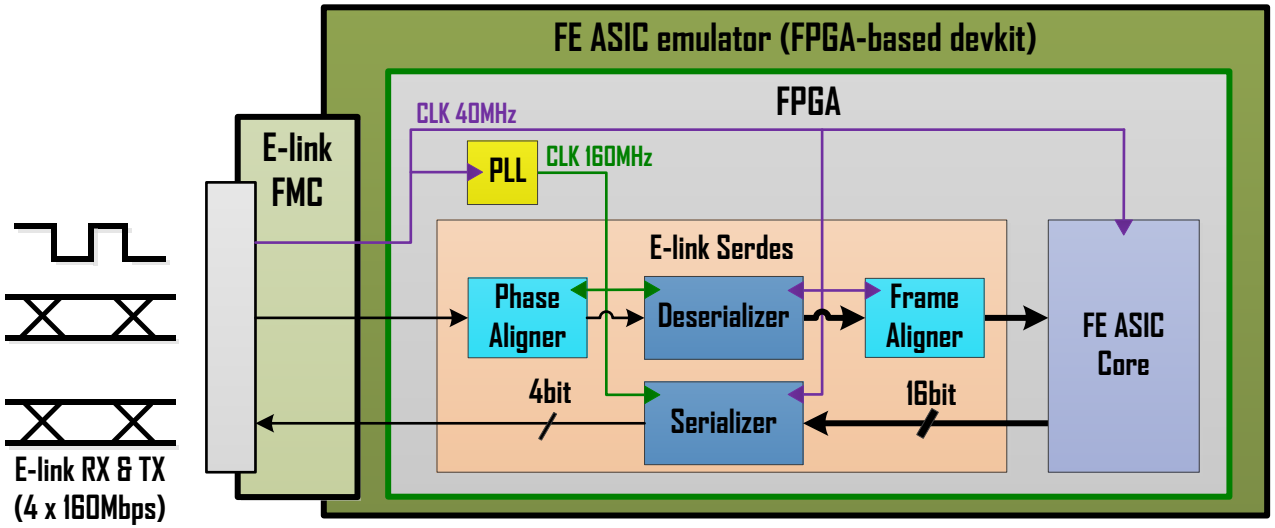
ASIC SPECS	
Line rate	640Mbps
Event size	512Byte
E-links	4@160Mbps

Demonstration system overview (11 of 16)

Front-End ASIC

- Emulation:



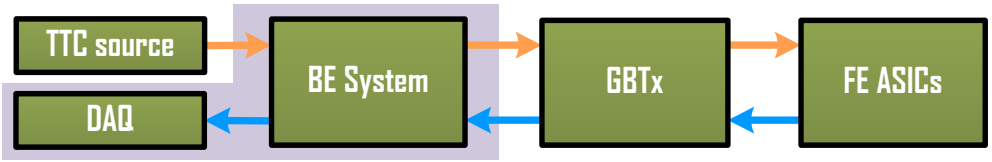


ASIC SPECS	
Line rate	640Mbps
Event size	512Byte
E-links	4@160Mbps

	READOUT DATA FRAME										
Word number	0	1	2	3	4	...	251	252	253	254	255
Word (16bit)	SOF (AAAAh)	Orbit Counter	Bunch Counter	Event Counter	Payload 0	...	Payload 247	STATUS	CRC	EOF 1 (BBBBh)	EOF 2 (CCCCh)

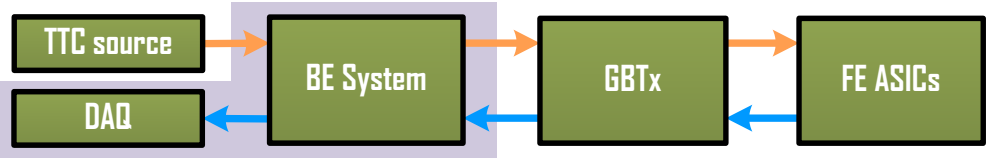
Demonstration system overview (12 of 16)

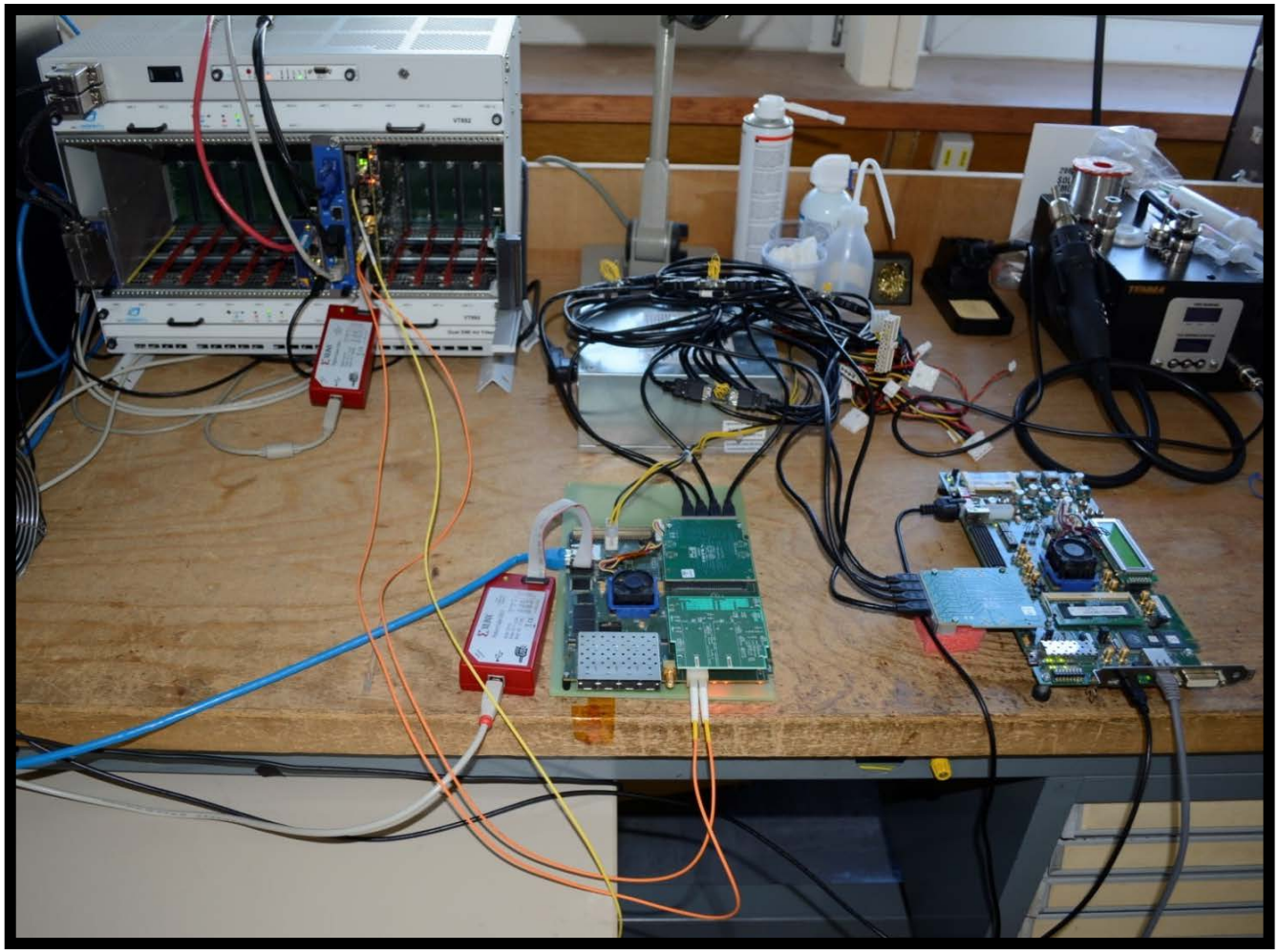
Implementation



Demonstration system overview (12 of 16)

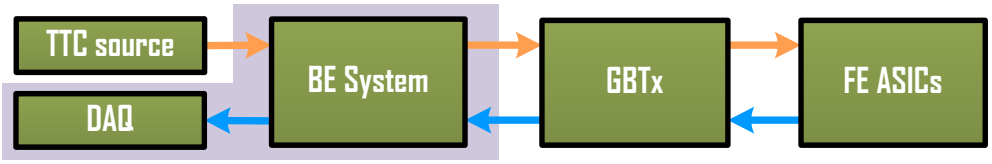
Implementation

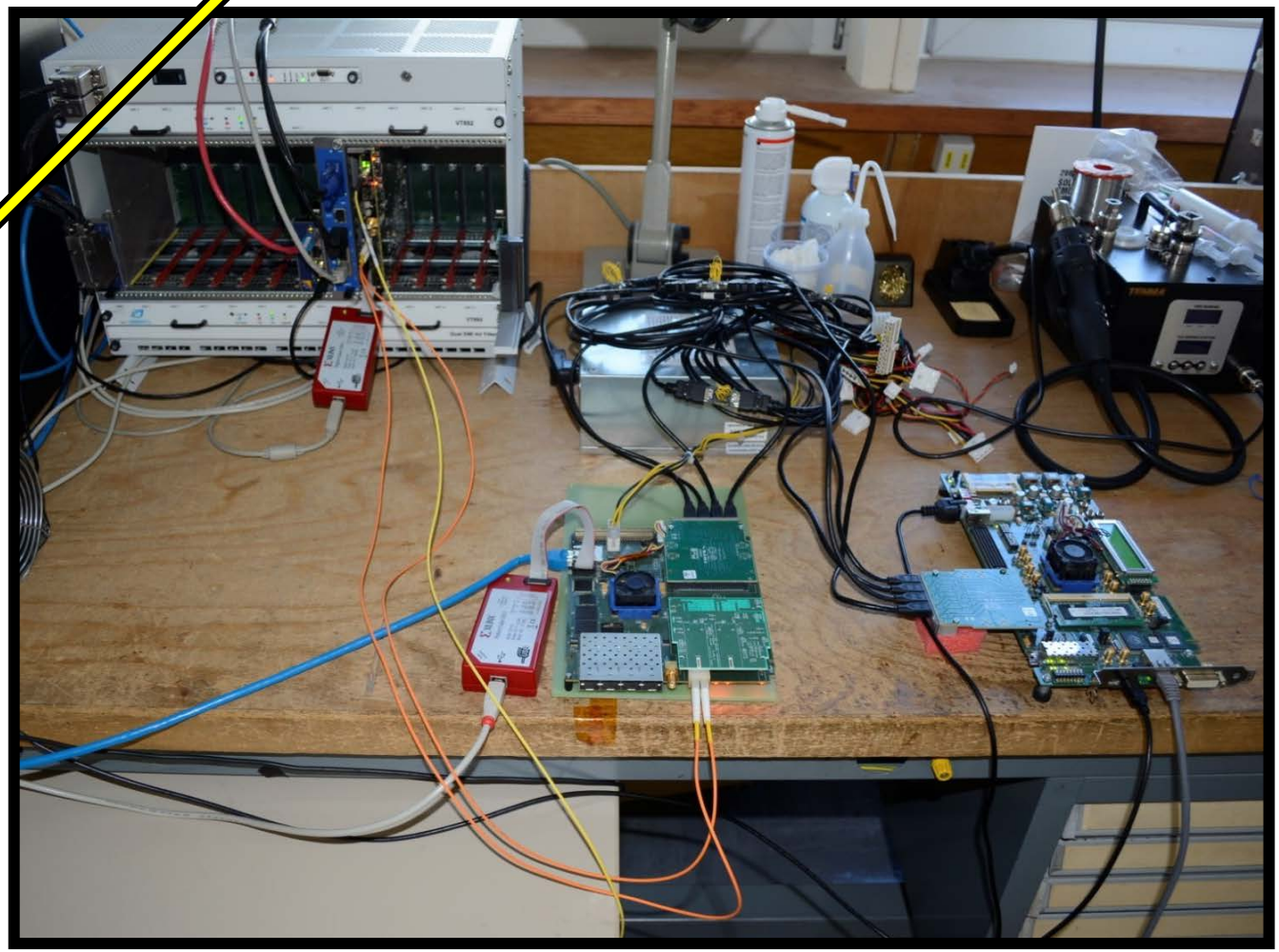




Demonstration system overview (12 of 16)

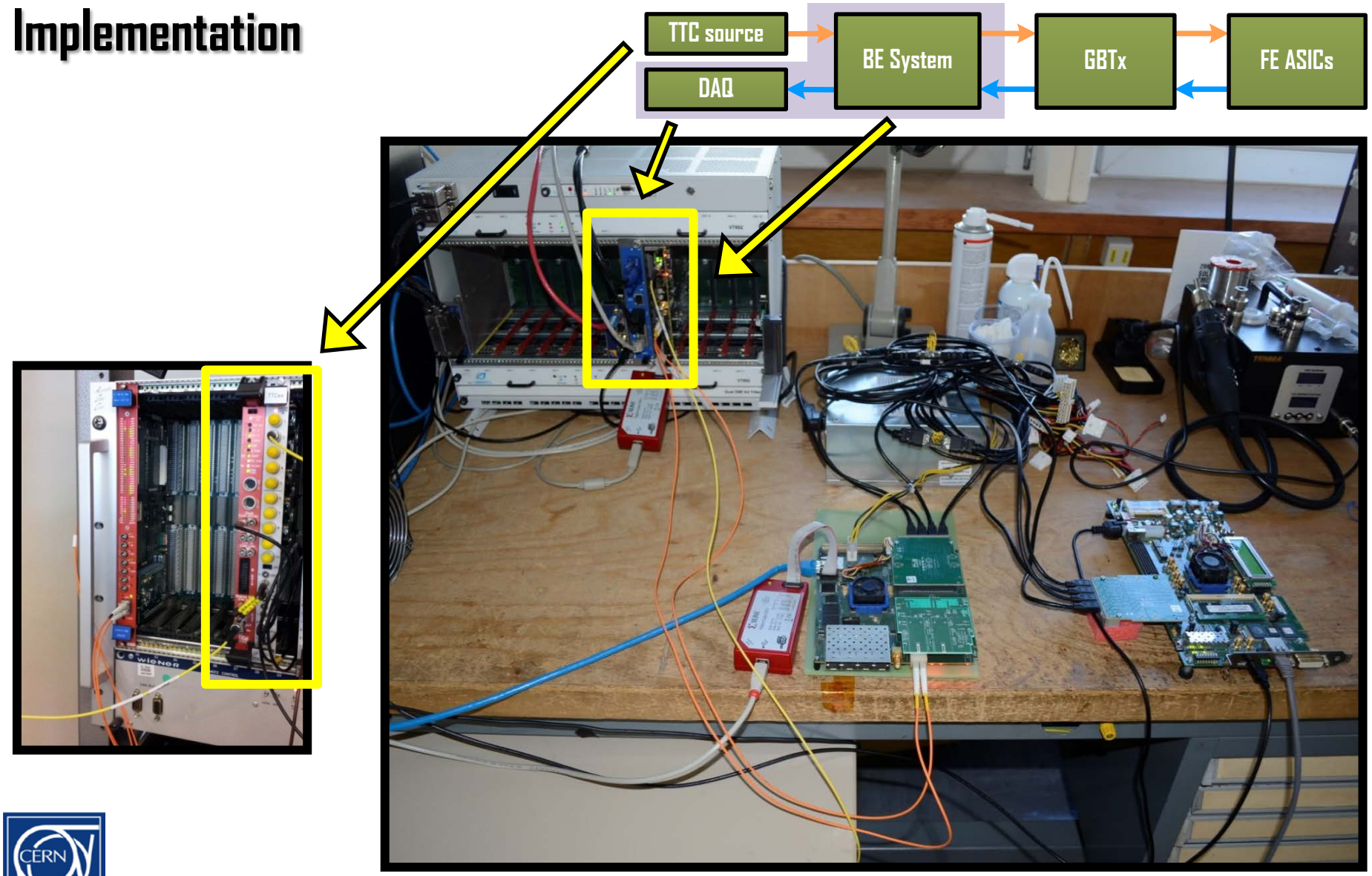
Implementation





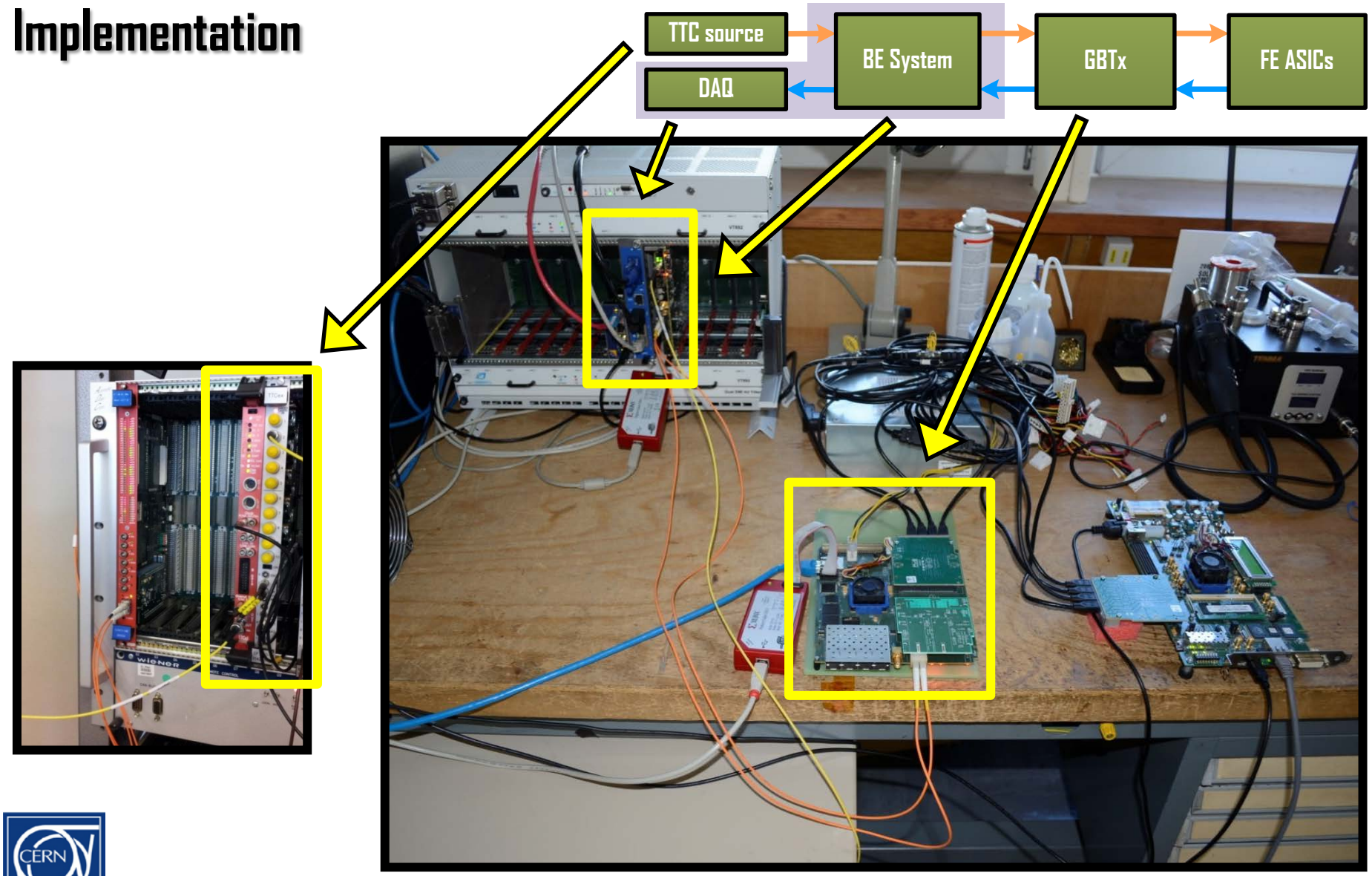
Demonstration system overview (12 of 16)

Implementation



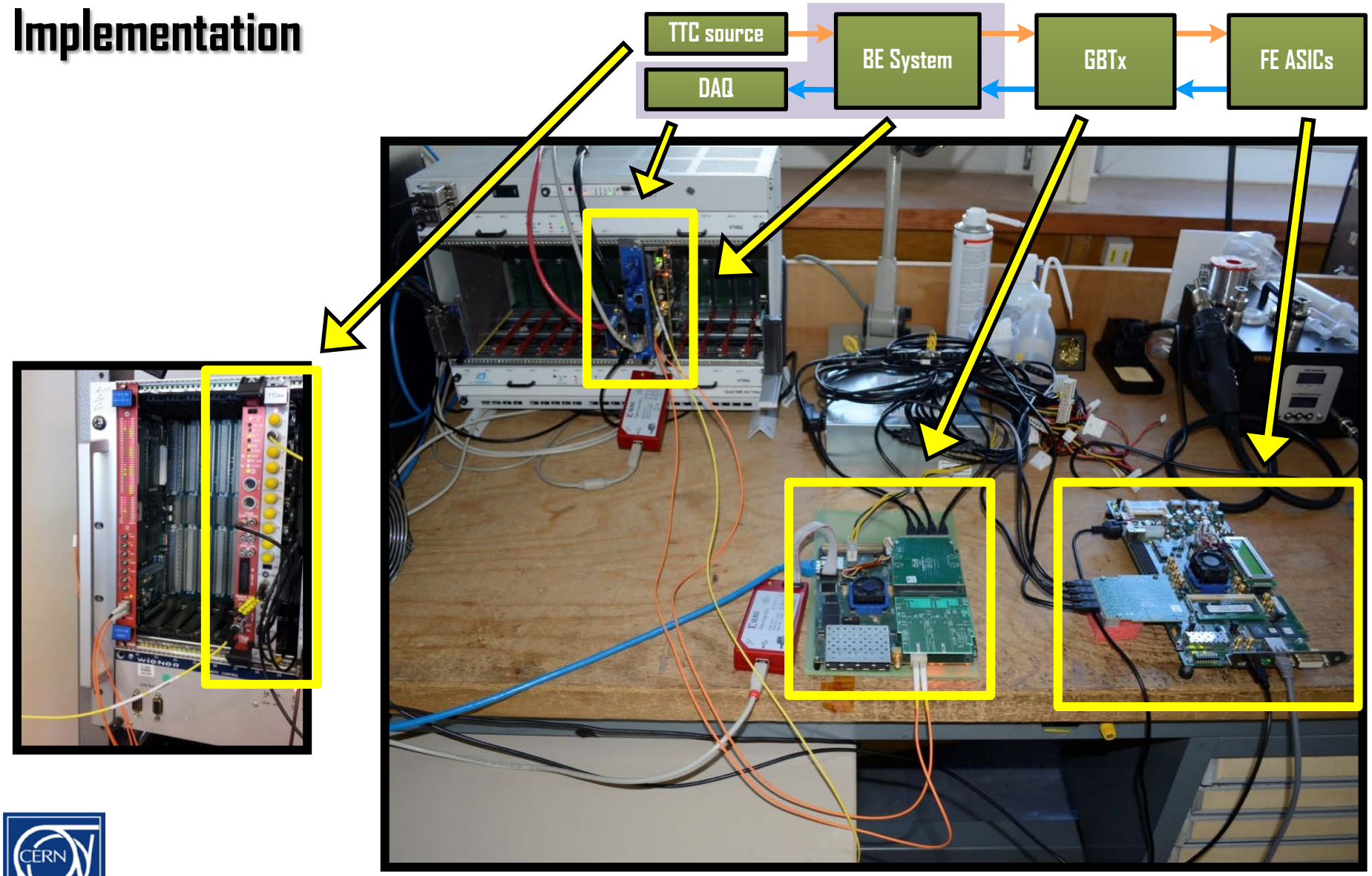
Demonstration system overview (12 of 16)

Implementation



Demonstration system overview (12 of 16)

Implementation



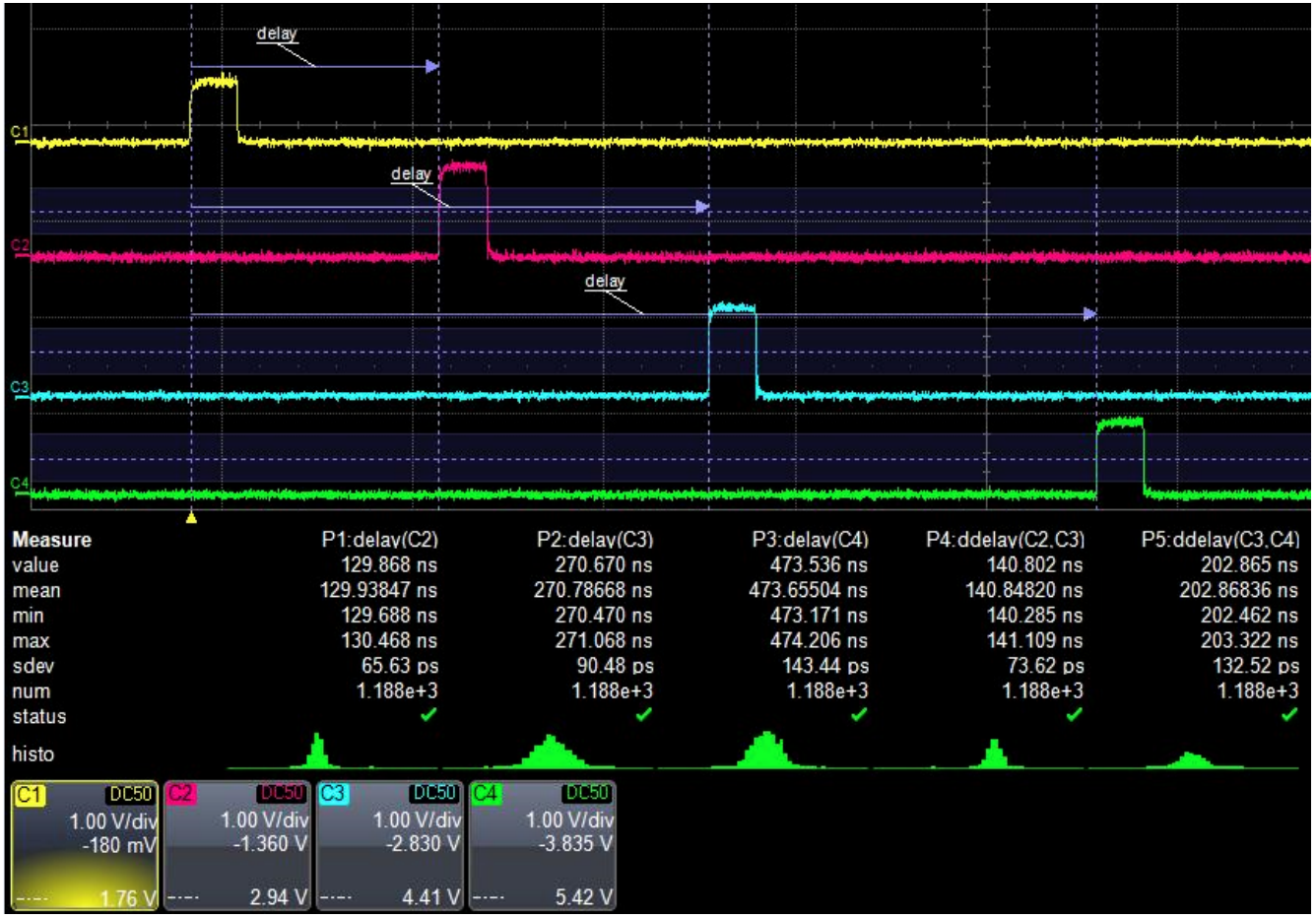
Demonstration system overview (13 of 16)

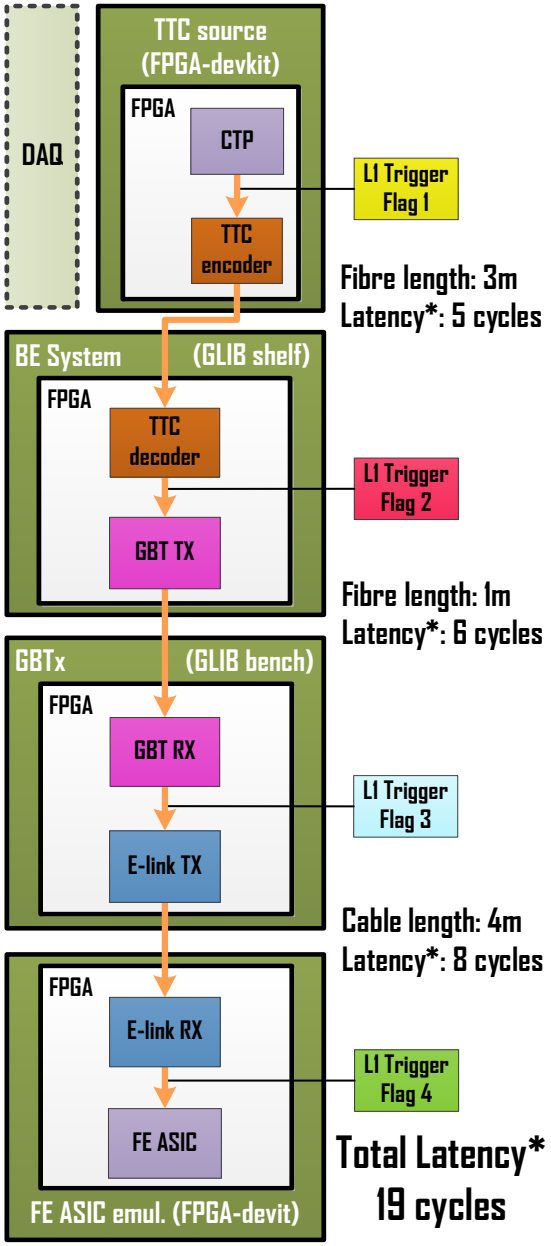
TTC phase & latency determinism

Demonstration system overview (13 of 16)

TTC phase & latency determinism

- Measurement flags & block diagram:



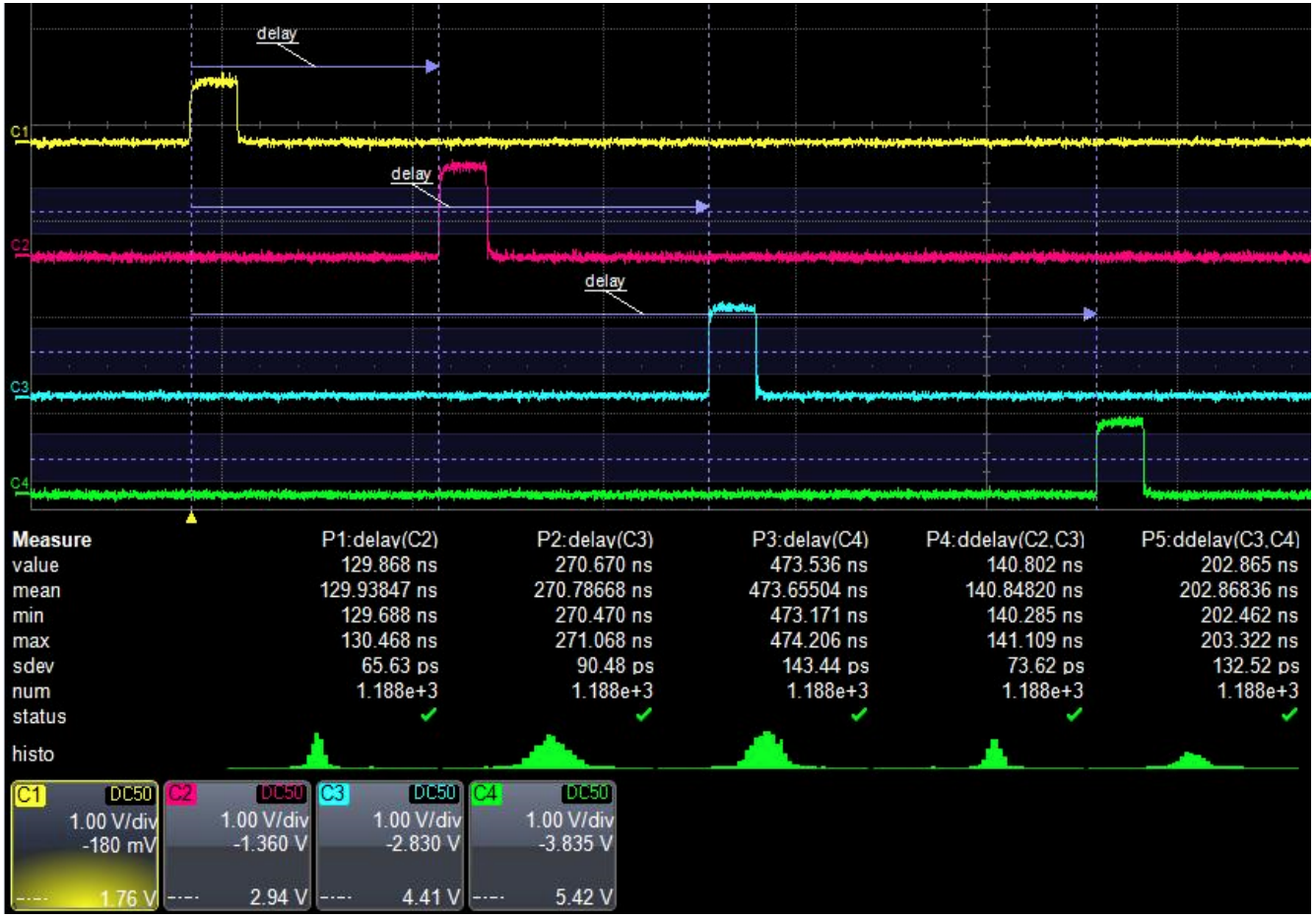


* Cycles of 25ns (40MHz)

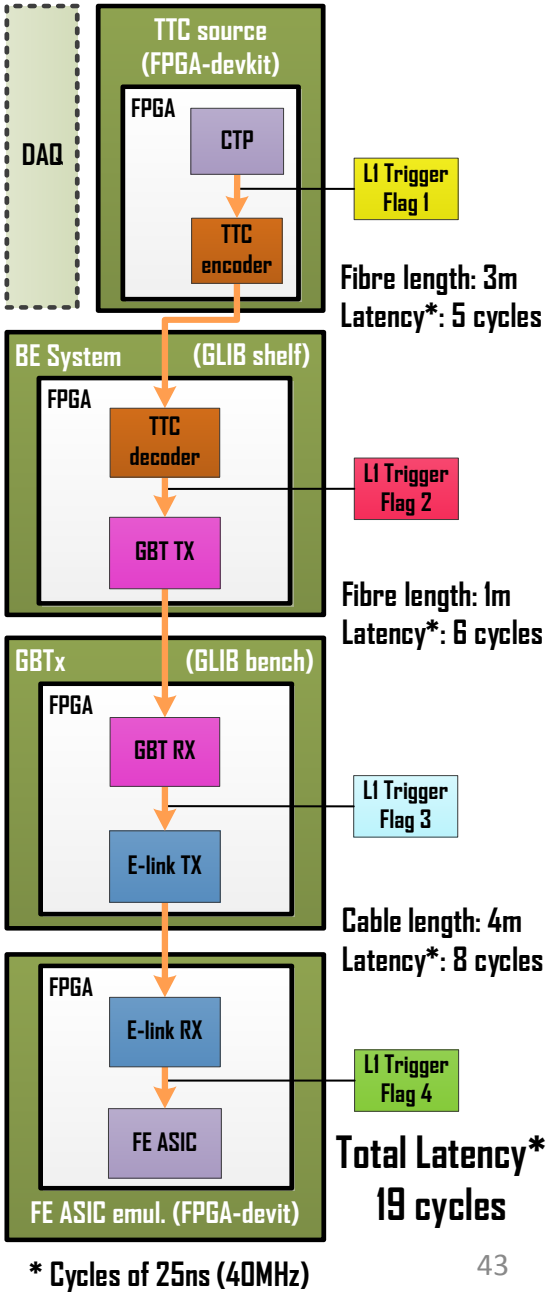
Demonstration system overview (13 of 16)

TTC phase & latency determinism

- Measurement flags & block diagram:



Measure	P1:delay(C2)	P2:delay(C3)	P3:delay(C4)	P4:ddelay(C2,C3)	P5:ddelay(C3,C4)
value	129.868 ns	270.670 ns	473.536 ns	140.802 ns	202.865 ns
mean	129.93847 ns	270.78668 ns	473.65504 ns	140.84820 ns	202.86836 ns
min	129.688 ns	270.470 ns	473.171 ns	140.285 ns	202.462 ns
max	130.468 ns	271.068 ns	474.206 ns	141.109 ns	203.322 ns
sdev	65.63 ps	90.48 ps	143.44 ps	73.62 ps	132.52 ps
num	1.188e+3	1.188e+3	1.188e+3	1.188e+3	1.188e+3
status	✓	✓	✓	✓	✓
histo					



Deterministic phase & latency
(intensive test procedures under development)

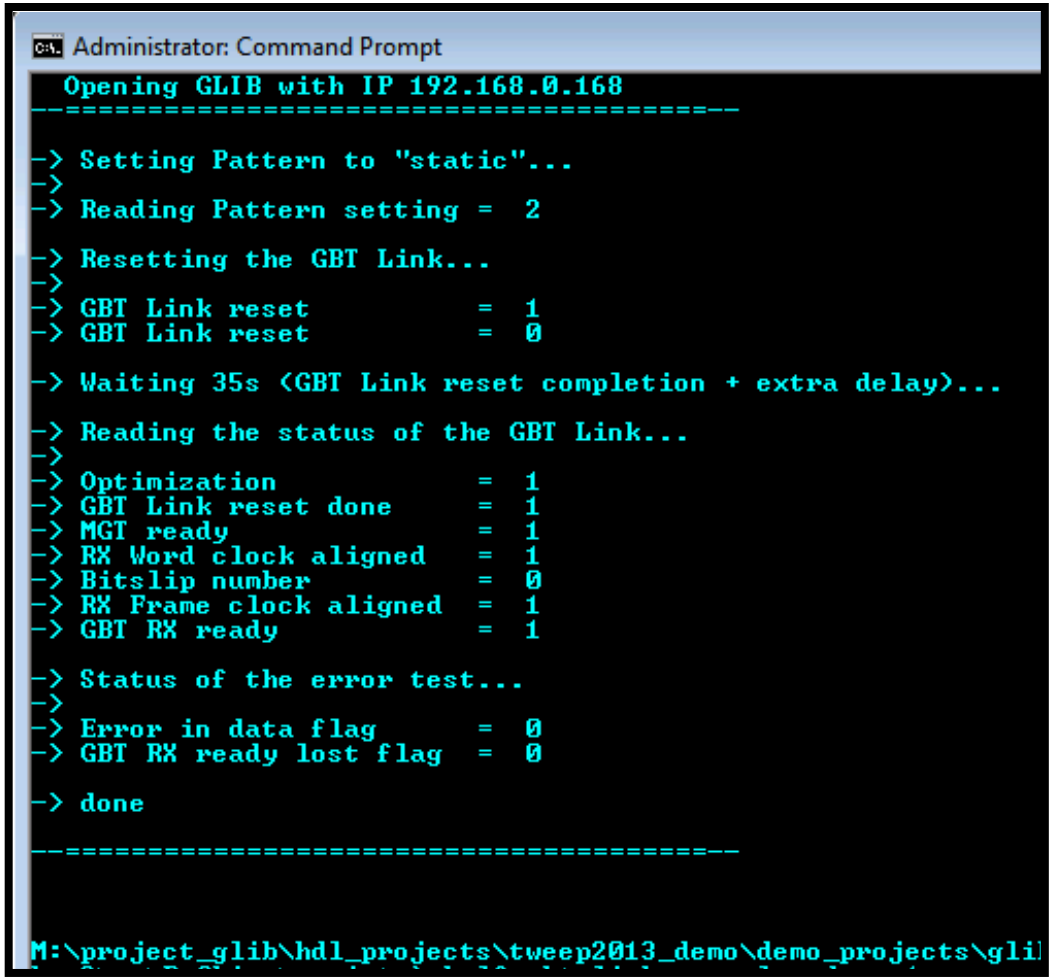
* Cycles of 25ns (40MHz)

Demonstration system overview (14 of 16)

Software

Software

- **Control:** IPbus-based software over Ethernet



Demonstration system overview (15 of 16)

Software

- **DAQ**: Custom software over PCIe

```
mbarrosm@pheseamc01:~
   ============================================================
   15 TWEPP demo
   ============================================================
   0 Quit
Your choice: [15] :

Final Version for TWEPP 2013

BAR2 is: 0x00000000f0400000
Data at offset 0 is 0x  cafe0000cafe00 (expected: 0x00cafe0000cafe00)
Data at offset 0 is 0x11ac1d1111ac1d11 (expected: 0x11ac1d1111ac1d11)
Data at offset 0 is 0x22babe2222babe22 (expected: 0x22babe2222babe22)
Data at offset 0 is 0x33beef3333beef33 (expected: 0x33beef3333beef33)
Continue? (1=yes, 0=no) :[0] :1

DMA buffer is at PCI address 0x       188000000

Enabling Readout...

Waiting for GLIB. data in register 8 = 0x               0
Waiting for GLIB. data in register 8 = 0x               0
Waiting for GLIB. data in register 8 = 0x               1

Start DMA transaction...

Waiting for DMA done. data in register 8 = 0x                0
Waiting for DMA done. data in register 8 = 0x                2

Decoding word 0 of frame 0
Start of frame: 0xaaaa
Orbit counter:  0xab55
Bunch counter:  0xb7ac
Event counter:  0xc70d
Decoding word 1 of frame 0
payload 1:      0xf118
payload 2:      0xf119
payload 3:      0xf11a
payload 4:      0xf11b
Decoding word 63 of frame 0
Status:         0xbabe
CRC:            0x93f5
EOF:            0xbbbb
```

Software

Demonstration system overview (15 of 16)

Software

- **DAQ**: Custom software over PCIe

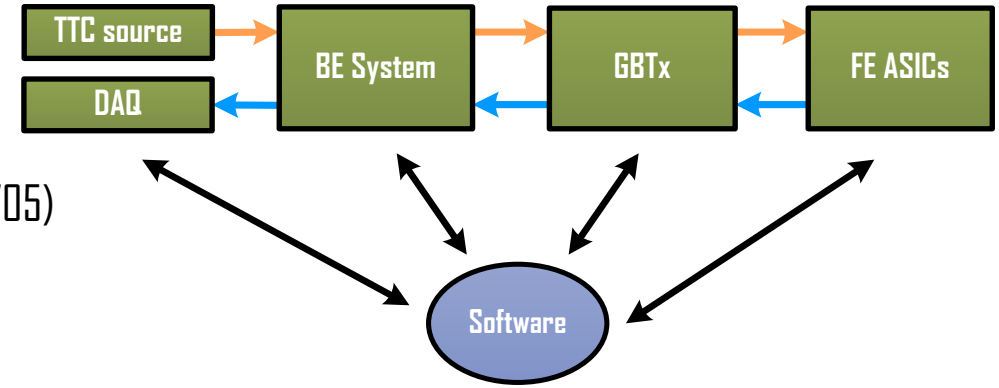
Software

```
mbarrosm@pheseamc01:~
   ============================================================
   15 TWEPP demo
   ============================================================
   0 Quit
Your choice: [15] :

Final Version for TWEPP 2013

BAR2 is: 0x00000000f0400000
Data at offset 0 is 0x  cafe0000cafe00 (expected: 0x00cafe0000cafe00)
Data at offset 0 is 0x11ac1d1111ac1d11 (expected: 0x11ac1d1111ac1d11)
Data at offset 0 is 0x22babe2222babe22 (expected: 0x22babe2222babe22)
Data at offset 0 is 0x33beef3333beef33 (expected: 0x33beef3333beef33)
Continue? (1=yes, 0=no) :[0] :1

DMA buffer is at PCI address 0x       188000000

Enabling Readout...

Waiting for GLIB. data in register 8 = 0x                0
Waiting for GLIB. data in register 8 = 0x                0
Waiting for GLIB. data in register 8 = 0x                1

Start DMA transaction...

Waiting for DMA done. data in register 8 = 0x                0
Waiting for DMA done. data in register 8 = 0x                2

Decoding word 0 of frame 0
Start of frame: 0xaaaa
Orbit counter:  0xab55
Bunch counter:  0xb7ac
Event counter:  0xc70d
Decoding word 1 of frame 0
payload 1:      0xf118
payload 2:      0xf119
payload 3:      0xf11a
payload 4:      0xf11b
Decoding word 63 of frame 0
Status:         0xbabe
CRC:            0x93f5
EOF:            0xbbbb
```

Readout Data Frame

Demonstration system overview (16 of 16)

List of components



- **TTC source:**
  - TTCci + TTCex **OR** FPGA-based devkit (Xilinx KC705)
- **Back-End System & DAQ:**
  - GLIB AMC + TTC FMC + SFP+
  - uTCA crate (Vadatech VT892)
  - AMC Processor (Kontron AM5030)
  - MCH (NAT-MCH Gen3 PCIe)
  - Power Module (NAT-PM-DC780)
- **GBTx:**
  - GLIB AMC + VL FMC + VTRx + E-link FMC **OR** SAT board (GBTx ASIC on-board)
- **Front-End ASICs:**
  - FPGA-based devkit (Xilinx ML605) + E-link FMC
- **Software**
  - Control: IPbus over Ethernet
  - DAQ: Custom software over PCIe

A GLIB-based uTCA demonstration system for HEP experiments

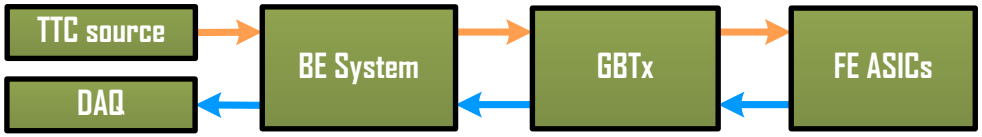
Outline:

- Introduction
- Demonstration system overview
- Summary & Outlook
- Acknowledgements & References

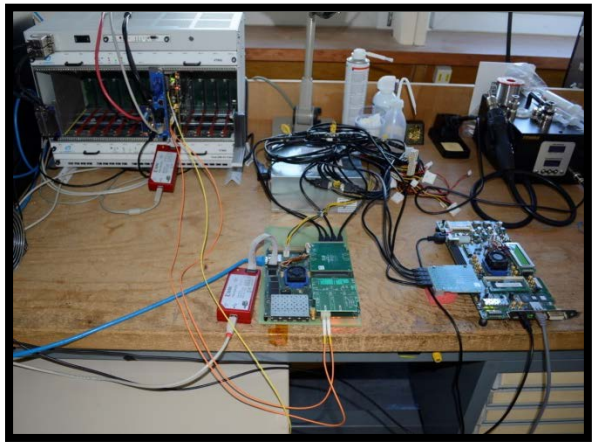
PH-ESE-BE

Hands-on the new link for LHC upgrades

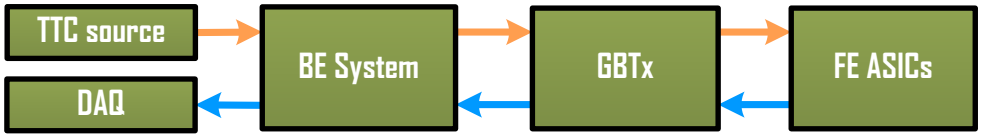
Summary & Outlook



- **Summary:**
  - First full system implementation using the new link for LHC upgrades.
  - First use of the GBTx ASIC in a full system.
  - Effective use of generic GLIB as BE and FE.
  - Successful combination of resources provided by various projects.
  - Managed to overcome numerous technical challenges.

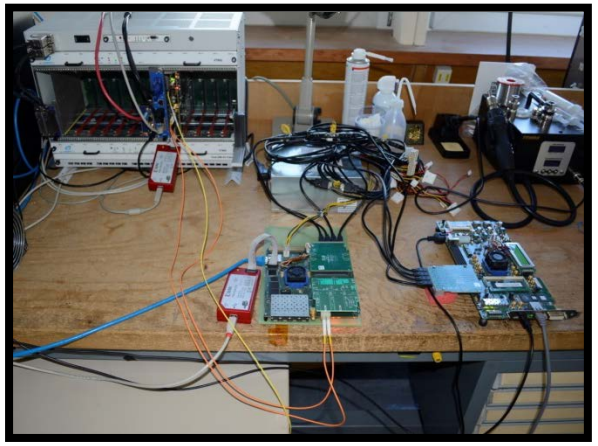


Summary & Outlook



- **Summary:**
  - First full system implementation using the new link for LHC upgrades.
  - First use of the GBTx ASIC in a full system.
  - Effective use of generic GLIB as BE and FE.
  - Successful combination of resources provided by various projects.
  - Managed to overcome numerous technical challenges.

- **Outlook:**
  - Conclude determinism studies.
  - Gradually upgrade the setup with real components.
  - Starting point for testing and/or commissioning systems
  - Realistic chain for lab and beam tests.



A GLIB-based uTCA demonstration system for HEP experiments

Outline:

- Introduction
- Demonstration system overview
- Summary & Outlook
- Acknowledgements & References

PH-ESE-BE

Hands-on the new link for LHC upgrades

Acknowledgements

- **GBT team**
- **IPbus team**
- **TTC team**
- **Versatile Link team**
- **xTCA Evaluation team**
- **Special thanks:**
  - For your help with the GBTx ASIC:
    - Sebastian Stefan Feger
    - Pedro Miguel Vicente Leitao
    - Ken Wyllie
  - For your support:
    - Paschalis Vichoudis
    - Sophie Baron

References

GLIB project:

- Main site: https://espace.cern.ch/project-GBLIB/public/default.aspx
- SVN repository: https://svn.cern.ch/reps/ph-ese/be/amc_glib
- Contact: glib-team@cern.ch

GBT project:

- Main site: http://cern.ch/proj-gbt
- Contact: Paulo.Moreira@cern.ch

GBT-FPGA project:

- Main site: http://cern.ch/proj-gbt/gbt-fpga
- SVN repository: https://svn.cern.ch/reps/ph-ese/be/gbt_fpga
- Contact: Sophie.Baron@cern.ch **OR** manoel.barros.marin@cern.ch

IPbus project:

- Main site: https://cactus.hepforge.org/index.php
- SVN repository: http://svn.cern.ch/reps/cactus/trunk/components/ipbus
- Contact: cactus@projects.hepforge.org

TTC project:

- Main site: https://espace.cern.ch/TTC2/TTCPage1/default.aspx
- SVN repository: https://svn.cern.ch/reps/ph-ese/be/ttc
- Contact: Sophie.Baron@cern.ch

Versatile Link project:

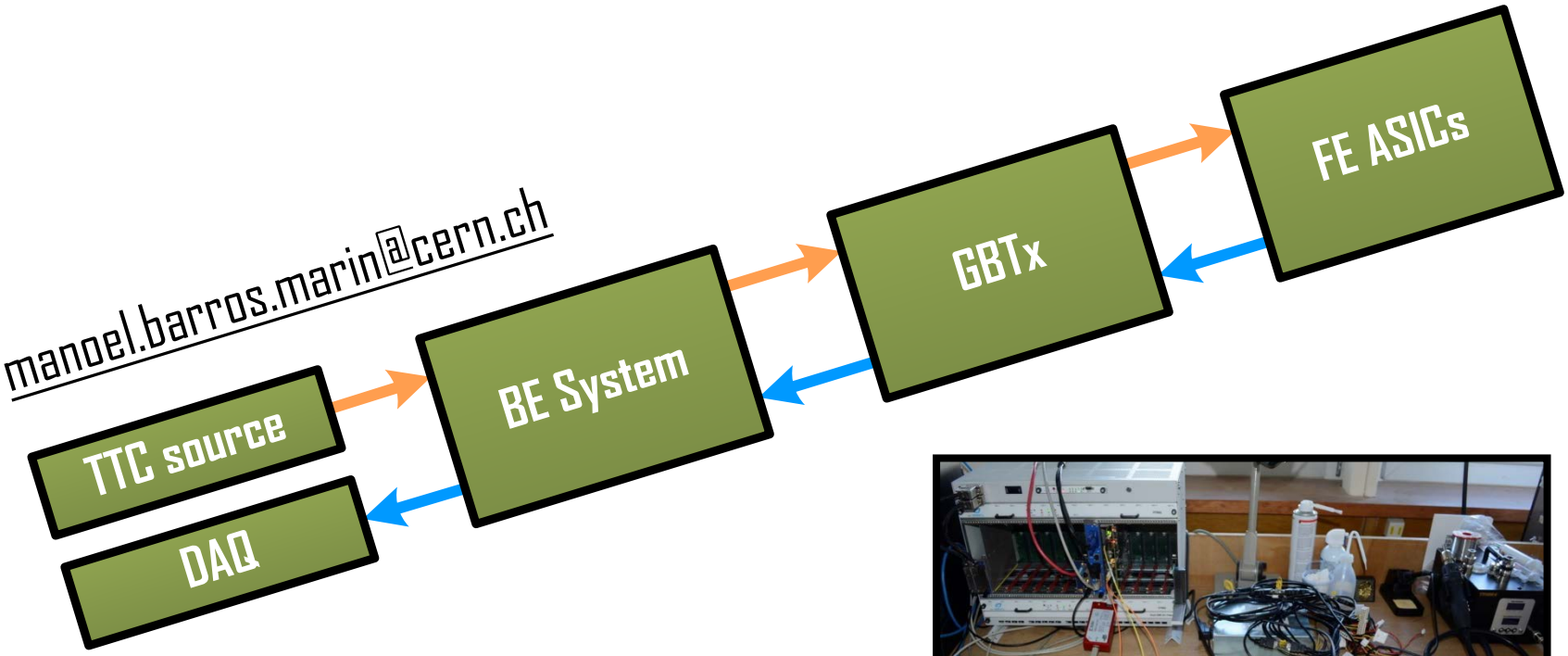
- Main site: https://espace.cern.ch/project-versatile-link/public/default.aspx
- Contact: Jan.K.Troska@cern.ch

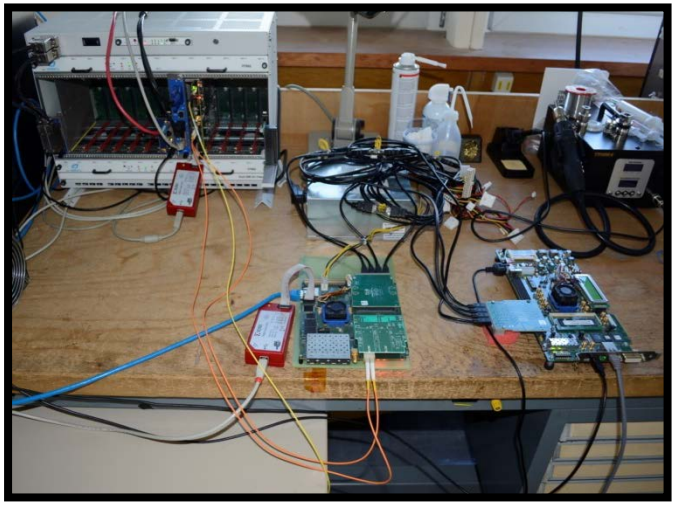
xTCA Evaluation project:

- Main site: https://twiki.cern.ch/twiki/bin/view/XTCA/WebHome
- Contact: Markus.Joos@cern.ch

Thank you

manoel.barros.marin@cern.ch

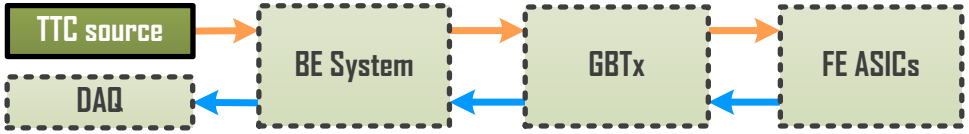




PH-ESE-BE

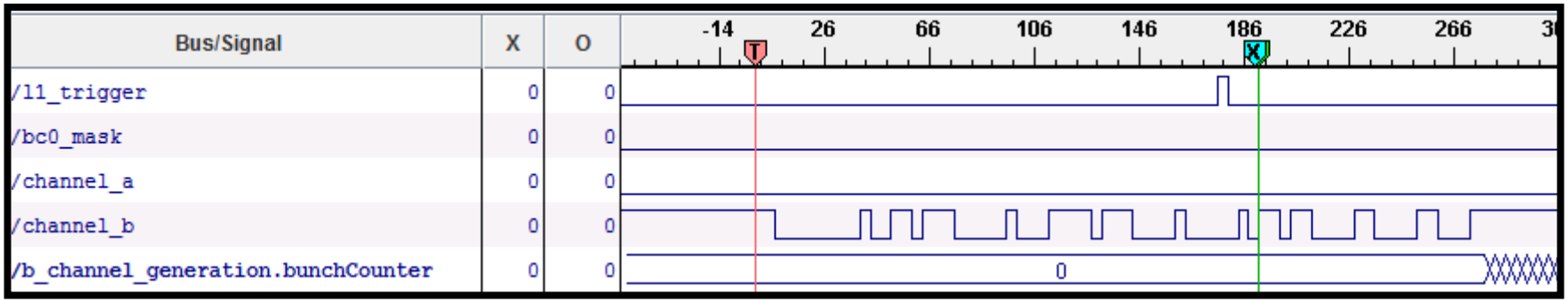
Demonstration system overview

TTC source (FPGA-based devkit)

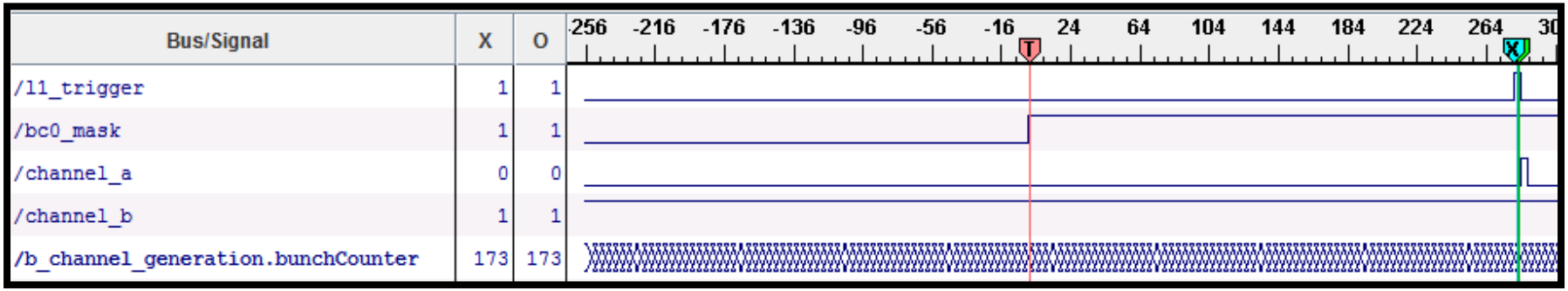


TTC (downstream)

Initialization

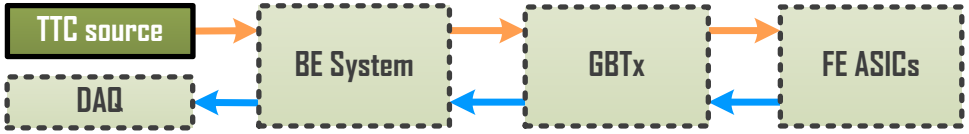


Level 1 Trigger



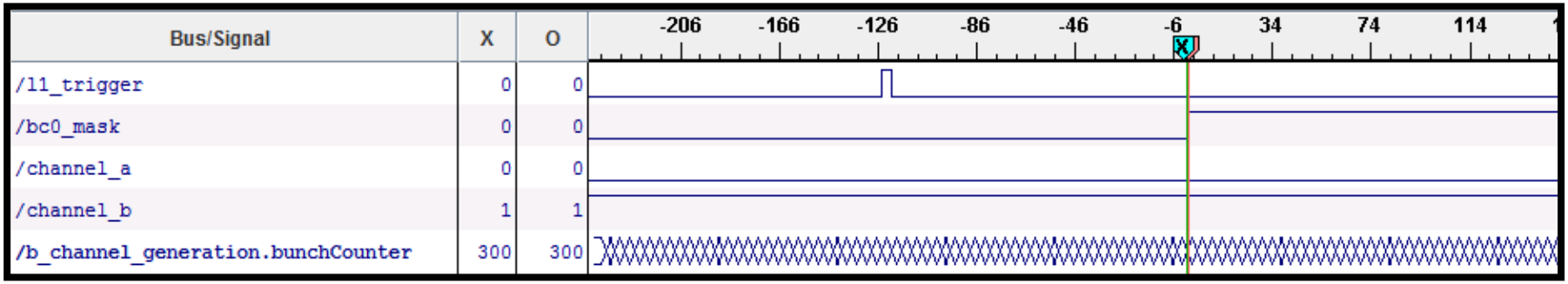
Demonstration system overview

TTC source (FPGA-based devkit)

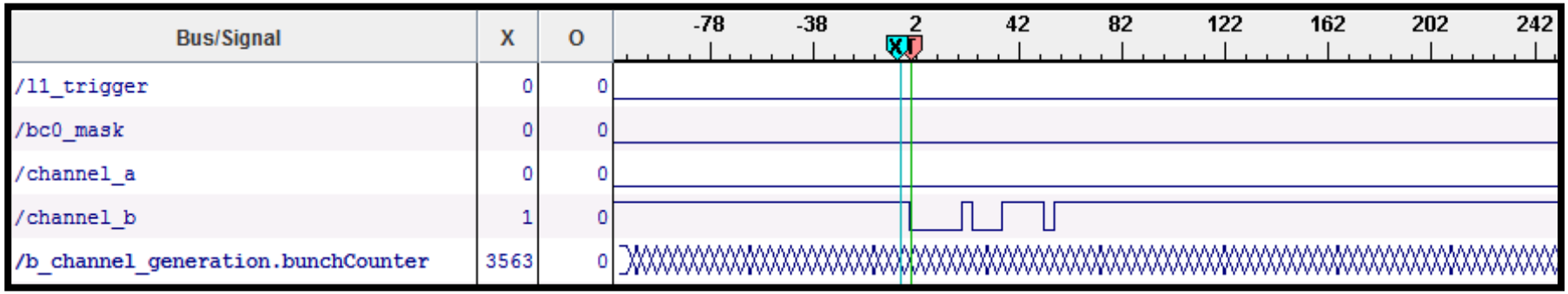


TTC (downstream)

Level 1 Trigger mask

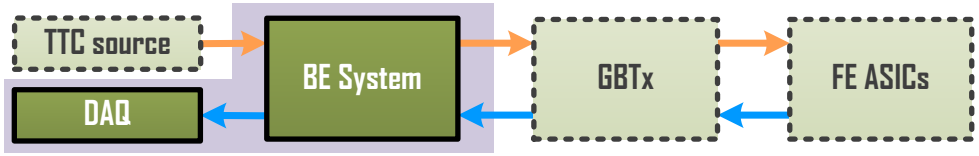


Bunch Counter Reset broadcast command



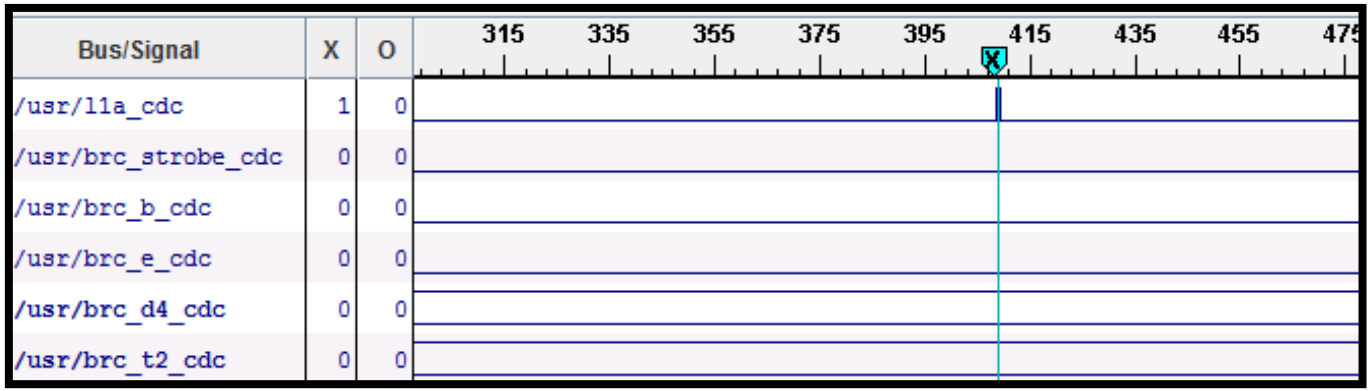
Demonstration system overview

Back-End System & DAQ (GLIB in uTCA shelf)

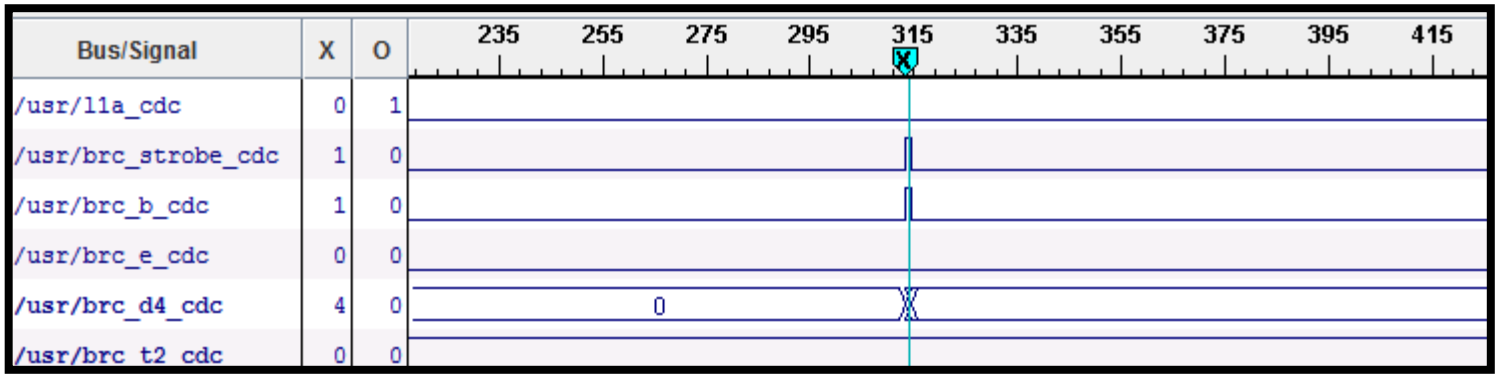


TTC (downstream)

Trigger

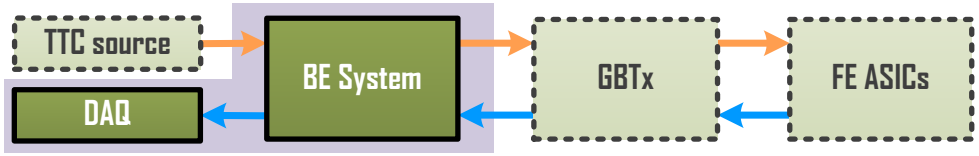


Broadcast command



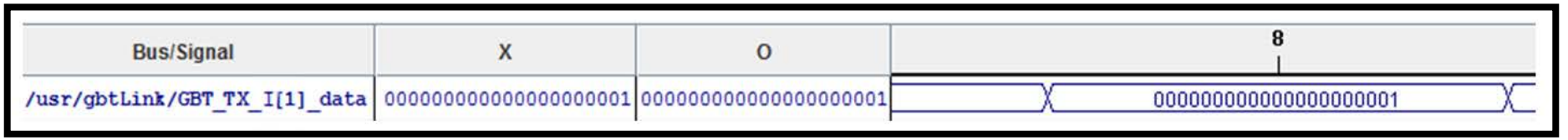
Demonstration system overview

Back-End System & DAQ (GLIB in uTCA shelf)

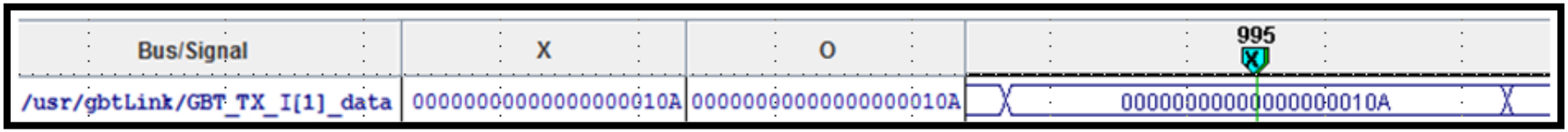


GBT Link TTC (downstream)

Trigger forwarding

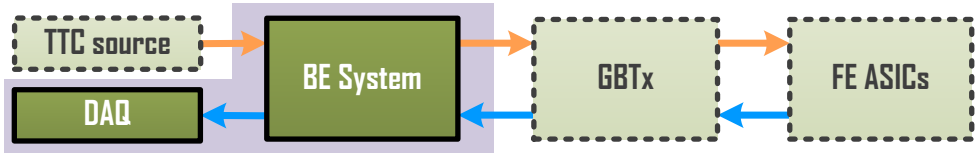


Broadcast command forwarding



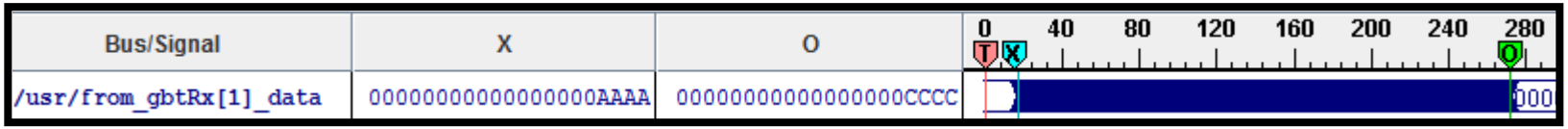
Demonstration system overview

Back-End System & DAQ (GLIB in uTCA shelf)

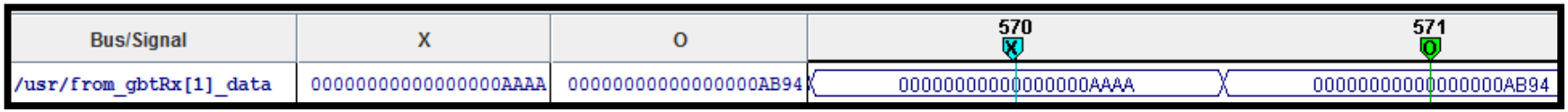


GBT Link & Readout logic DAQ (upstream)

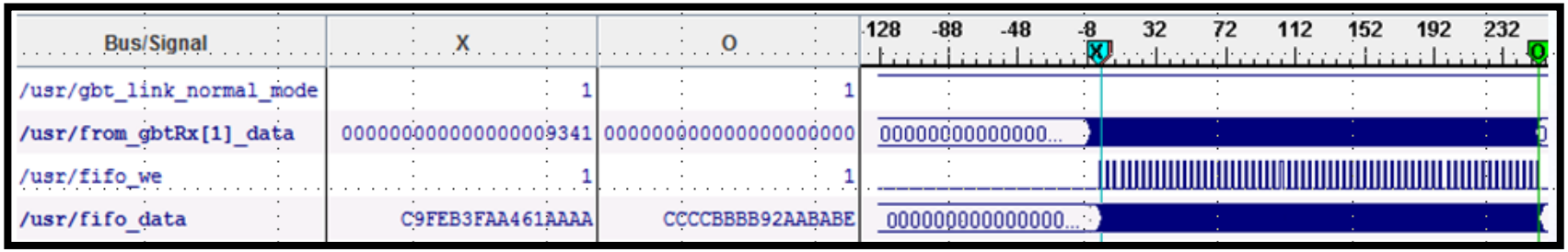
Incoming Readout Data Frame



Incoming Readout Data Frame detail

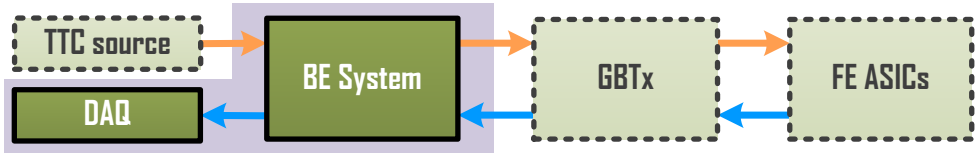


Incoming Readout Data Frame & Readout logic



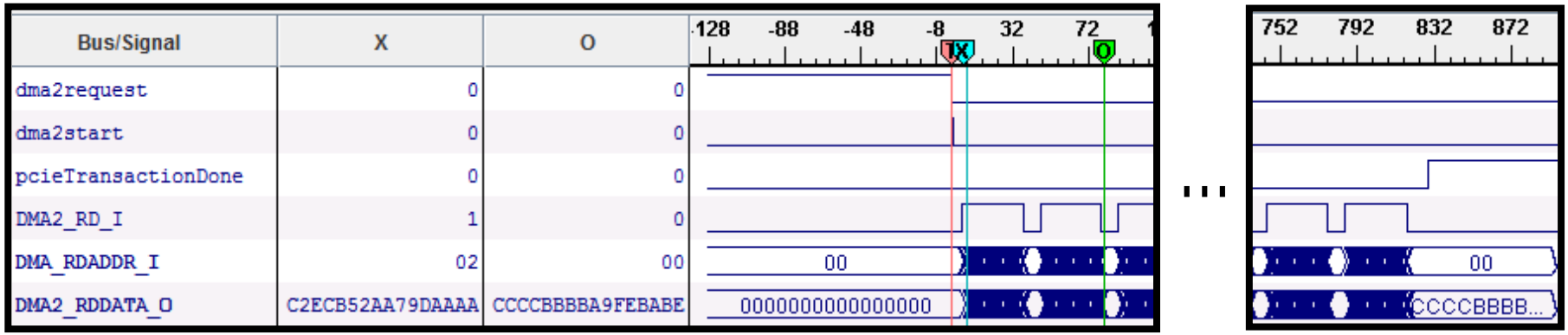
Demonstration system overview

Back-End System & DAQ (GLIB in uTCA shelf)



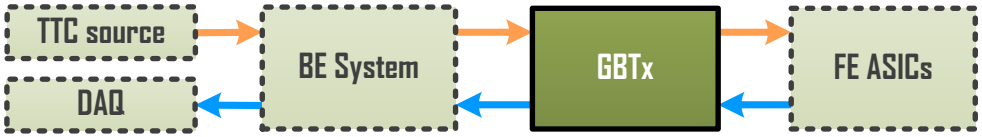
GBT Link & Readout logic DAQ (upstream)

DMA (PCIe) transaction



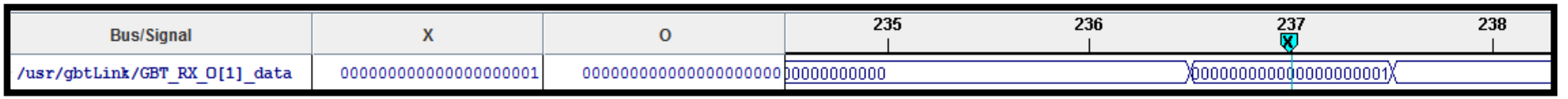
Demonstration system overview

GBTx (GLIB on bench)

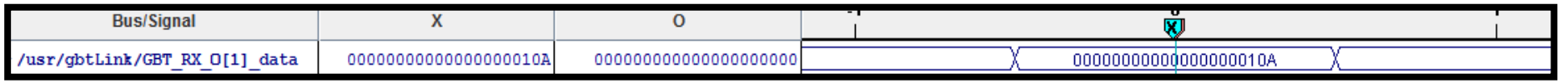


GBT Link TTC (downstream)

Trigger reception

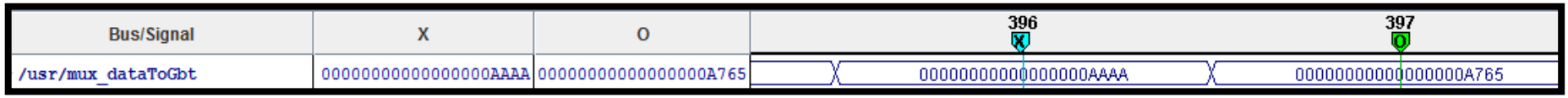


Broadcast command reception



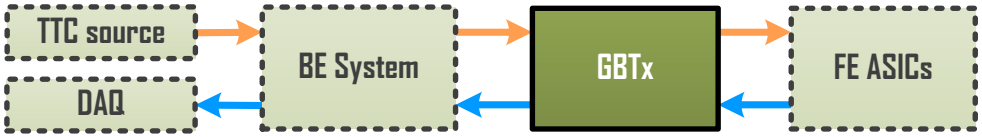
GBT Link DAQ (upstream)

Readout Data Frame forwarding



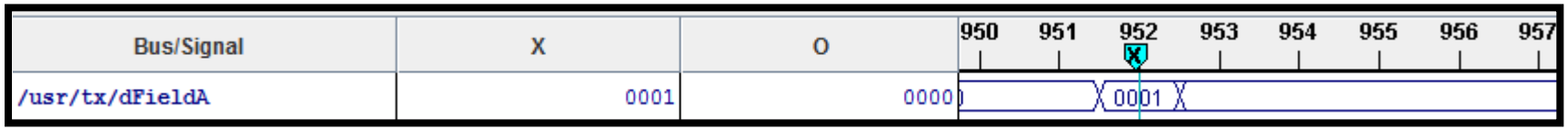
Demonstration system overview

GBTx (GLIB on bench)



E-links TTC (downstream)

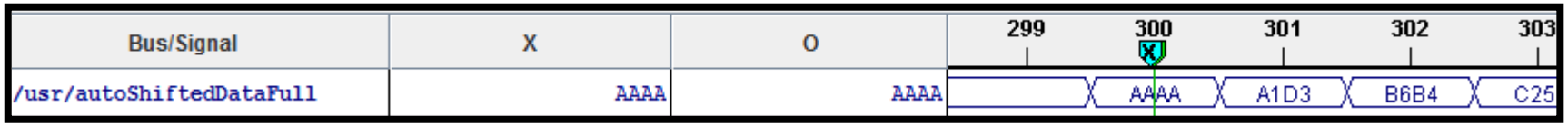
Trigger forwarding



Broadcast command forwarding

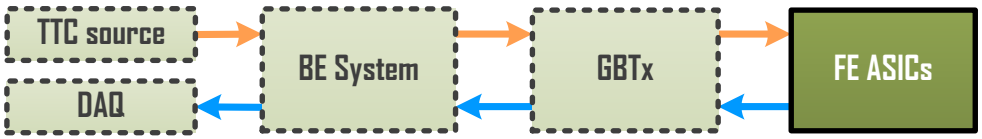
E-links DAQ (upstream)

Readout Data Frame reception



Demonstration system overview

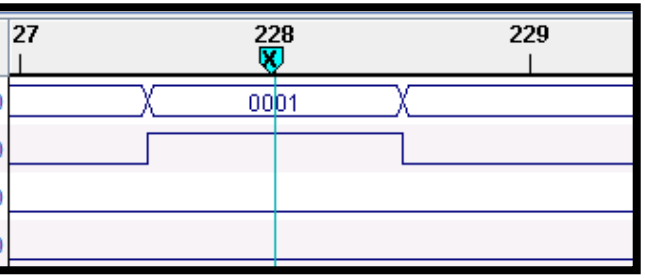
Front-End ASIC emulation (FPGA-based devkit)



E-links TTC (downstream)

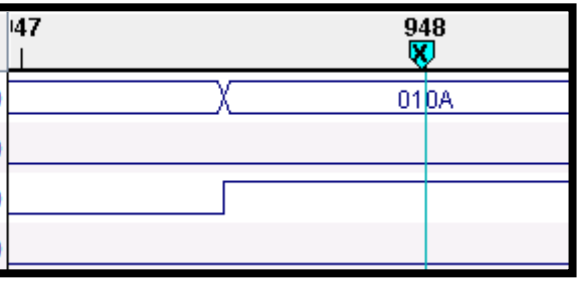
Trigger reception

Bus/Signal	X	O
/autoShiftedDataFull	0001	0000
/feAsicEmulator/L1A_I	1	0
/feAsicEmulator/BC0_I	0	0
/feAsicEmulator/EC0_I	0	0



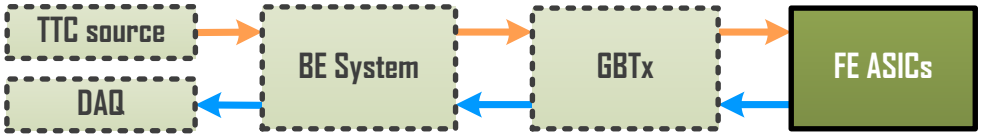
Broadcast command reception

Bus/Signal	X	O
/autoShiftedDataFull	010A	0000
/feAsicEmulator/L1A_I	0	0
/feAsicEmulator/BC0_I	1	0
/feAsicEmulator/EC0_I	0	0



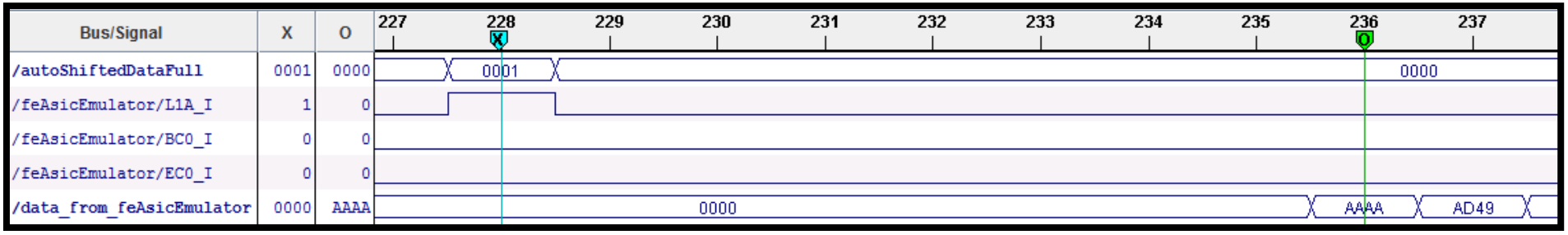
Demonstration system overview

Front-End ASIC emulation (FPGA-based devkit)



E-links DAQ (upstream)

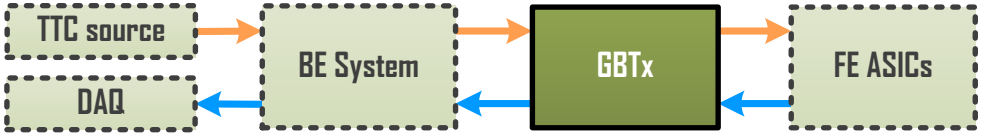
Readout Data Frame transmission

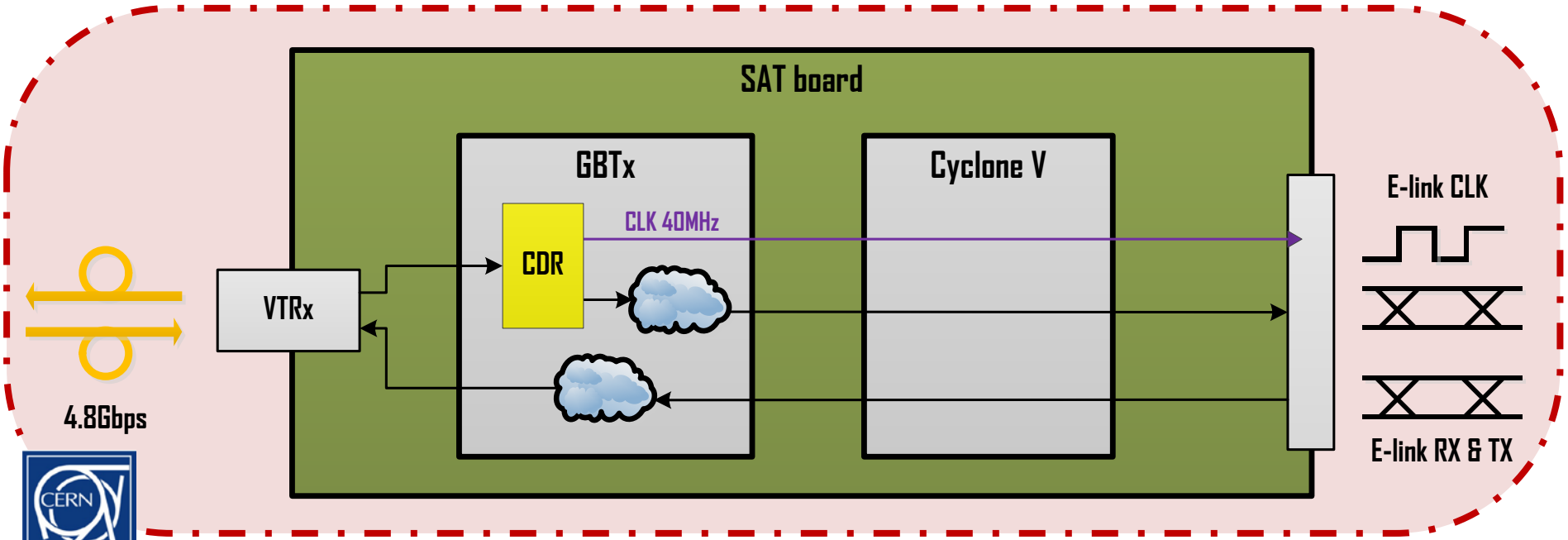


Demonstration system overview

GBTx

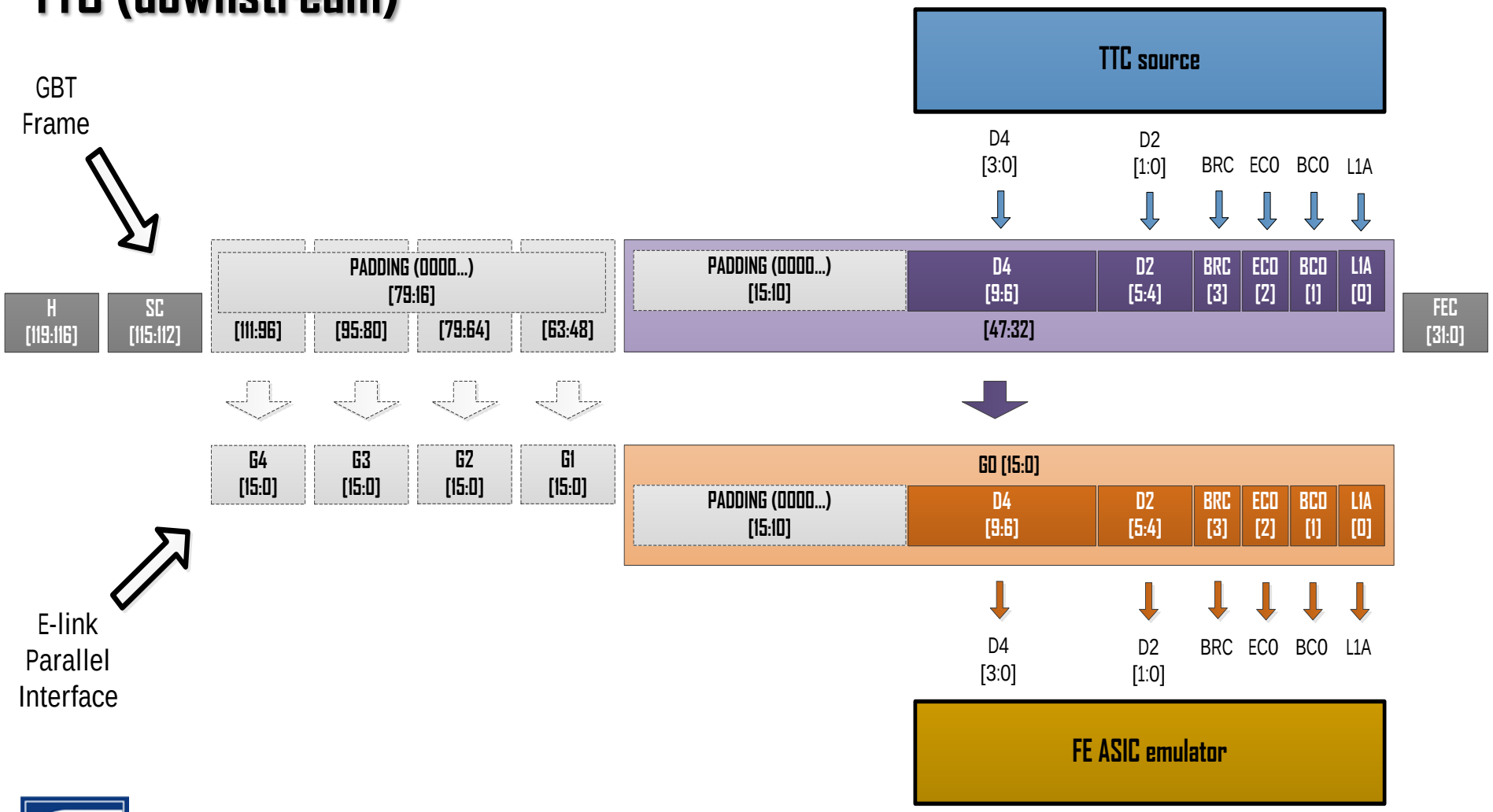
- Use of GBTx ASIC:

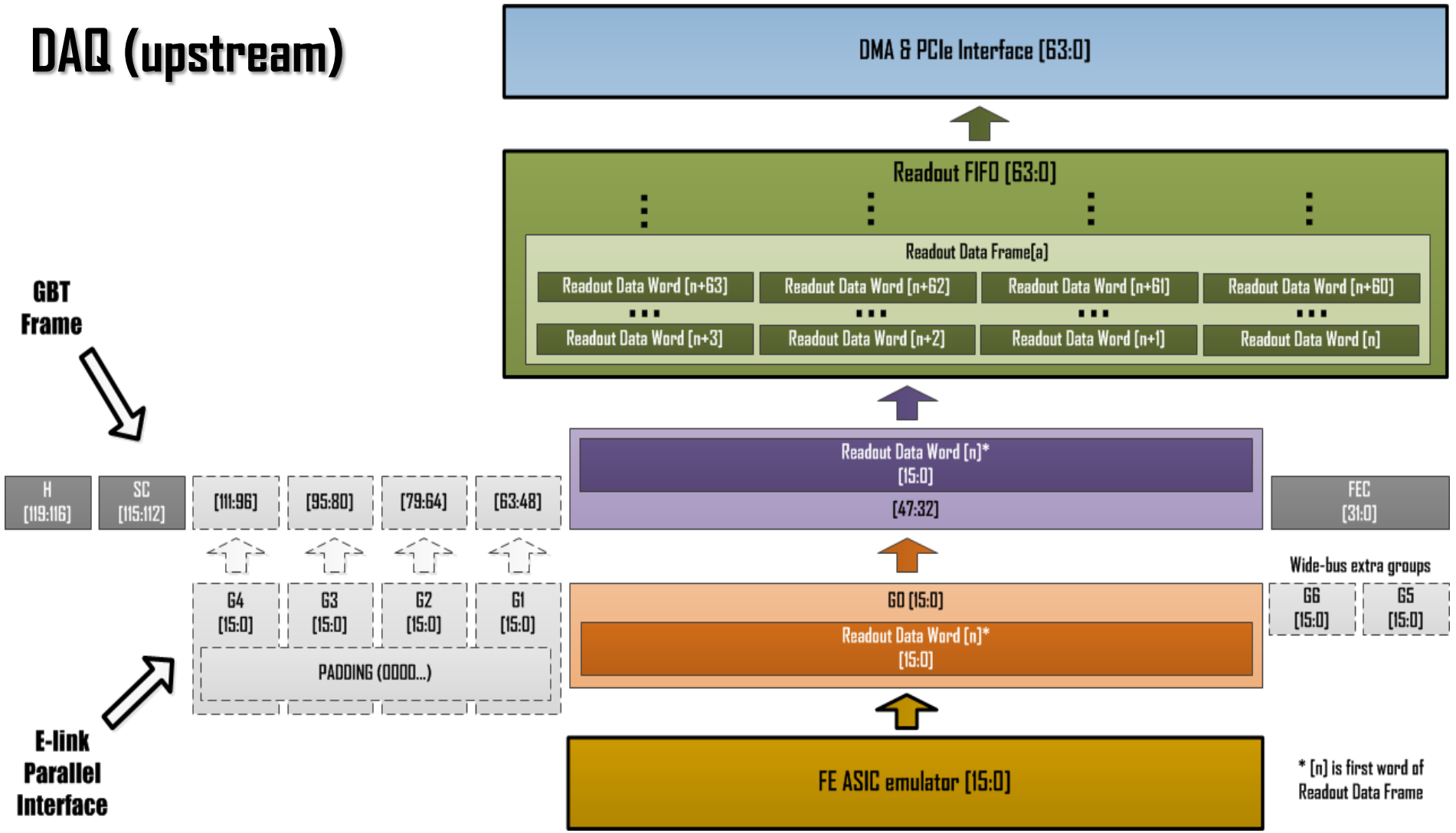




Data mapping

TTC (downstream)



Data mapping

DAQ (upstream)