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A GLIB-based uTCA demonstration system for HEP experiments

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The Gigabit Link Interface Board (GLIB) project is an FPGA-based platform for users of high-speed optical links in high energy physics (HEP) experiments. The project delivers hardware, firmware/software and documentation as well as provides user support. These resources facilitate the development of evaluation platforms of optical links in the laboratory as well as triggering and/or data acquisition systems in beam or irradiation tests of detector modules. This article focuses on the demonstration of a triggering and data acquisition setup for HEP experiments using hardware and firmware/software resources provided by the GLIB project.

Summary

The Gigabit Link Interface Board (GLIB) project is a development platform for users of high-speed optical links in high energy physics (HEP) experiments. The major hardware component is an FPGA-based double-width Advanced Mezzanine Card (AMC) conceived to operate either inside a µTCA shelf or on a bench with an optional link to a PC. In order to ensure the GLIB AMC compatibility with legacy and future interfaces as well as enhance its I/O bandwidth, some FPGA Mezzanine Cards (FMCs) have been developed. Besides hardware devices, the project delivers firmware/software, documentation and user support. These resources facilitate the development of evaluation platforms of optical links in the laboratory as well as triggering and/or data acquisition systems in beam or irradiation tests of detector modules.

This article focuses on the demonstration of a triggering and data acquisition setup for HEP experiments using hardware and firmware/software resources provided by the GLIB project. The setup comprises a back-end (BE) and a front-end (FE) part communicating through a Gigabit Transceiver (GBT)/Versatile Link (VL), the new bi-directional rad-hard link operating at 4.8 Gb/s. The BE consists of a uTCA shelf containing an AMC processor blade and a GLIB AMC equipped with a custom FMC for interfacing with a VME-based Trigger/Timing and Control (TTC) system. The FE part, due to the unavailability of GBT-based boards and compatible FE ASICs, consists of an emulated version of these devices. The role of the GBT chipset and the FE ASIC(s) is played by another GLIB AMC (operating on a bench) and a commercial FMC carrier, respectively. For the communication with the BE, the "GBT" GLIB AMC carries a VL FMC equipped with a VL transceiver (VTRx). For the emulation of the electrical link (e-link) communication between GBT and FE ASIC, both cards carry e-link FMCs.

Using that setup, we demonstrate the complete chain of a new-generation HEP system i.e. TTC reception at the level of the BE, forwarding of slow control, clock and trigger information to the FE through the downstream GBT/VL, emulation of e-link communication between GBT and FE ASIC at the level of FE as well as reception of FE data at the level of BE via the upstream GBT/VL and high-speed data readout by the AMC processor through the backplane of the shelf (Fat Pipes) using PCI Express x4 Gen2.

It is important to mention that a board featuring a GBT transceiver (GBTx) ASIC, an FPGA as well as SFP+/VTRx sockets, namely the GBT Stand Alone Tester (GBT-SAT) board, is currently under development. In case the GBT-SAT will be available and the GBTx well characterized, the board could play the role of the FE system instead of the GLIB, making the demonstration even more realistic. In that case, the on-board FPGA will emulate FE ASIC module operation.

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