Development of Dedicated Front–end Electronics for Straw Tube Tracker in PANDA Experiment

Dominik Przyborowski[1],
M. Idzik[1], T. Fiutowski[1], P. Salabura[2],
P. Strzempek[2], J. Tokarz[1]

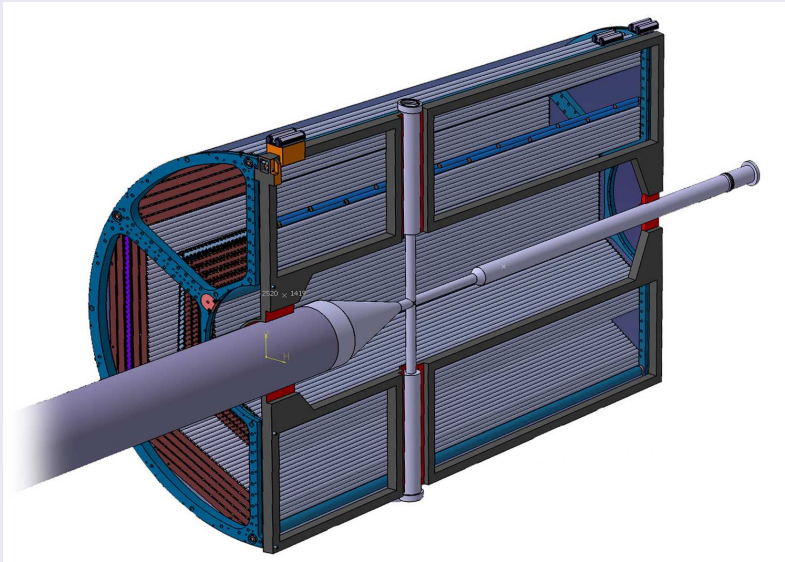
[1] AGH University of Science and Technology
[2] Jagiellonian University

Topical Workshop on Electronics for Particle Physics
23 - 27 September 2013, Perugia, Italy

Outline

PANDA STT

PANDA STT cross section

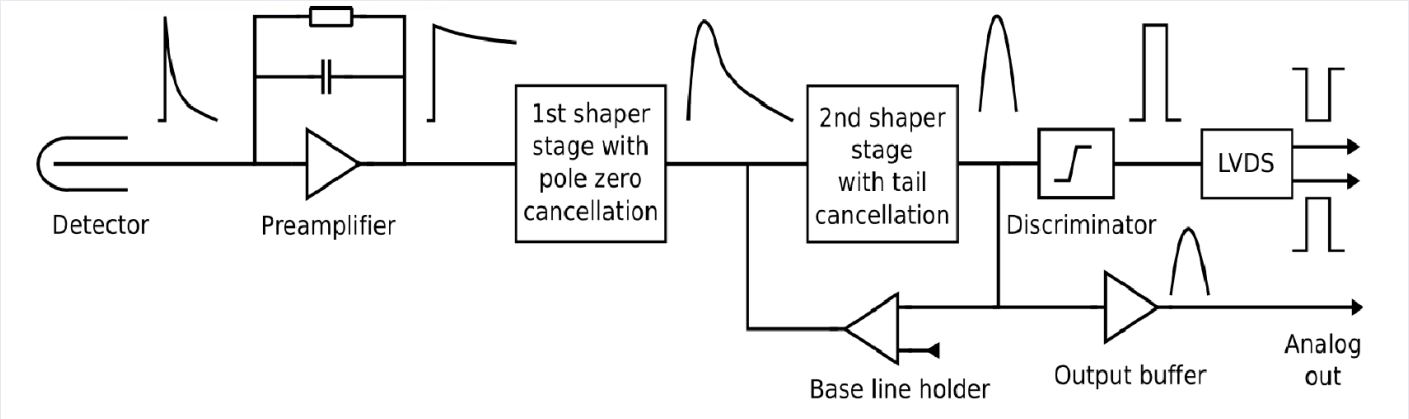


Parameters

- Dimensions: 1.5 m length and 10 mm diameter
- Detector capacitance $\sim$ 25 pF
- Ar/CO_2 (10%) gas mixture
- Expected count rate: $\sim$ 800kHz/tube
- $\sim$ 5000 channels

Outline

Specification



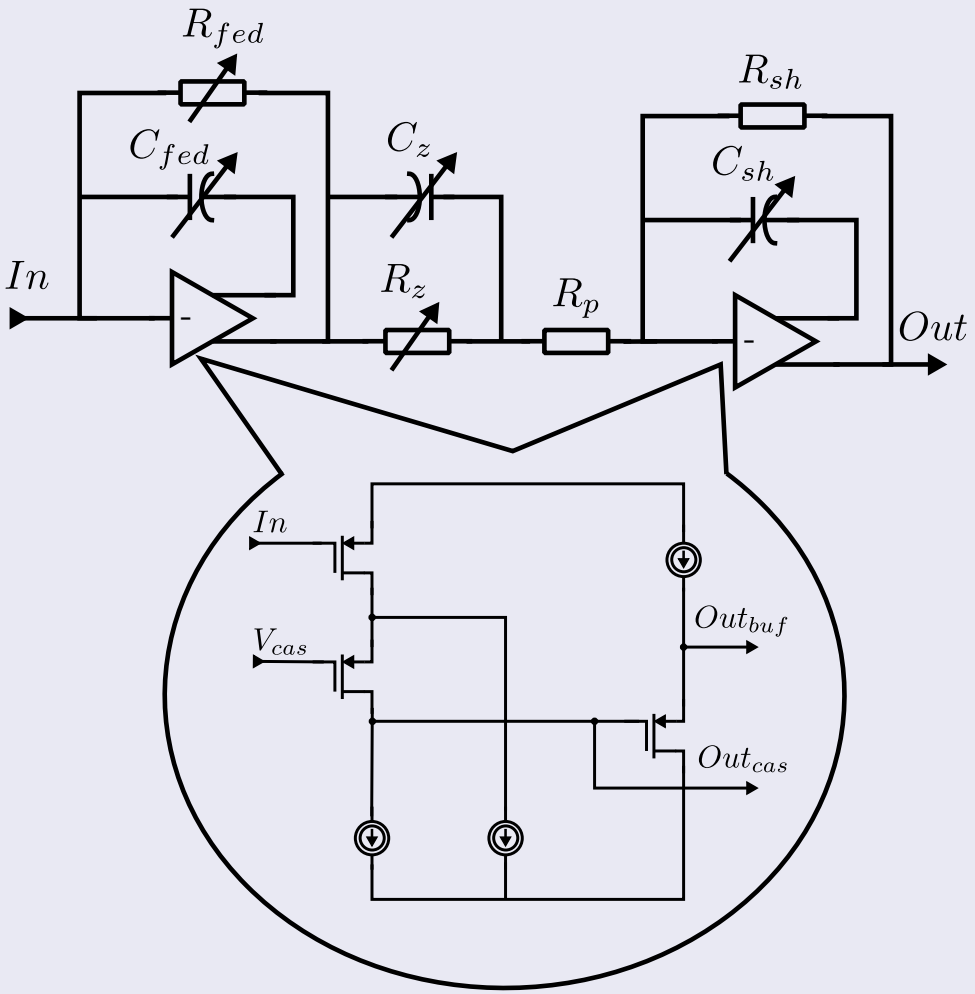
Features

- CSP with variable gain and time constant
- CR–RC^2 shaper with variable peaking time
- Ion tail cancellation circuit with trimming
- Baseline stabilized by BLH circuit
- Leading edge discriminator for time and ToT measurements
- Fast LVDS output
- Buffered analog output

Outline

Architecture
Preamplifier and Shaper

Schematic diagram



Features

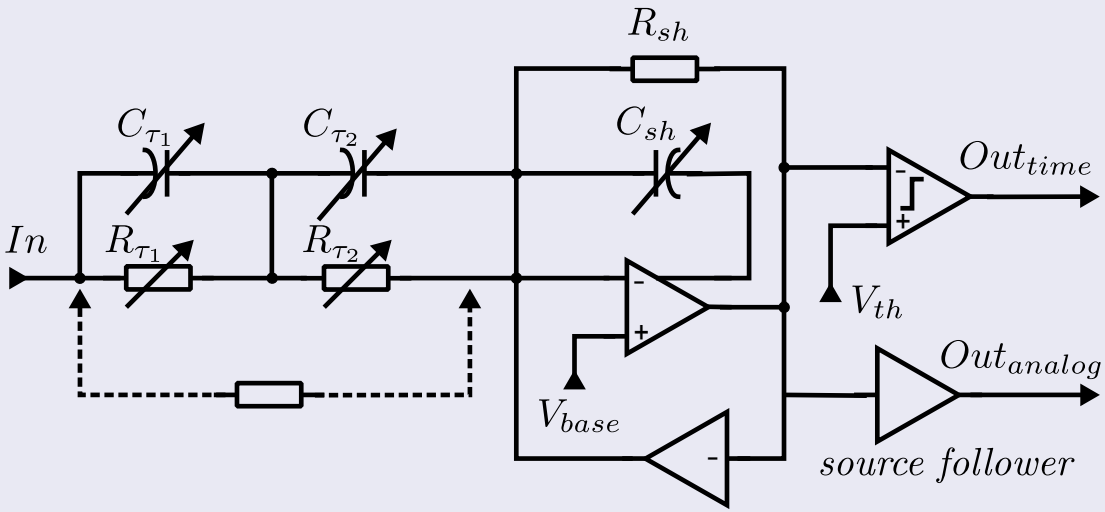
- Variable charge gain: 0.5 – 4 mV/fC
- Variable preamp time constant: 25 – 800 ns
- PZC matched to various preamp settings
- 1^{st} shaper stage with $\mathrm{T_P}$ in range 10 – 40 ns

Input transistor

- Drain current = 2 mA
- W/L = $2000\mu/0.35\mu$
- Transconductance $\approx$ 26 mS

Architecture
Tail Cancellation and Output stages

Schematic diagram

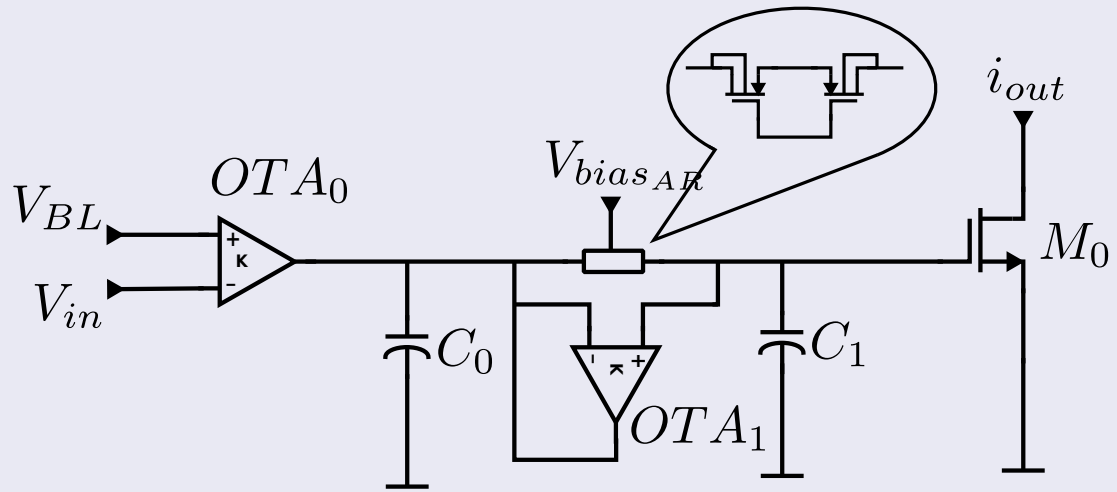


Tail cancellation

- 4 modes of work:
  CR–RC^2, only τ_1, only τ_2, both
- Trimming time constants:
  $tau_1 \in 3 - 43$ ns (6 bits)
  $tau_2 \in 18 - 511$ ns (6 bits)

Architecture
Baseline Holder

Schematic diagram

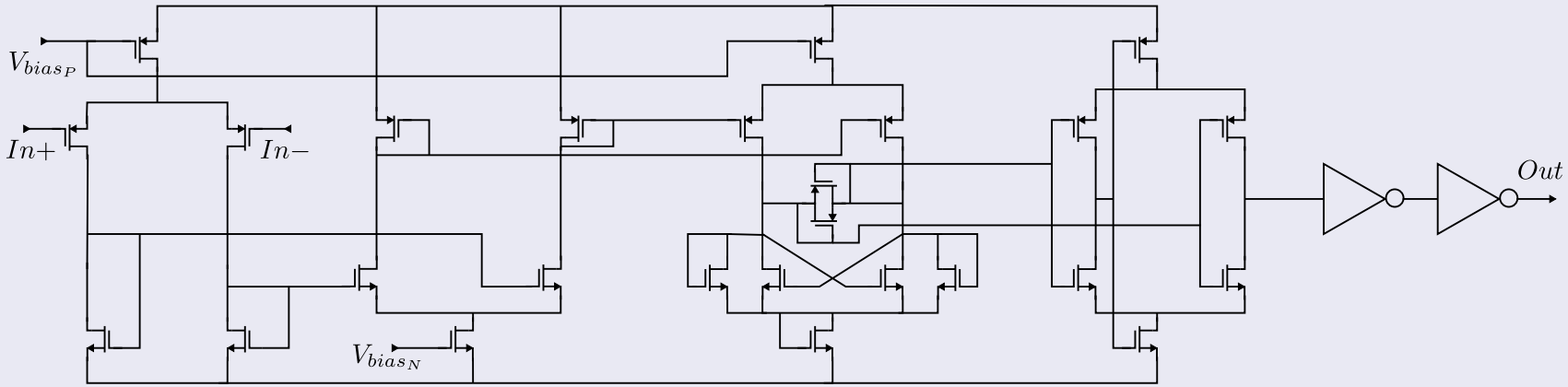


Components

- Nonlinear buffer (slew rate limited - OTA_0 and C_0)
- High value tunable active resistor for low pass filter
  (A. Tajalli, Y. Leblebici, E.J. Brauer, *Implementing Ultra-High-Value Floating Tunable CMOS Resistors*, Electronics Letters, 2008, pp. 349-350)
- Current sink controlling current in last stage feedback

Architecture
Leading Edge Discriminator

Schematic diagram



Stages

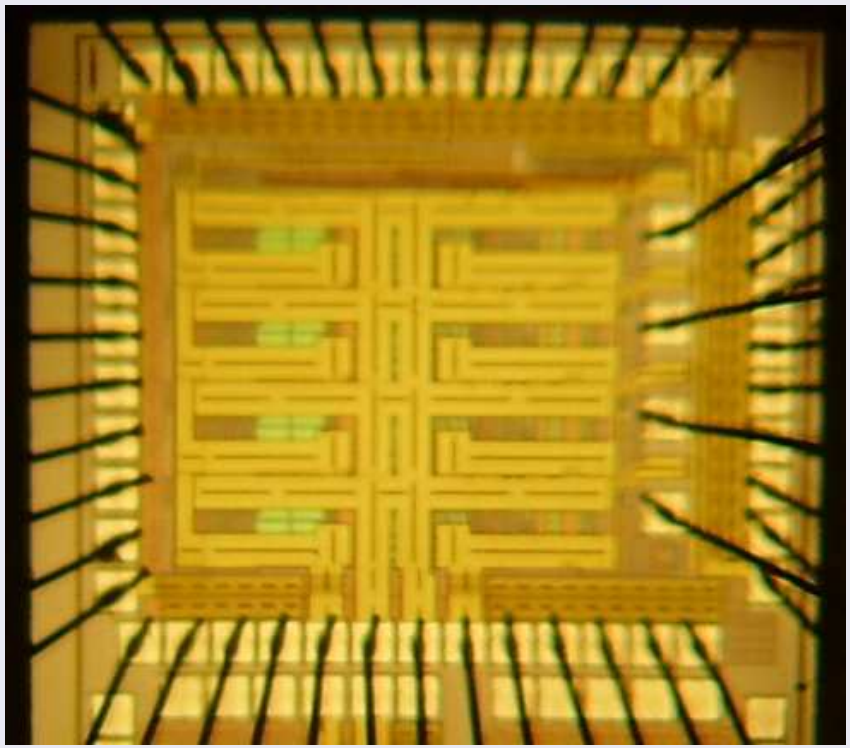
- Two low–gain preamplifing stages
- Latch stage with histeresis
- Self–biased amplifier
- Inverters

Measurement results

First prototype basic data

- AMS 0.35μm 2P–4M CMOS Process
- Four channels
- Channel size: 200×1130 μm^2
- Power consumption: $\sim$ 15.5 mW/ch + LVDS $\sim$ 12 mW $\approx$ 28 mW/ch
- Peripherals not yet designed, biasing and thresholds setting externally

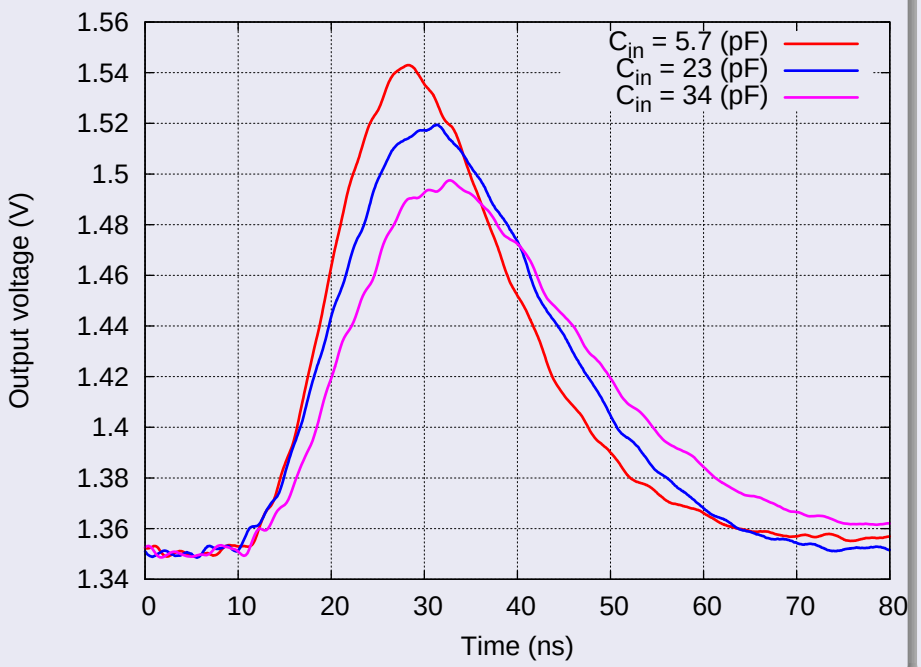
Chip size: 1.5 × 1.2 mm^2



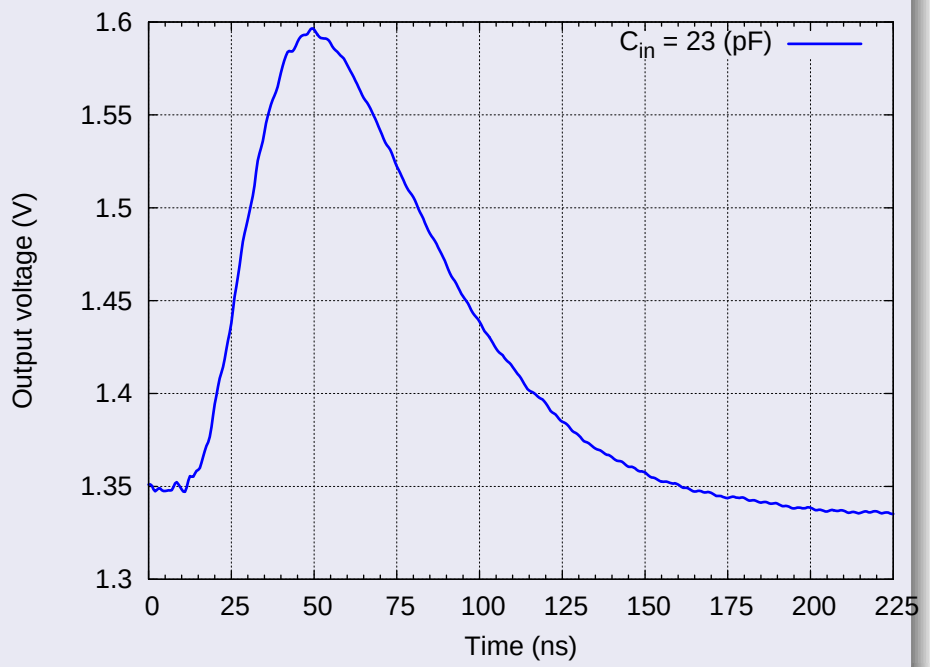
Outline

Measurement results
Pulse shapes

Response for 10ns T_P settings



Response for 40ns T_P settings

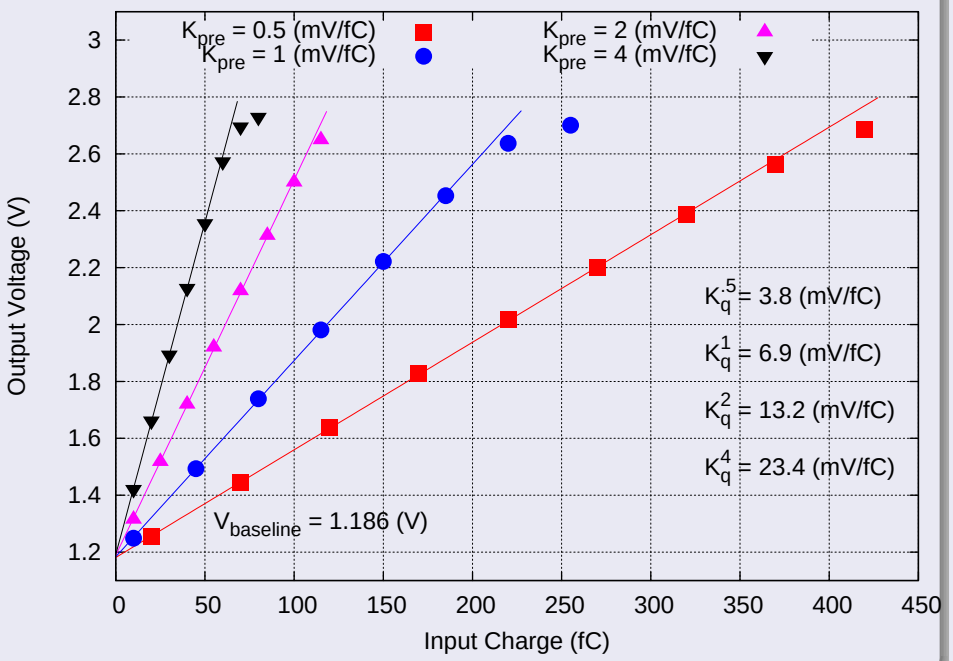


Response slower due to layout parasitics and output buffer performance

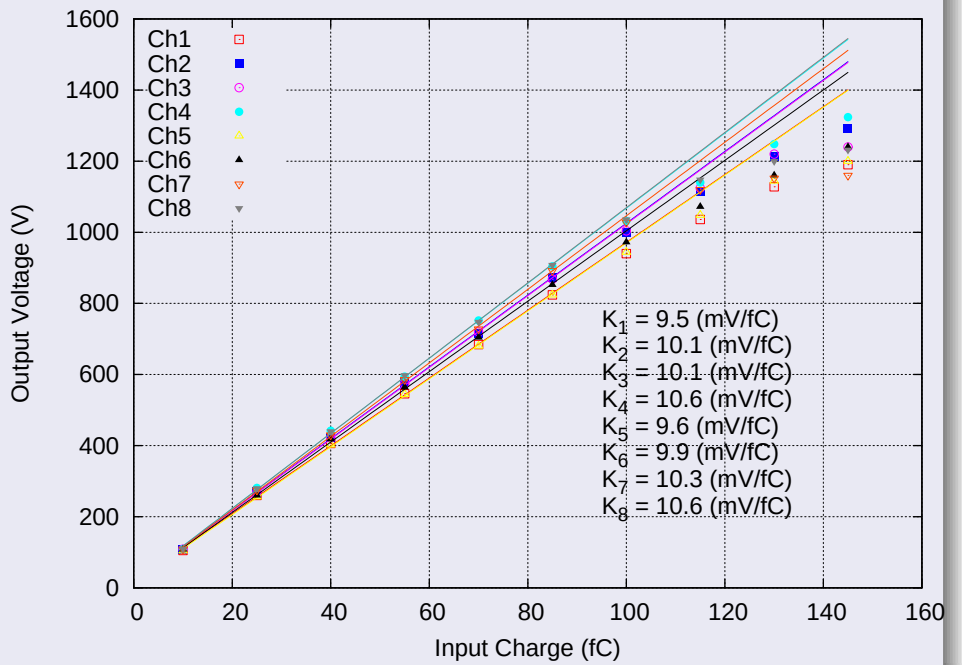
Outline

Measurement results
Linearity and Gain

Channel modes



Channel uniformity



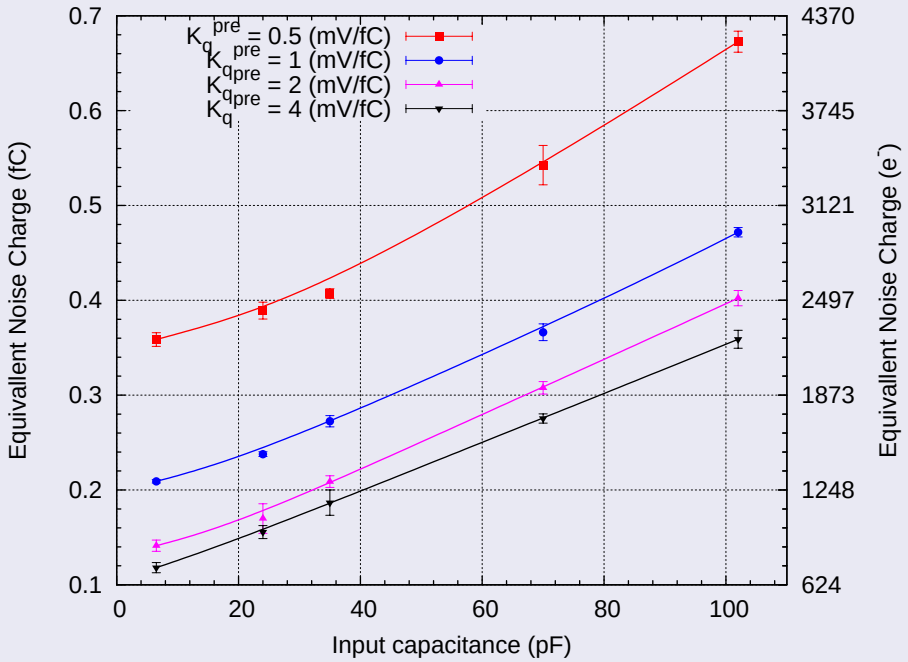
S–curves measurements

Analog buffer output

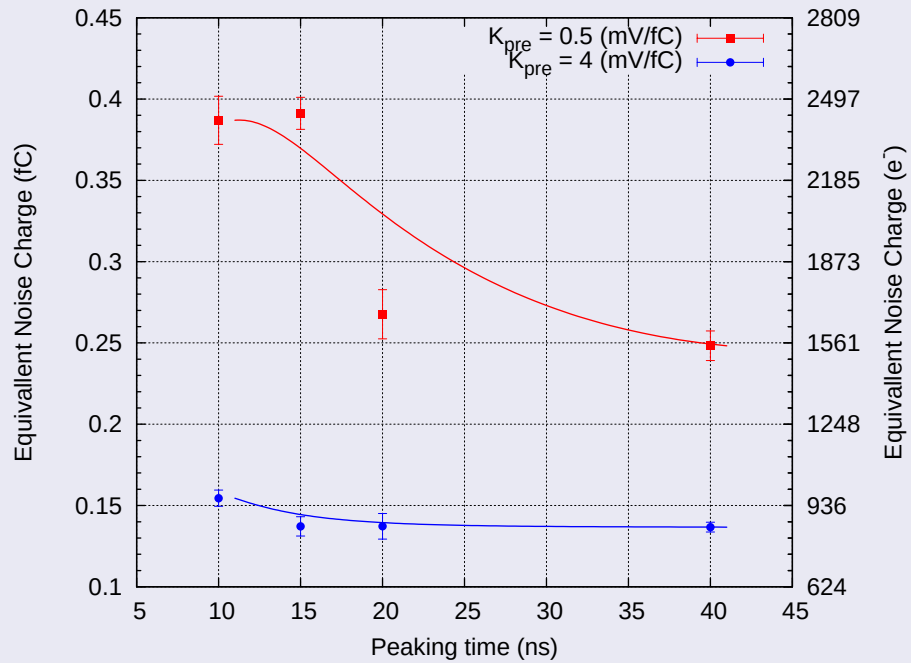
Outline

Measurement results
Noise

ENC vs input capacitance



ENC vs peaking time

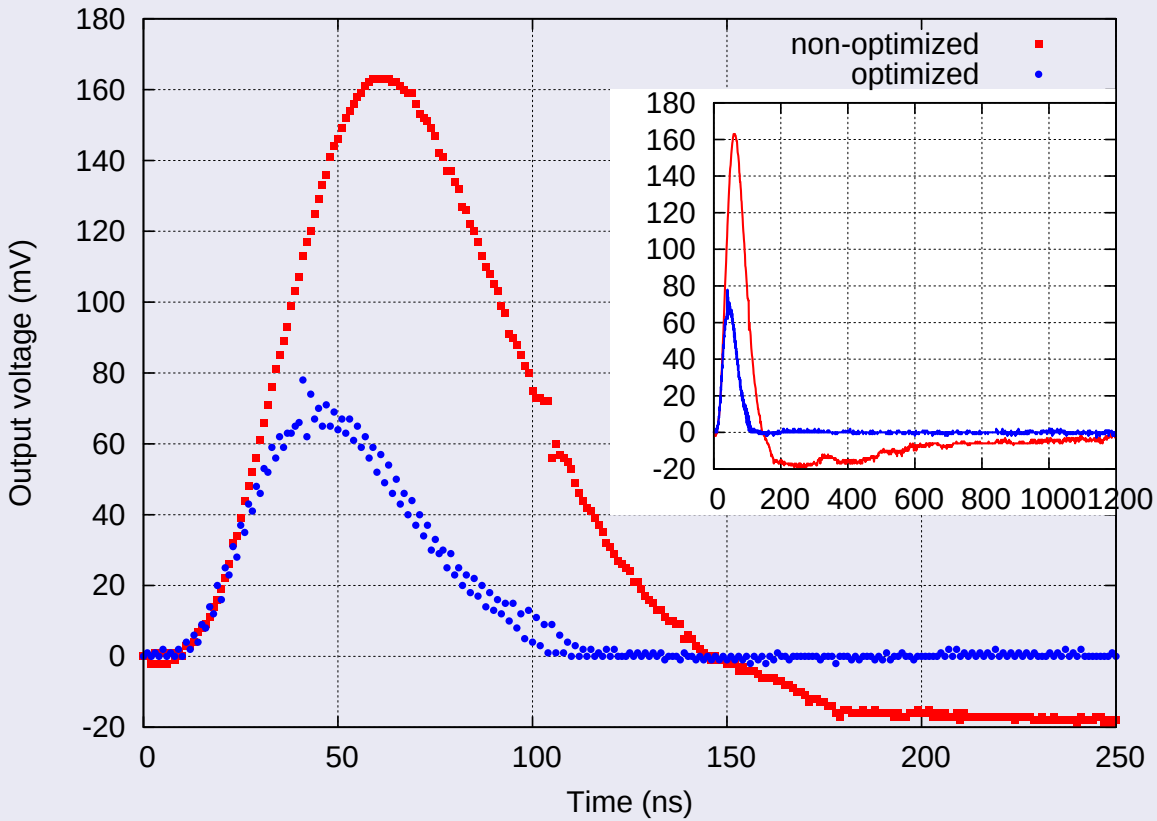


ENC $\approx$ 1000 e$^-$ for default FE settings
($K_{pre} = 2mV/fC$, $T_P = 10ns$ and $C_{in} = 25pF$)

Outline

Measurement results
Tail cancellation

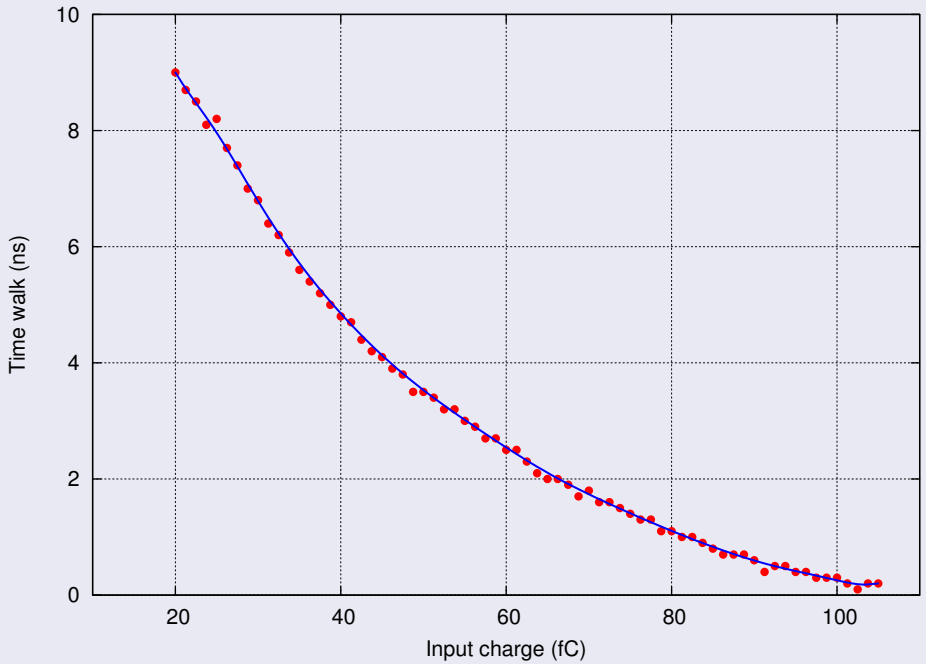
Responses for Fe^{55} X–rays



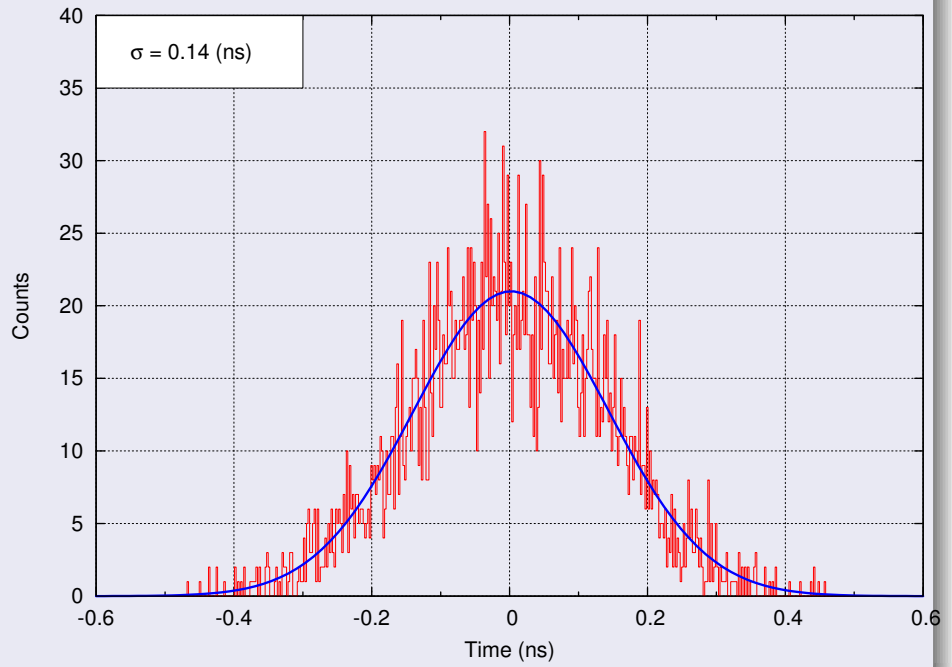
Outline

Measurement results
Time resolution

Time walk



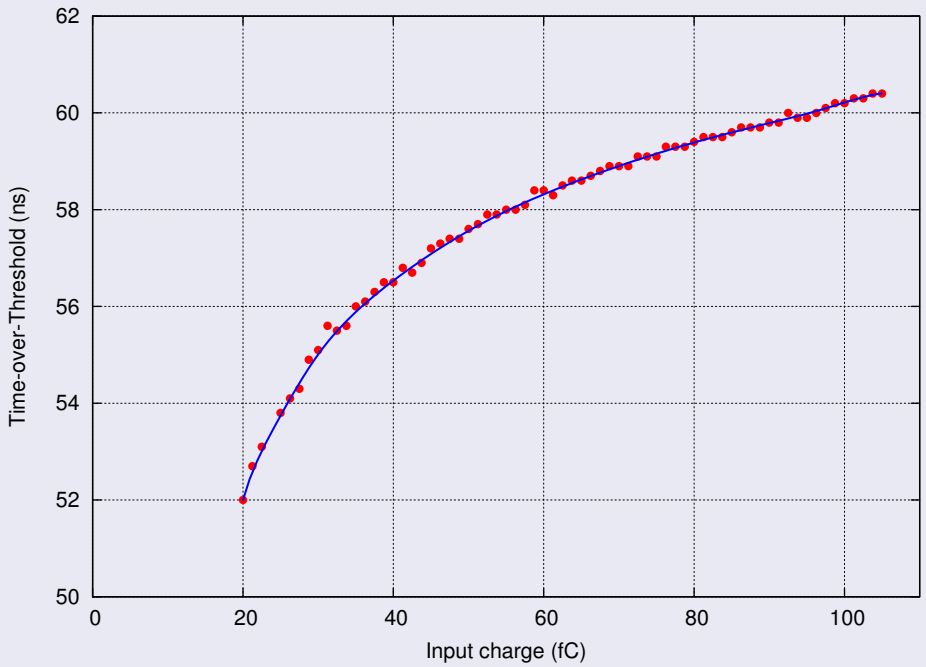
Jitter

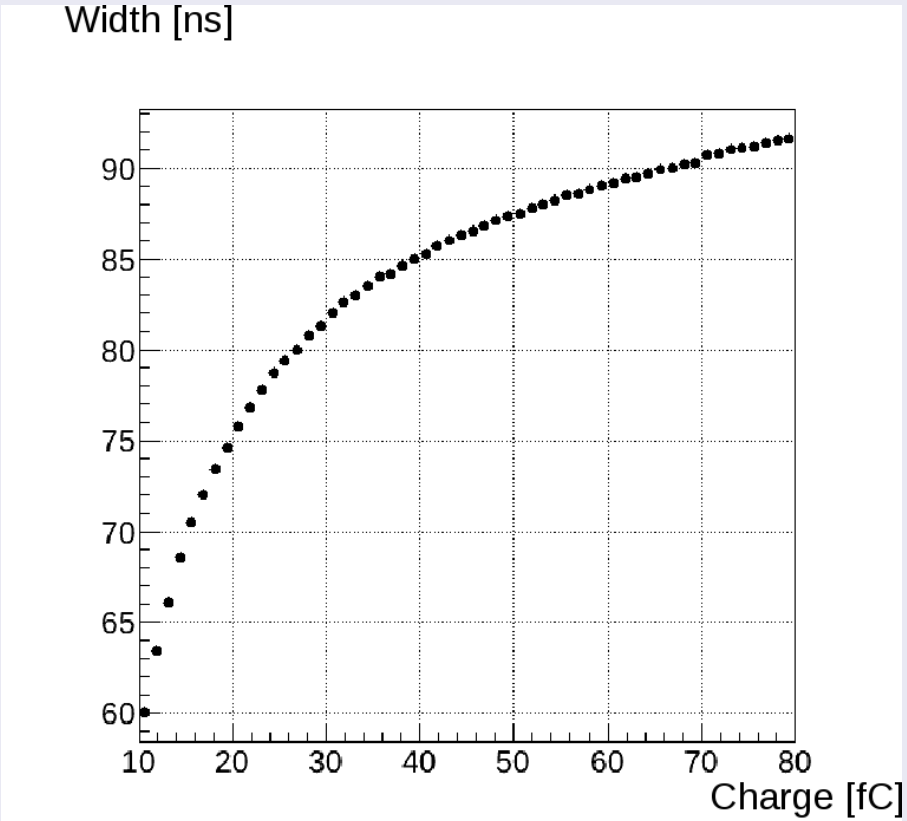


1–2 ns time precision could be obtained by compensating time walk basing on amplitude information

Outline

Measurement results
Time–over–Threshold





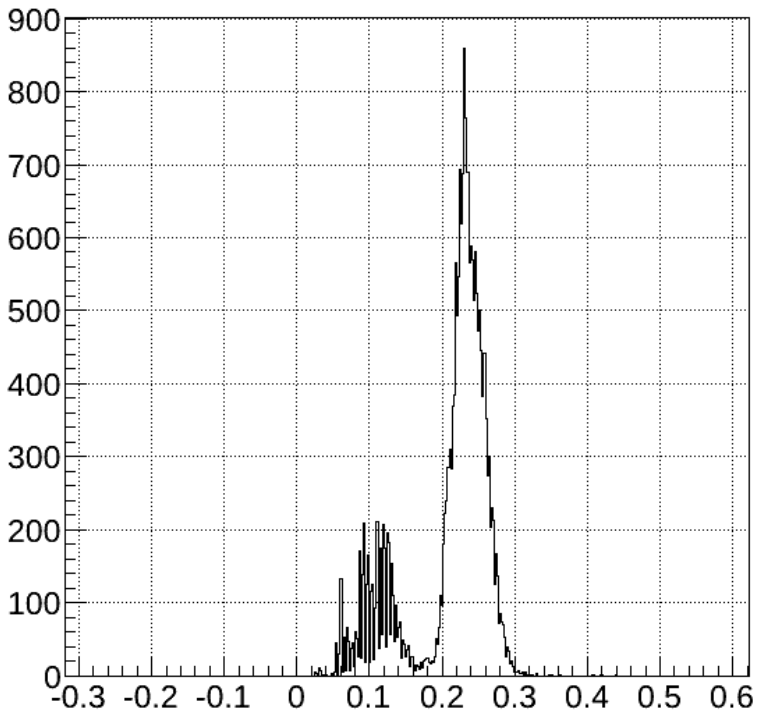
Results achieved for delta pulse and different FEE settings

Outline

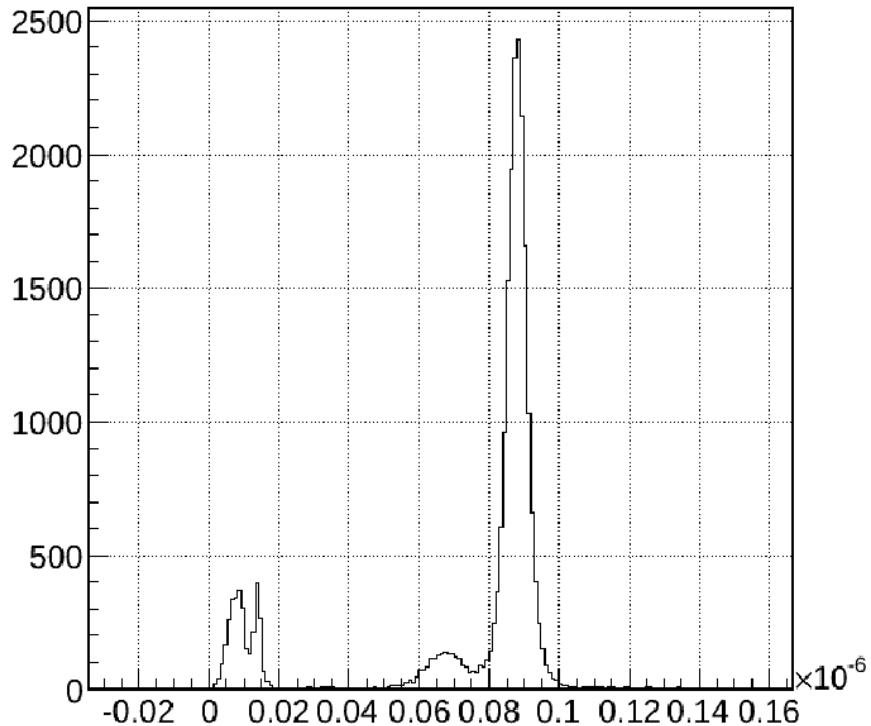
Measurement results

Fe^{55} X–rays spectrums

Amplitude spectrum



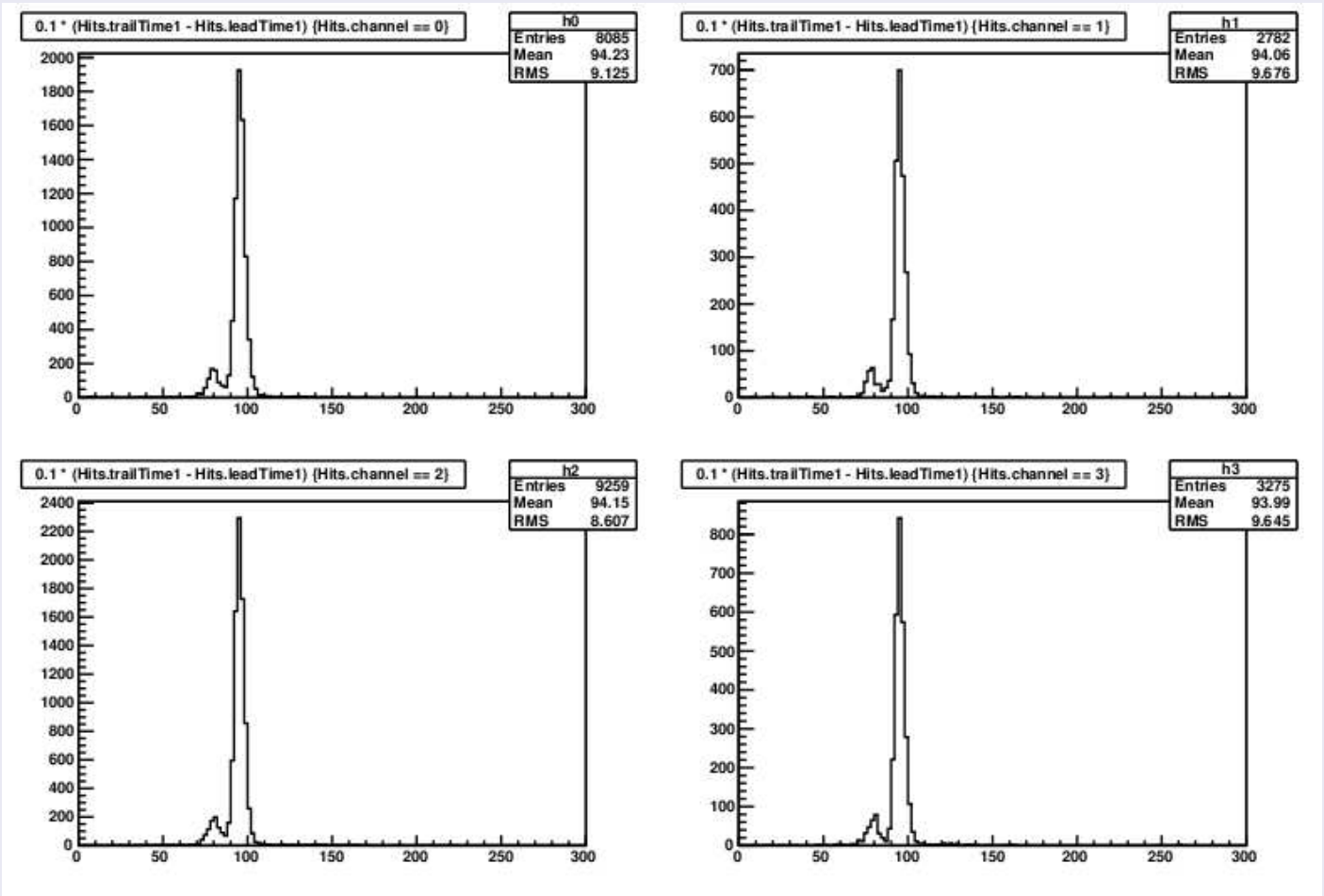
ToT spectrum



Measurement results

Fe^{55} X–rays spectrums

Fe^{55} ToT spectrums for four channels

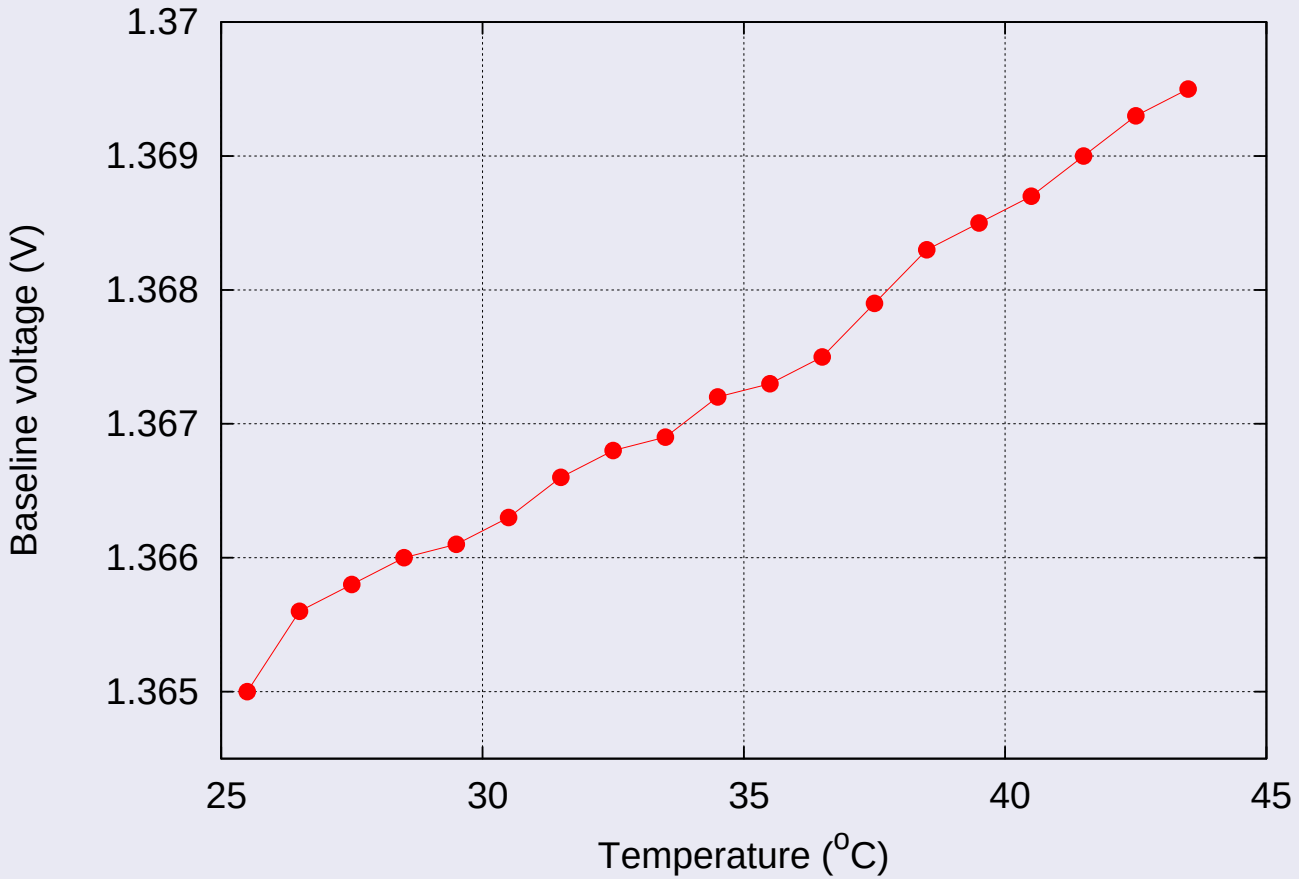


Outline

Measurement results

Baseline

Baseline level vs temperature



Measure after output buffer – V_{gs} and β variations

Summary and plans

Summary

- 1^{st} prototype of STT front–end fully functional
- Variable gain 3 – 24 mV/fC and peaking time $\sim$ 20 – 40 ns work well
- ENC $\approx$ 1000 e^- for default conditions ($K_{pre} = 2mV/fC$, $T_P = 10ns$ and $C_{in} = 25pF$)
- Tail cancellation works and could be trimmed to various types of input signals
- Readout module with 8 ASICs (32 channels) succesfully used in test-beam

Future plans

- Adding DACs for threshold and baseline settings
- New 8 channel prototype in progress – submission planned at the end of this year

Improvments

- Preamplifier and shapers redesign to obtain higher speed (meet 10ns of T_P specification)
- BLH modification to minimize baseline dispersion
- Improvements of output buffer