New CMS DAQ link development

Standard DAQ link for new hardware (not VME based)

SlinkXpress

xTCA Interest Group Meeting – TWEPP, 2013
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New CMS DAQ link for uTCA

- For new uTCA based systems (first ones to be installed are from HCAL), a new scheme of interfacing is designed instead of Slink64.

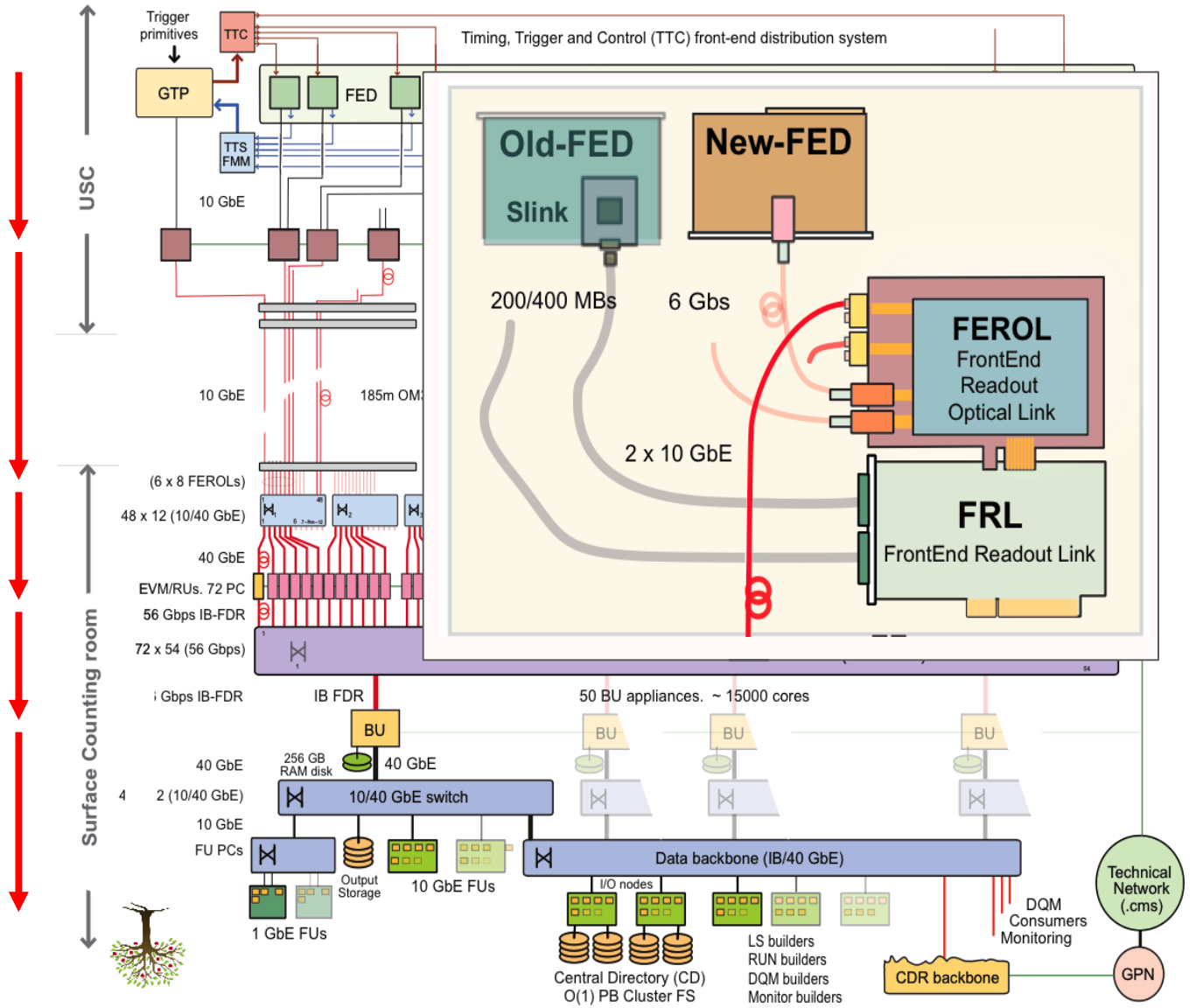
- The sender is no more a mezzanine driving copper cables but is an FPGA IP core directly integrated into AMC13 FPGA driving an 8b/10b fibre @ 5 Gb/s. The speed can be increased if needed.

- Link features a retransmit capability based on CRC checks/missing frame
  - Both sender and receiver designed originally on MOLs (ALTERA based prototypes)
  - Both blocks ported to Xilinx Virtex 6 using an ML-605 (Xilinx commercial evaluation board)
  - IPs successfully used by Boston group on 2 AMC13 linked together through the link

- From the user point of view, the link has the same interface than Slink64 and uses the same CMS common data format ☺

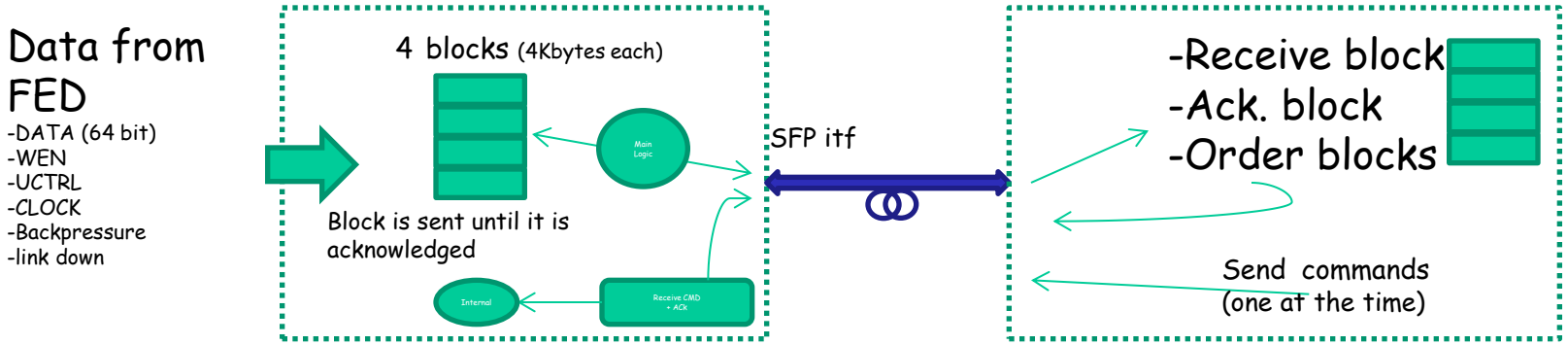
- Sender also features an internal data generator fully controlled from the receiving side

Where SlinkXpress is used ?



Link mechanism in brief (1)

- The sender and receiver have 4 blocks of 4 kBytes each.
- When a block is full or when it contains a complete event, the content is sent over the link.
- Data organised in frames : SOF, EOF, different frame types
  - Init, Data, ACK, Command
- The receiver checks the CRC and if correct, sends an ACK frame to sender. The block is freed and can receive new data.
- If CRC not correct or event not seen/received, no ACK frame sent.
- Sender re-send again the block after configurable timeout.
- If the 4 blocks are busy, back-pressure on the FED side is raised.
- On the receiver side, data are extracted in sequence for the consumer



Link mechanism in brief (2)

- When retransmits occur, part of the bandwidth is used for retransmit and not for new data

- If the data link is used close to its max bandwidth and retransmit occurs, the link may never recover the full bandwidth after retransmits disappear (similar phenomena in 10GbE section shown by Petr later).
- This is because the "lost seat" can never be compensated if the "next planes are full"
- This situation is detected and the number of input blocks is temporarily reduced from 4 to 2 during the time needed to clear the delayed blocks.
  - Equivalent to create more seats than passengers during a short time
- Then, the nominal number of blocks is re-established

- Only 2-3 clock cycles between consecutive frames
  - The bandwidth of the link is used at ~100%

Status and To be done

- New DAQ link IP has been tested successfully in several setups here in our labs and also at Boston U with 2 AMC13s (Virtex 6 version)
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- Good/close collaboration with AMC13 designers (E. Hazen, S. Wu, C. Hill)

- To be done :
  - Port of the IPs for the AMC13 Gen 2 based on Kintex-7, on going and soon done !
  - Using Kintex evaluation board KC-705
  - Repeat the same tests as with AMC13 Gen 1 on AMC13 Gen 2
  - If data size requires it, increase from 5 Gb to 10Gb using the new AMC13 but keep the same protocol

"Protocol in-depth"

The protocol is based on 32-bit data path (using the 8/10 bit code)

During the idle state, the block send x7CBCDC1C (k= "1111"; all K bytes)

Each frame starts with x00FB (K= "01")
And end with CRC and 0xFD00 (K = "10")

All Bytes between have a meaning (data, Word-count,..)

Init frame:
Sequence number : 0x0000000 (32bit) bit 31 =0
LSC_ID: (16bit)
Length : 16bit = 0 for init

Command frame:
Sequence number : 0x0000000 (32bit) bit 31 =0
LDC_ID: (16bit)
Length : 16bit
Command (32 bit (bit31= 1 specify a write = 0 a read)
DATA (32-bit each)

Data frame:
Sequence number : 0x0000000 (32bit) bit 31 =0
LSC_ID: (16bit)
Length : 16bit
Command (64bit : specify the content of the frame)
DATA (64-bit each)

Ack frame:
Sequence number : 0x0000000 (32bit) bit 31 = 1
LDC_ID/LSC_ID: (16bit)
Reserved: 16bit
data(64 bit (data /status)