AMC13 Module
CMS MicroTCA Overview
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at Boston University
and the CMS Collaboration worldwide

See http://www.amc13.info for detailed documentation
Outline

- CMS is going MicroTCA (.0 but not .4)
  - Brief review of crate configuration
  - Brief tour of cards in production
- AMC13XG Module status report
  - Design Update
  - 10G link testing
  - TTC path temperature coefficient
“MTCA.CMS” Crate
(note MTCA.0 but not necessarily MCTA.4)

One specific geometry shown, others possible...
“MTCA.CMS” Crate Requirements

- Dual-star backplane with redundant clocks
  - Fabrics A, B routed star-wise to both MCH sites
  - MCH2 CLK1 routed star-wise to AMC FCLKA
- Full-height, double width slots (pref. 12)
- Vertical cooling
MicroTCA installation in CMS

• Subsystems installing uTCA now or soon:
  – HCAL back-end
  – TCDS system
  – Global trigger
  – Calorimeter trigger
  – Muon trigger

• Incomplete list!
HCAL Backend Electronics: HF will upgrade to uTCA in LS1

TDR concept is becoming reality

- Pre-production HF uHTRs recently completed at Saha (India)
- Successful Electronics System Review in June
- Installation targeted for early 2014

- 10 Gbps-capable pre-production AMC13 (AMC13XG) recently delivered at Boston University
- Development and testing firmware with uHTR underway
Upgraded TCDS with upgraded Global Trigger

TCDS: TTC/TTS replacement system
Several MicroTCA crates; various modules
Calorimeter Trigger: Layer 1

Stage-2: CTP7

- Based on Virtex-7 XC7VX690T FPGA
- Zynq processor running Xilinx PetaLinux for service tasks
- Baseline Layer 1 hardware
- Link power distribution to support a mixture of speeds
  - 4.8/6.4 Gbps inputs
  - 9.6/10 Gbps outputs
- Schematic design completed
- Layout in progress
- Component count will be:
  - Higher than CTP6 (μTCA)
  - Lower than oRSC (VME)

CTP6 – Virtex-6 based prototype for CTP7

See TWEPP 2012:
https://indico.cern.ch/contributionDisplay.py?contribId=86&confId=170595&sessionId=54
https://indico.cern.ch/contributionDisplay.py?contribId=97&confId=170596&sessionId=53

Andrew W. Rose, Imperial College
Calorimeter Trigger: Layer 2

Stage-2: MP7

- 1.5Tb/s optical signal processor
- Xilinx Virtex-7 FPGA:
  - XC7VX485T or XC7VX690T
- Advanced boot-loader & diagnostics (full system test at start-up)
- On-board firmware repository
- $2 \times 144$Mbit 550MHz QDR RAM (optional)
- Been in hand for over a year
  - Continuous testing over that period
  - Very well understood
- Extensive software and firmware

Imperial MP7 processor board

See also TWEPP 2012:
https://indico.cern.ch/contributionDisplay.py?contribId=86&confId=70593&sessionId=51
https://indico.cern.ch/contributionDisplay.py?contribId=97&confId=70593&sessionId=53
CMS Muon Track Finder
3 uTCA crates with various modules

(Virtex-7 Version soon)

Virtex-6 Core logic module

- Custom backplane connector
- Core logic FPGA
- Control FPGA
- uTCA connector
- 1Gb FLASH Main FPGA firmware storage
- PT LUT module connector
- Control FPGA JTAG
- FMM connector
- SD card connector
- MMC USB console
- MMC JTAG
- MMC CPU

Estimated power consumption: ~50 W (assuming FPGAs nearly full)
PT LUT mezzanine not included

MMC = Module Management Controller
L1 Muon and Global Trigger

- The MPC mezzanine card for parallel operation of the CSC trigger was reviewed and approved for production launch (U.S. funding also has been identified)

- A prototype of the memory module for the upgraded muon track-finder micro-TCA electronics (MTF7) has been successfully tested.
  - 1GB of RLDRAM used for $P_T$ assignment using track “fit” parameters
  - Can clock 5 muons in 1 BX, added latency (~2.5BX) is under study

- Documents prepared for Global Trigger Upgrade:
  - Trigger Menu Editor specification reviewed, key for menus
  - Data interface document prepared as CMS Internal Note
FC7 motherboard for TCDS modules
The CERN GLIB

- Conceived as a test board, but may well end up installed at P5 in various systems
- 100+ produced!
The AMC13XG
What is AMC13?

- It is *not* an MCH! It is a 13th AMC in MCH-2 slot
- It distributes LHC clock / timing / controls to AMCs
- It collects DAQ data from AMCs
- It provides standard interface to CMS subdetectors:
  - CMS DAQ via 1-3 optical fibers (currently at 5.0 Gb/s)
  - TTC via 1300nm fiber @ 160Mb/sec biphase mark code
    - Future TTC upgrade may be supported
  - TTS via 1300nm fiber with protocol *t.b.d.*
- Latest version is 10Gb/s capable on backplane and optical links
History / Versions

- **DTC (2010, 3 built)**
  - Based on NAT-MCH
  - Prototype all functions

- **AMC13 (2011, 17 built)**
  - Based on new T1
  - New port assignments

- **AMC13XG (2013, 15 built)**
  - Redesigned T1 (only)
  - 10Gb/s links

 XC3S200A / XC6V130T

 XC6SLX25T / XC6VLX130T (or 240T)

 XC6SLX25T / XC7K325T
AMC13XG (XG = Ten Gigabit)

- AVR32 uC MMC
- Spartan-6 FPGA
- DDR3 SDRAM
- T3 connector (JTAG, I2C)
- Tongue 1 PCB
  - GbE, Fabric A
- Tongue 2 PCB
  - Clocks
- Quad SFP+ Optical cage
- Kintex-7 FPGA
  - With heatsink

T3 connector board removed to show internal detail
AMC13XG Front Panel

- **LED1**: (MMC Red LED)
- **Serial #**: (MMC console)
- **USB**: (MMC console)
- **JTAG**: (MMC AVR-32)
- **JTAG**: (AMC13 FPGAs)
- **LED2**: (MMC Green LED)
- **SFP0**: (DAQ Loop-back test)
- **SFP1**: (DAQ Output)
- **SFP2**: (Spare)
- **SFP3**: (TTC/TTS)

3x SFP+ 10Gb/s capable

Functions listed for initial HCAL firmware
Out of time!

Summary:
- CMS adopting MTCA.0 widely
- “final” AMC13XG design complete
  - built in qty 15
  - Larger scale production starting late 2013
- Keeping an eye on MTCA.4, trying not to be explicitly incompatible
Reserve Slides
Why Not .4? Mainly history...

- CMS converged on uTCA in 2009. Requirements:
  - Vendor standard crate
  - Backplane clock and TTC distribution
  - DAQ with ~ 400MB/s * 2 per crate
  - 12 slots preferred due to detector modularity
  - “DTC” prototype completed (NAT-MCH mezzanines)
- Further details settled in 2010:
  - MCH2 site used for AMC13 timing/DAQ module
  - Only fabrics A, B used for infrastructure
  - MCH2 tongues 3, 4 (fabrics D and up) available for user applications
- This is not incompatible with MTCA.4 (though we “prefer” full-height AMC slots)
AMC13 Clock Paths

- Low-jitter clock path
  Measured jitter << 10ps (measurement limit)

- TTC through FPGAs, but re-timed to clock at backplane
AMC13 DAQ Path

- Link Tx (in AMC)
- MicroTCA Backplane 5.0 Gb.s
- FIFO
- Event Builder
- TTC
- L1A FIFO
- 8k event SDRAM
- IPbus control / monitor / local DAQ
- DAQ Tx
- DAQ Fiber
- Possible 2nd DAQ fiber
- GbE

Note: Data could flow through SDRAM

Fiber Out 5.0 Gb/s (to 10 Gb/s)
AMC to AMC13 backplane link

AMC (e.g. HCAL uHTR)

- BU provided firmware
- LHC clock
- L1A
- BC0 etc
- TP[0:7]
- BC0
- CLK
- Data
- Framing
- Buffer Status
- Level 1 Trigger
- TTC Receiver
- MUX
- Level 2 DAQ
- MGT
- 12 point-to-point links
- 80 Mb/s TTC Protocol Fabric B
- 5 Gb/s 8b/10b Fabric A
- AMC13
- IO
- MGT
- AMC13 links
- Fabric A
- Fabric B

16-bit buffer status

26 Sept 2013
25 / 40
Link to CDAQ

- 5.0 Gb/s optical link with “S-Link like” protocol
- Firmware developed by CDAQ (both ends)
  - Error check coding, retransmission on error
  - Error monitoring
  - Full diagnostic and test capability from receive end

Data from FED
- DATA (64 bit)
- WEN
- UCTRL
- CLOCK
- Backpressure
- link down

4 blocks (4Kbytes each)
Block is sent until it is acknowledged

- Receive block
- Ack. block
- Order blocks

Send commands (one at the time)
T1 PCB Stackup

Nelco 4000SI-13 Material

1  GTL  |  Prepreg 2.7 | Impedance control (10G, SDRAM)
2  GP1  |  Core 5.0   | GND
3  GP2  |  Prepreg 5.4| Split power
4  G1   |  Core 5.0   | Impedance control (SDRAM)
5  GP3  |  Prepreg 2.7| Split power
6  GP4  |  Core 5.0   | GND
7  GP5  |  Prepreg 5.4| Split power
8  G2   |  Core 5.0   | Impedance control (SDRAM)
9  GP6  |  Prepreg 5.4| GND
10 G3  |  Core 5.0   | Impedance control (10G, SDRAM)
11 GP7 |  Prepreg 2.7| GND
12 GBL |  Impedance control (10G, SDRAM)

Overall: 1.6mm
Signal: 18μm
Power: 36μm
Top Layer 1 (signal)

- **DDR3**
- **Kintex-7**
- **UTCA connector**
- **DDR3 power**
- **LS to T2**
- **HS to T2**
- **1.8V**
- **2.0V**
- **3.3V Payload**
- **1.0V**
- **1.2V**
- **1.0V aux**
T2 PCB Stackup
Standard FR-4 Material

1. GTL
   1. 5 mil dielectric

2. GP1
   2. 3 mil dielectric
   3. 9 mil dielectric

3. GP2
   4. 9 mil dielectric

4. G1
   5. 9 mil dielectric

5. GP3
   6. 9 mil dielectric

6. G2
   7. 9 mil dielectric

7. GP4
   8. 5 mil dielectric

8. GBL
   Impedance control (TTC)

Overall: 1.6mm
Signal: 18μm
Power: 36μm
T2 PCB Layout

- Spartan 6 FPGA
- UTCA connector
- Fabric B (TTC)
- AVR 32 (MMC)
- Clock fanout ICs
- Connector to T3
- Connector from T1
Eye Patterns on Serial Links
Backplane Test in VT892 Crate
Double-length (loop-back) test

AMC13XG (Kintex-7 FPGA)

GTX

MCH2 connector

~5 cm PCB (Nelco)

AMC1 connector

20 cm (est) backplane PCB

Jumper Board

Total length: 50 cm (3.3ns)

NOTE: Preliminary!
still tweaking parameters

5.0 Gb/s

10.0 Gb/s
10GB Fiber Loop-Back Test

MCH2 connector

AMC13XG (Kintex-7 FPGA)

GTX

SFP Transceiver
Avago AFBR-703SDZ

~3 cm PCB (Nelco)

30M Fiber

10.0 Gb/s

NOTE: Preliminary! still tweaking parameters
Temperature Sensitivity of AMC13 Clock network
TTC Clock Delay Testing
904 (E. Laird) and at BU

Goal: Measure phase shift between TTC input and clock on uTCA backplane
Repeated Power Cycles

B. 904 (E. Laird et al)
Note: vertical scale inverted

- Measure TTC to custom AMC rx card
- 6 power cycles of whole uTCA crate
- Converges in $O(200s)$
- Slow drift seen but very low level,
  - nearly unmeasurable with this setup

Hypothesis: temperature effect
Delay vs position in AMC clock chain

2814 has no delay/phase spec!

- SFP
  - 1300nm receiver (ATM type)
  - Compatible with TTC fiber data
- ADN2814
  - Clock/data Recovery
- SY89832
  - Fanout
  - T1 U3
- SY89872
  - Divide by 2/4
  - 160MHz x 4
- LVDS
- Future Option
  - For ext clock
- SY89832
  - Fanout
  - T2 U23
- DS91M125
  - 1:4 Fanout
  - 40MHz Clock
  - To uTCA backplane
- Tongue 2
  - M-LVDS

Measured phase shift vs warm-up
- All +/- at least 20ps

These MLVDS drivers have spec'd Tempco of 10 ps/°C
Delay vs Temp @ BU

Change crate temp by blocking cooling. Temp measured in air near AMC13XG

Δ delay at input to MLVDS drivers

Total plot range corresponds ~ to normal warm-up

![Temperature vs Delay Graph](image)

Slope: 25.8 ps/°C
Phase shift: Conclusions

- Phase shift with temperature is not unexpected, and is much less than the old TTCrx
- The phase is stable after 200s or so warmup
- It is fine for foreseen applications
- ~ half of the shift is in the clock/data separator IC which is the heart of the design
- Improving it would require starting over on the clock path design
- A modest improvement could be gained by switching from uTCA-standard MLVDS to LVDS
  - And, Mr Wu told us so from the start!
AMC13 Board Stack

- Base configuration has only tongues 1, 2
- Base board - With optics and HS links (Fabric A)
- Clocks board - distributes LHC clock and controls
- Mezzanine connector for T3 with I2C
  - T3 has JTAG and LEDs

T1 base board
- MMC functions (Wisconsin firmware)
- TTC optical rx
- 3x SFP+ cage
- Cross-over GbE from MCH1 for controls and local DAQ

T2 Clocks board
- Clock / controls fanout

T3 board
- Provides JTAG / LEDs on front panel
- Can be removed after initial programming
- Crosspoint switch or other custom board can be installed here (but see notes!)

Quad SFP+ Cage

Connector to T3 provides:
- Power
- JTAG (MMC and Xilinx)
- Utility SPI
- MMC serial console